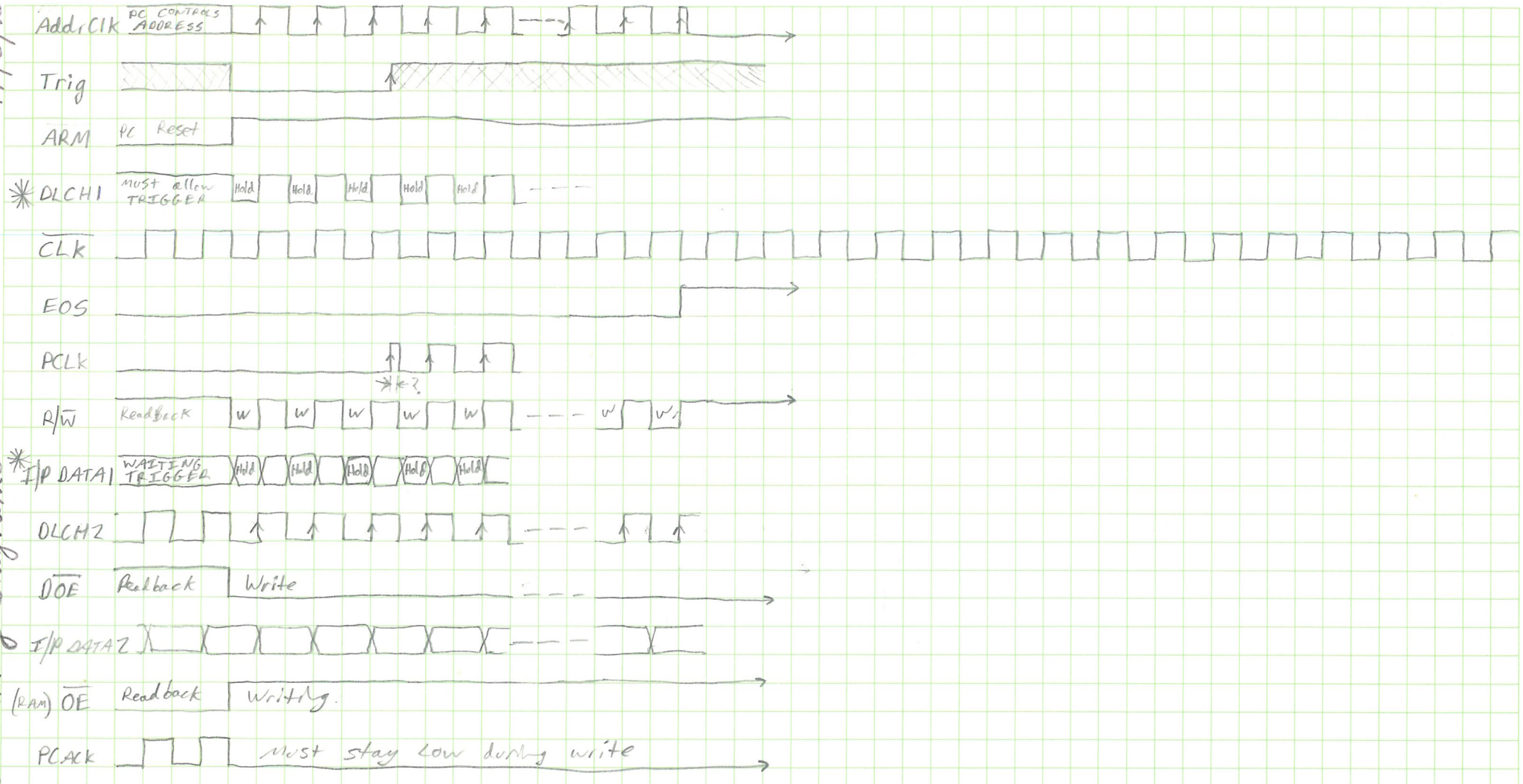
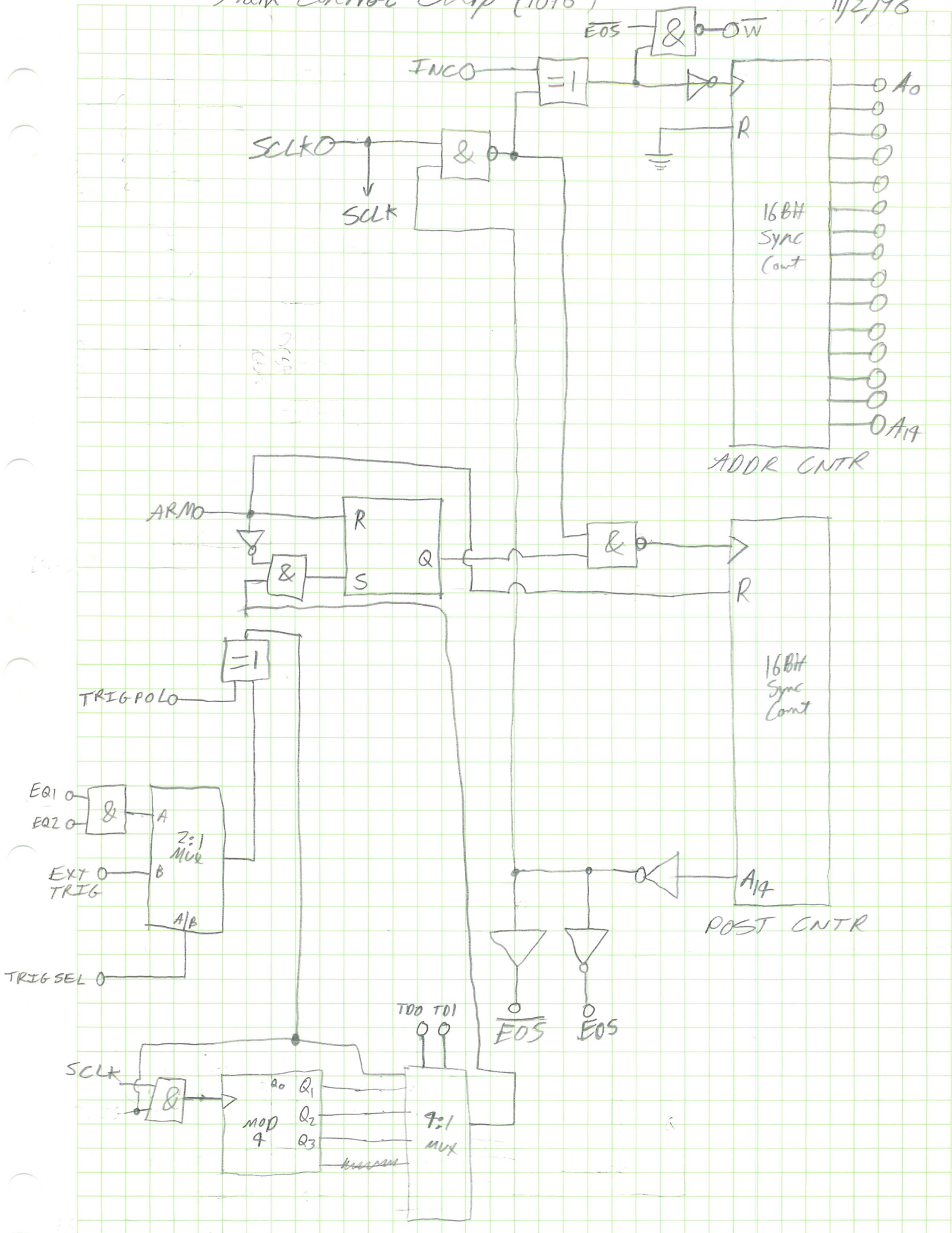
17/8/95

PCLA Rev 1.0 Timing Diagrams



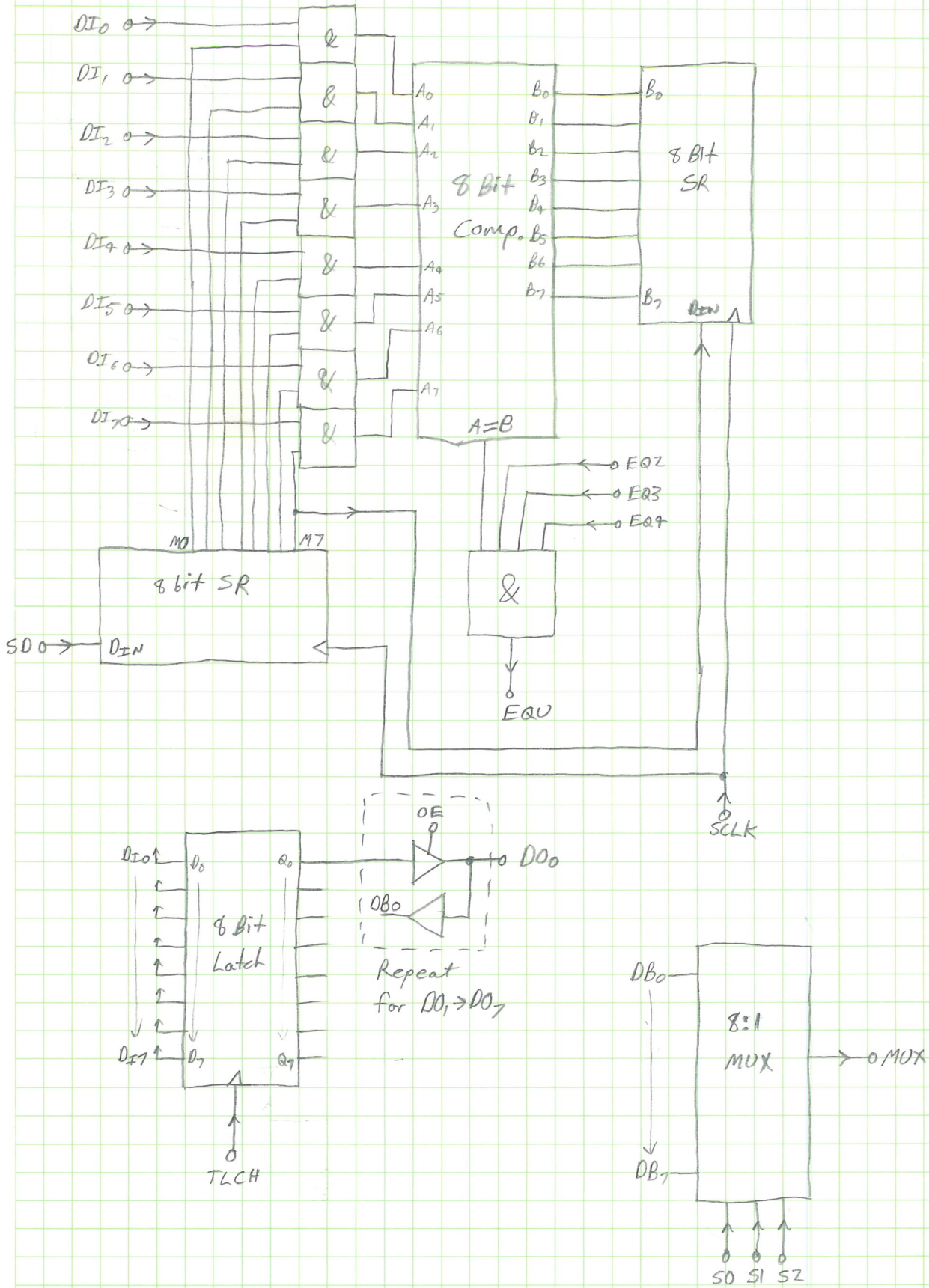
NOTE :- DLCH1 & I/P DATA1 ARE for 74573 Transparent latch I/P Design.
- DLCH2 & I/P DATA2 ARE for Buffered I/P, latched o/p Design.

Main Control Chip (1016) 11/2/96



Logic Analyser Trigger Chip (LATC)

28/8/95



Control Circuit concept

25/8/95