Dare! Design Tips for designing CE compliant PCB boards (personal notes)

* **Ground Planes**
  Multiple ground planes always cause unwanted return currents between these copper planes;
  so it is *much* better to use ONE single ground plane.

  A copper ground plane is in itself incredibly low impedant!.

  This means that connector shells should be directly tied to the ground
  (reference) plane, just like the GND signal pin of the connector.
  This is okay, as return currents follow the shortest path, which is under the signal trace.

  The only way to use multiple ground planes is to stitch them with **lots** of via's;
  using a X-Y via grid with a pitch being lower than 1/10 of the shortest wavelength.
  This is very time-consuming in production, so very expensive.7

  So one ground plane covering the entire board is execllent; more planes only cause harm.
  Power (non-ground) planes are generally not advisable, except as a local heat sink area.
  It is much better to have high impedant power traces that are well decoupled locally (see below).

* **Decoupling**
  It is crucial to keep (the area of) current loops as small as possible, especially for high-frequent signals.
  So the power supply traces and wires only should carry a DC component.
  To do this, power pins of a chip should be decoupled with at least a 10nF and 100nF X7R capacitor in parallel,
  and with a ferrite bead to the power line near the chip.
  Small ferrite beads carrying a current saturate and loose much of their their magnetic properties.
  Chips with multiple power pins each should al least get their own 10nF decoupling capacitor.
  Decoupling capacitors should be connected with short, thick traces and two vias to the reference plane.

* Design boards with analog and digital circuitry as if you make a classic board
  with separate analog and digital reference planes; but just use a single reference plane.
  This guarantees that analog and digital signals are well separated.

* **All connectors should be placed at one side of the board.**
  This minimizes common-mode currents flowing through your reference plane,
  and also makes your board more immune to ESD spikes.
  Thus ESD currents flowing from cable A to cable B will flow along your board edge, and not across your board.

* Power entries to the board should get a Pi-filter consisting of a **small 10NF** capacitor to ground,
  a good ferrite bead, and a bulk capaitor and a second small 10NF capacitor to the ground (reference) plane.

  The ferrite bead should have an impedance of >= 100Ohm over the full spectrum **at the nominal bias current**.

  The small 10NF caps are very low impedant for >= 1GHz signals and for typical sub-nanosecond ESD spikes.
  NB: a capacitor acts as a band filter in the multi-MHZ to GHz regions, dependent on capacity and physical size.

* Low-frequent data lines should be decoupled using a L-C filter (Z >= 100 Ohm at 30MHz - 1GHz),
  and a C around 470pF.

* For isolated serial ports, the isolated 0V should be decoupled with a high-voltage capacitor
  to the ground plane using short and thick traces.
  The data lines should be decoupled to the local ground with minimal bandwidth.

* Often is is handy to make a metallized strip at the edge of the board with the connectors. This allows you to extend the ground plane is a very low impedant way, and also to add ground fingers to the case if needed.

A **PCB side metallization** can be made by adding a local TOP and BOTTOM ground plane strip, and then stitching them with a series through hole pads with rather big holes (say 1-2mm), then mill those plated holes into half (option called "copper to the board edge" at Eurocircuits). You then end up with an extended ground plane tat is available on the top, bottom and side edge of the board. The sharp poststamp-like serrated bare copper edge can help to attract ESD sparks during CE testing.

* a wide-band non-differential signal that runs over a reference plane (for example a clock signal) will emit very little as long as it is terminated well!

* Do not route high speed signals along the edge of the ground plane; try to keep the outer 10mm free from fast signals.

* By the way, self-adhesive copper tape is no good long-term grounding solution. The glue will loose its adhesion over time.

* Use spread-spectrum clocking to improve the quasi-peak emission measurement where possible. This sweeping should be done quickly (with a >= 20kHz cylcle) because the quasi-peak measurement has a short attack and slow decay time. Sweeping slowly does not yield much improvements because of this fast attack/slow decay quasi peak circuit.

USB, Ethernet and all PLL-locked signals cannot be spread-spectrum clocked; but most other digital signals can be spread-spectrum clocked without any problem.

* a metal enclosure should be treated as an extension of the electrostatic shield, and should be connected to the ground plane at all cable entry points for best signal integrity and immunity. All metal parts should be bolted to any metal frame/chasis with serrated rings for best ground contact.

* a ‘star ground’ concept is a relict from old audio times. Forget it for RF and for CE-compliant designs!