Understanding Modern Power MOSFETs

Fairchild Power Seminar 2006

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Session Objectives

- Explain what a board designer needs to know about MOSFETs
- Explain how to choose a MOSFET for synchronous buck applications
  - Which MOSFETs are needed for a 12V input, 1.2V output, 20A, 300kHz buck converter?
  - How are they selected?

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Agenda

- DC behavior explaining $R_{DS(ON)}$
- Thermal behavior
- Avalanche breakdown
- Switching behavior
  - Explaining the effects of gate charge
- Synchronous buck circuitry
- Half-bridge structure

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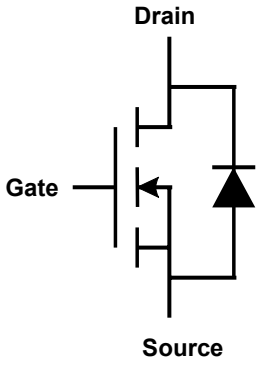
Introducing the N-channel MOSFET

- In power electronics, a MOSFET is usually used to implement a semiconductor switch
- Consider the N-channel (enhancement mode) MOSFET
- If 0V is applied between gate and source (V_{GS} = 0V) the MOSFET switch is open
- If a large positive voltage is applied between gate and source (e.g. V_{GS} = 10V), the MOSFET switch is closed
- As the gate is high impedance it should NEVER be left open
  - This applies to logic inputs on chips for the same reason



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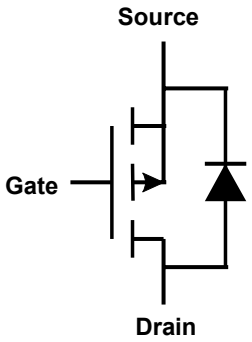
Introducing the P-channel MOSFET

- Sometimes P-channel MOSFETs are used
- Consider the P-channel (enhancement mode) MOSFET
- If 0V is applied between gate and source (V_{GS} = 0V) the MOSFET switch is open
- If a large negative voltage is applied between gate and source (e.g., V_{GS} = -10V), the MOSFET switch is closed



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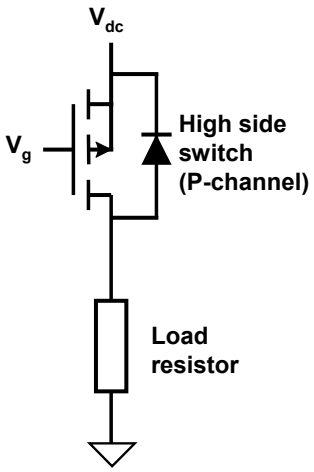
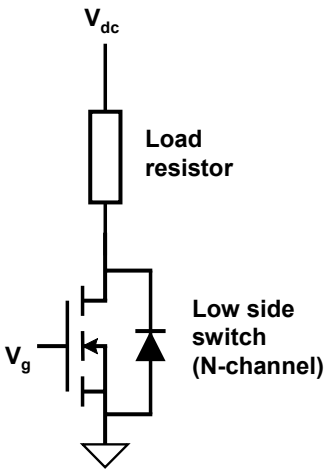
High Side and Low Side Switches



Switches on fully if (V_{dc} – V_g) > 10V



Switches on fully if V_g > 10V

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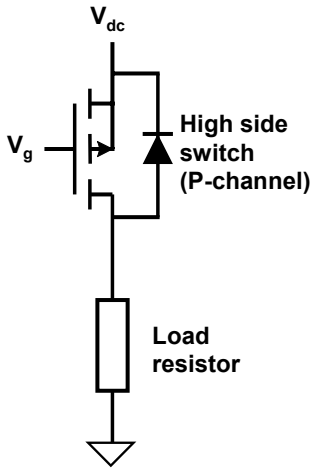
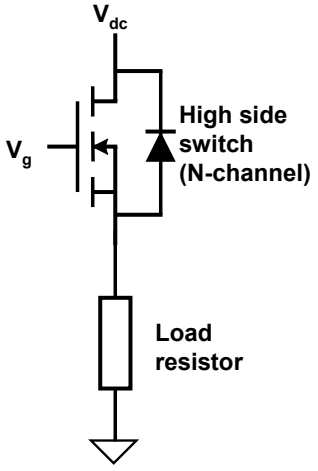
High Side Switch Options





- Simple drive circuit
- Higher $R_{DS(ON)}$ than for N-channel
- Watch out for V_{GS} max when driving

- Turns on fully only if $V_g > V_d + 10V$
- Bootstrap or charge pump drive needed

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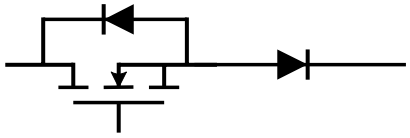
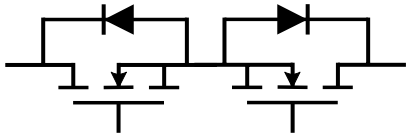
Uni-directional and Bi-directional Switches

- All MOSFETs have a body diode
- A single MOSFET switch can block voltage in only one direction
- To block voltages in both directions, a diode is needed
  - This allows uni-directional current flow
- To block voltages in both directions, allowing bi-directional current flow, a second MOSFET is needed
- This configuration is used in
  - Battery chargers
  - Lighting dimmers





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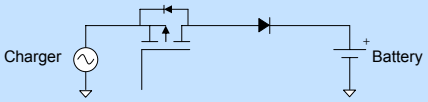
Uni-directional Switch Example

Design challenges
- Size
- Power dissipation
- I_D capability

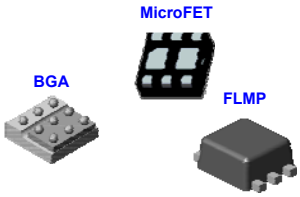
Topology choices
- Single PMOS & Schottky
- Dual PMOS (bi-directional)

Charger Application Circuit

MOSFET used as a current source

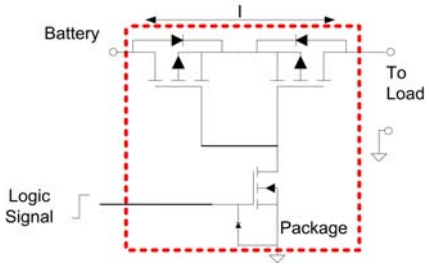


Proposed solutions to meet design challenges
- Single PMOS BGA or FLMP MOSFET
- Single PMOS & Schottky MicroFET MOSFET
- Dual PMOS FLMP MOSFET or MicroFET MOSFET



Bi-directional Switch Example

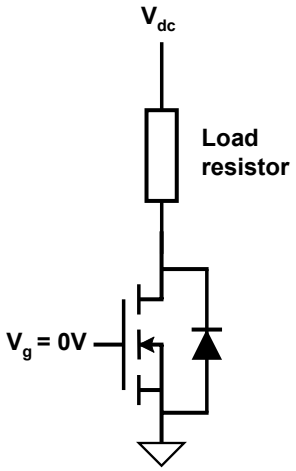
Bi-directional advantages
- Full isolation in 'OFF state'
- Bi-directional current control
- Reduced loss vs. standard diode
- Additional protection
- Full function in SSOT-6
- Accessory connector & USB Interface
- Ideal for applications where bi-directional operation, leakage protection, and digital control are required.



Package	V_{gs} Max.	$R_{ds(on)}$ Max (mΩ)			Part Number	Release
		V_{gs} @ - 4.5V	V_{gs} @ - 2.5V	V_{gs} @ -1.8V		
SSOT-6	8	250	350	450	FDC6332L	Released

MOSFET Voltage Rating

- When a MOSFET is in the OFF state, it prevents current flowing through the load, except for a small leakage current, I_{DSS}
- Here, V_{dc} must not exceed the maximum specified drain-source voltage of the MOSFET, V_{DS} max
- The ability of a MOSFET to block voltage
  - Decreases with temperature
  - Decreases with negative V_{GS}



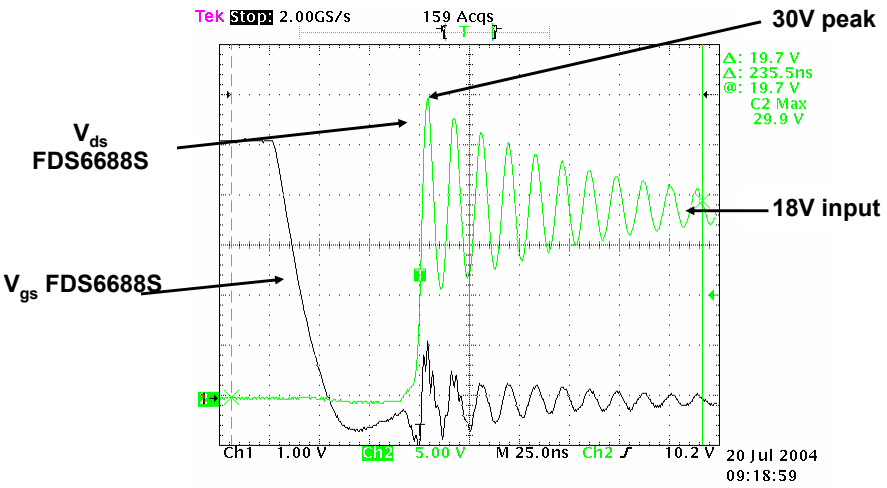
Choosing the Right Voltage Rating

- The voltage rating of the MOSFET must be larger than the bus voltage V_{dc}
- Allow safety margin for:
  - Bus voltage variations
  - Input voltage spikes
  - Ringing in synchronous buck
  - Motor drive spikes
  - Flyback transformer spikes
  - Change in V_{DS} at low temperature
  - Change in V_{DS} with negative V_{GS} drive

Typical MOSFET voltage ratings

Portable equipment	***20V***
FPGA, VLSI supply	***20V,30V***
24V motor drive	***60V***
48V system	***80-100V***
80V system	***150-200V***
85VAC – 220VAC	***450-600V***
Three phase PSU	***800-1000V***

Example of Ringing on Switching Node



FDS6294 upper FET / FDS6688S x2 Lower FET

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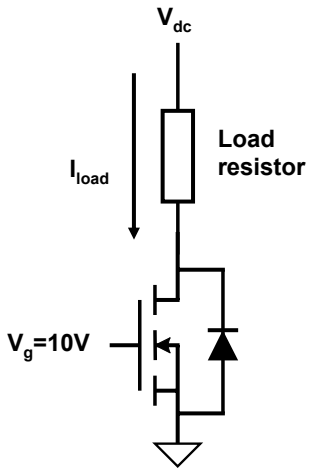
MOSFET Current Rating

- All MOSFETs have a specified maximum current rating
  - Continuous operation
  - Peak pulse current for some MOSFETs
- In practice, $R_{DS(ON)}$ is more often used for choosing MOSFETs
- The peak pulse current curves are useful in motor drives and other industrial applications



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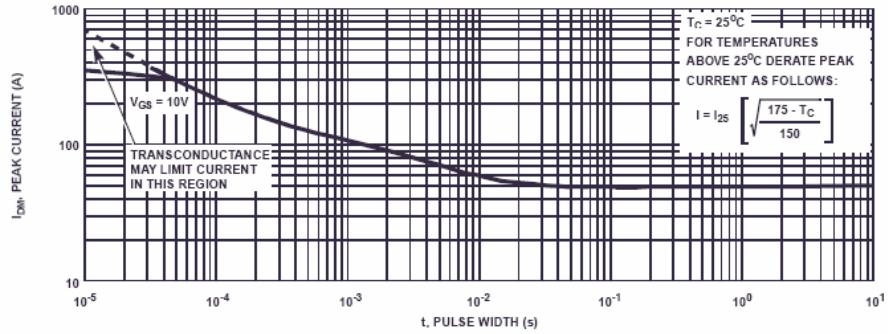
FDD16AN080AN Peak Current Rating



Peak Current Capability

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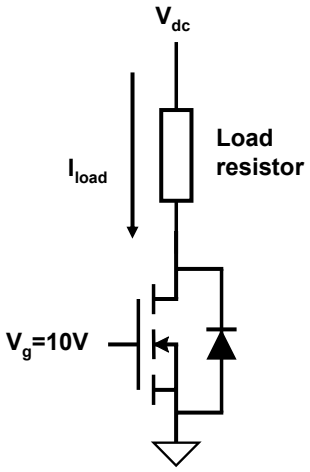
Conduction Losses

- When a MOSFET is in the ON state, it behaves like a resistor
- The resistance between the drain and the source is $R_{DS(ON)}$
- So the power dissipation is $I_{load}^2 x\ R_{DS(ON)}$
- For a given device, $R_{DS(ON)}$
  - Increases with temperature
  - Decreases with V_{GS}
  - Slightly increases with current



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Example: FDD16AN080AN $R_{DS(ON)}$

On Characteristics

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu A$	2	-	4	V
$r_{DS(ON)}$	Drain to Source On Resistance	$I_D = 50A$, $V_{GS} = 10V$	-	0.013	0.016	Ω
		$I_D = 25A$, $V_{GS} = 6V$	-	0.019	0.029	
		$I_D = 50A$, $V_{GS} = 10V$, $T_J = 175^oC$	-	0.032	0.037	

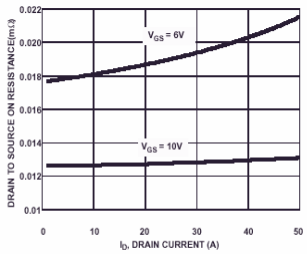


Figure 9. Drain to Source On Resistance vs Drain Current

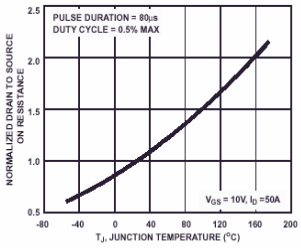
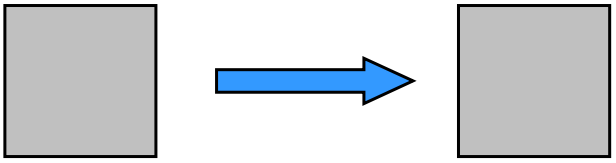


Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

Effect of Technology on $R_{DS(ON)}$

- For a given technology
  - Increasing the required V_{DS} max rating will increase the $R_{DS(ON)}$ for the same die size
  - Increasing the die size will decrease $R_{DS(ON)}$
- One of several important targets when developing newer MOSFET technologies is to improve the specific $R_{DS(ON)}$
  - Formally measured as $R_{DS(ON)}$ x square millimeter
  - Often simply $R_{DS(ON)}$ x square
- Our new SuperFET™ technology has a lower specific $R_{DS(ON)}$ than our CFET technology
  - CFET technology - 0.65Ω/600V device fits into D^2PAK
  - SuperFET technology - 0.19Ω/600V device fits into D^2PAK

Maximum Rated Voltage Impact on $R_{DS(ON)}$



Increasing the maximum rated voltage for the same die size:

- Increases the $R_{DS(ON)}$

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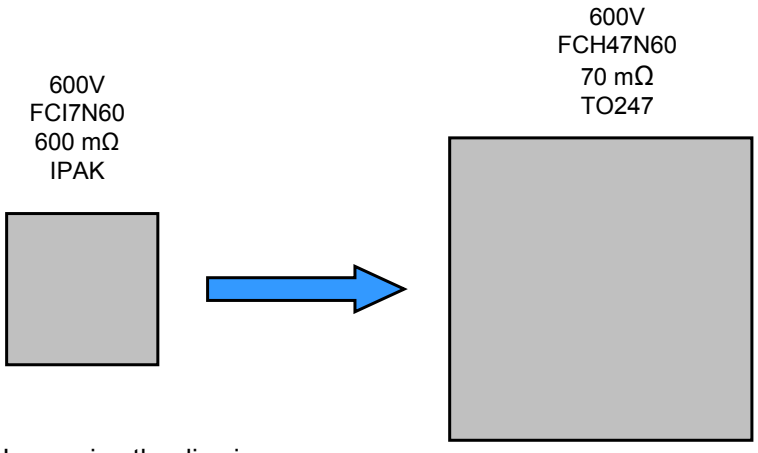
Die Size: Impact on $R_{DS(ON)}$



Increasing the die size:

- Reduces the $R_{DS(ON)}$
- Increases the cost
- Increases the size of the package needed

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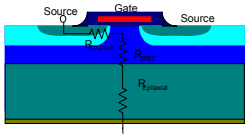
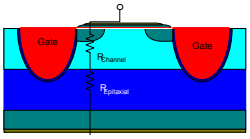
Technology Trends: $R_{DS(ON)}$ Perspective

Planar



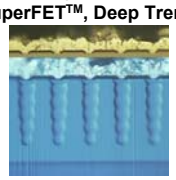
Reduce $R_{DS(ON)}$ by etching the gate into a "trench" (normally for low voltage MOSFETs)

Trench



Reduce the effect of V_{DS} max requirement on $R_{DS(ON)}$ by epitaxial/etched pillars (normally for high voltage MOSFETs)

Charge Balance (SuperFET™, Deep Trench)



The charge balance and trench approaches add extra manufacturing process steps in order to reduce the die size needed to achieve a given $R_{DS(ON)}$

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Comparison of MOSFET Key Parameters

75V MOSFET technology trends - Comparing MOSFETs of equal die size

	HUF75545P3 (Older Planar)	FDB045AN08A0 (Newer Trench)
$R_{DS(on)}$	10mΩ	4.5mΩ
Q_g	235nC	138nC
P_d	270W	310W
t_{rr} (@ 25°C)	100ns	53ns
Q_{rr} (@ 25°C)	300nC	54nC

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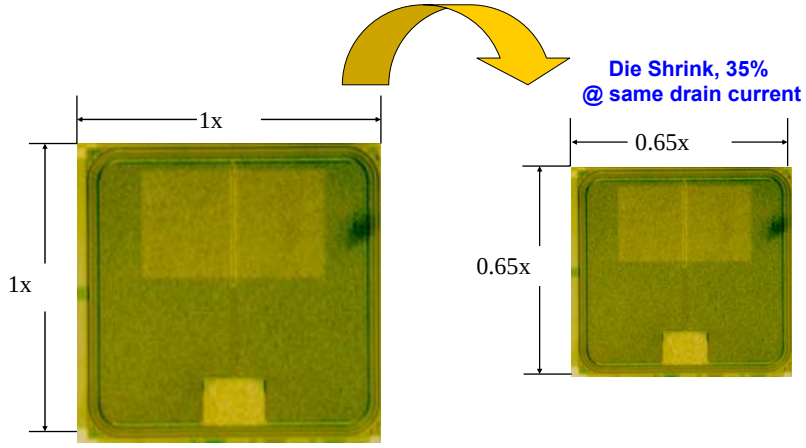
Die Comparison: Planar versus Charge Balance MOSFET



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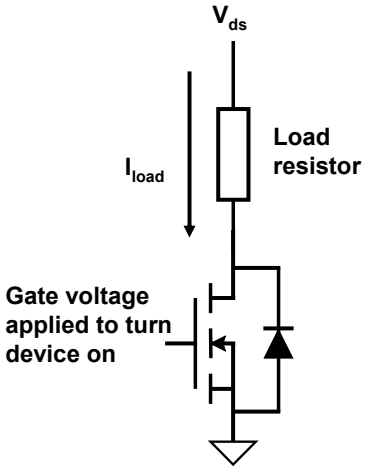
Gate Voltage

- A MOSFET will turn on if the gate voltage is somewhat larger than a parameter known as the threshold voltage, V_{TH}
- As $R_{DS(ON)}$ decreases with increasing V_{GS}, it is advantageous to drive the MOSFET gate much higher than the threshold voltage



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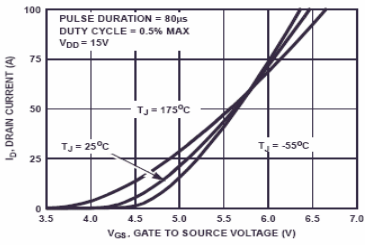
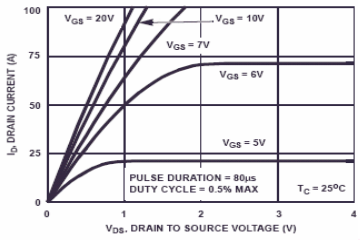
DC Characteristics

- The transfer and saturation characteristics show the relationship between V_{GS}, I_D and V_{DS}
  - If not otherwise specified, the forward transconductance, gm, which is the incremental change in I_D per change in V_{DS}, can be determined from the transfer characteristics
  - The saturation characteristics show the boundary between linear and saturation modes, and can also be used to estimate gm
- In saturation mode, $I_D = gm(V_{GS}-V_{TH})$: used when considering switching



Transfer characteristics



Saturation characteristics

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Maximum Permitted Gate Voltage

- The maximum permitted gate voltage, V_{GS} max is specified in the absolute maximum ratings of the datasheet
  - If this value is exceeded, the MOSFET will be destroyed
- Oscillation on the gate can lead to transient voltages, which could exceed V_{GS} max and therefore destroy the gate
  - Pay particular attention to the gate drive layout
  - Keep the gate drivers very close to the gate
- If using negative gate drive on the MOSFET, which we generally do not recommend, note that the V_{DS} max rating will also be reduced by the amount of the negative gate drive

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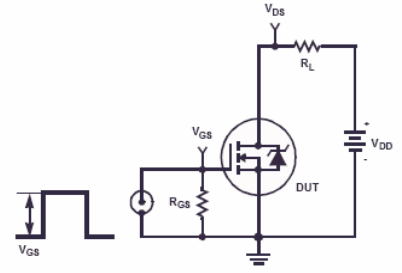
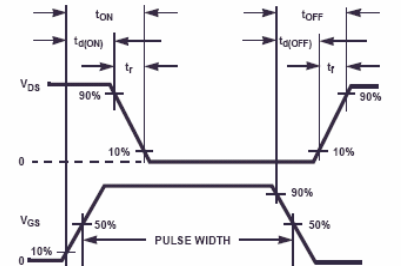
Switching Times for Resistive Loads



Switching Time Test Circuit



Switching Time Waveforms

- Switching times for resistive loads are measured with specified V_{GS}, V_{DS} and I_D
  - Here, R_g=0 during the on time, R_g=R_{GS} during the off time
  - Alternatively, a gate resistor is used
- Most MOSFET switching applications have inductive loads
  - For these applications, the above timing diagram is less useful than the gate charging characteristics reviewed later

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MOSFET Selection Criteria DC Operation

Main Criteria

- Voltage Rating (V_{DS} max)
- $R_{DS(ON)}$
- V_{GS} needed to switch on device sufficiently
- Package type (through hole or surface mount)
- Package thermal characteristics

Supplementary criteria

- Peak current rating

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Selection and Thermal Calculation Example

Example:

A switch is needed for the following DC drive application:

- V_{bus}: 48V (from local power supply)
- Nominal current: 4A
- Peak current: 8A for 2 seconds (infrequently)
- Ambient temperature: 85 deg C max
- DPAK (TO252) no copper area for cooling permitted

Select a MOSFET that can do this

- Taking absolute worst case assumptions
- Taking realistic assumptions

Ignore switching losses

Selection Steps

- The bus voltage is a well-regulated 48V supply
  - Fairchild offers 60V, 75V, 80V, 100V MOSFETs in DPAK
  - Select 75V to give sufficient margin
- From the FDDxxAN08 datasheets
  - Thermal resistance, junction-to-ambient for DPAK is 100K/W
  - Maximum junction temperature is 175°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case TO-252	1.11	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-252	100	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-252, 1in² copper pad area	52	°C/W

Selection Steps: Power Dissipation

Junction Temperature = Maximum Ambient Temperature + Thermal Resistance x Power Dissipation

Thermal Resistance = 100 K/W

Junction Temp Max = 175° C

Ambient Temp Max = 85° C

Power Dissipation Max = (175 – 85)/100 = 0.9W = I_{load}^2 x $R_{DS(ON)}$

(Switching losses have been ignored)

Selection Steps: Determining $R_{DS(ON)}$

I_{load}^2 x $R_{DS(ON)}$ = 0.9W (in the absence of switching losses)

As I_{load} = 4A, $R_{DS(ON)}$ needs to be less than 56 milliohms

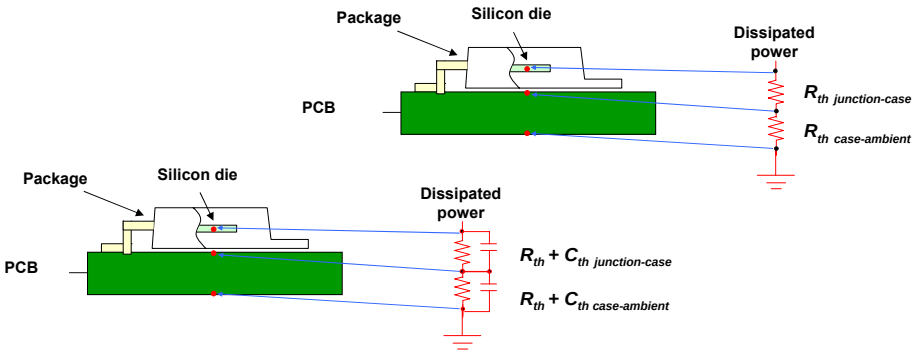
The $R_{DS(ON)}$ specification must be met at 175° C

Choose the smallest device (device with the highest $R_{DS(ON)}$) to meet this requirement: here the FDD16AN080A

On Characteristics

$V_{GS(TH)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250µA	2	-	4	V
$r_{DS(ON)}$	Drain to Source On Resistance	I_D = 50A, V_{GS} = 10V	-	0.013	0.016	Ω
		I_D = 25A, V_{GS} = 6V	-	0.019	0.029	
		I_D = 50A, V_{GS} = 10V, T_J = 175°C	-	0.032	0.037	

Simple Thermal Models



The upper thermal model considers just thermal resistance
It implicitly assumes that the PCB and the package heat up instantly.
In reality, all materials have a specific heat capacity.

This is modeled in the lower thermal model with a thermal capacitance.

Calculation of Die Temperature at 4A Continuous Current

- The calculation of die temperature using the previous formula will give a very conservative result
  - 100 x I_{load}^2 x $R_{DS(ON)}$ + 85 = 100 x 16 x 0.037 + 85 = 144° C
  - Reason: the $R_{DS(ON)}$ rating used is the 175° C rating
- So we calculate the temperature at 4A using iteration
  - The $R_{DS(ON)}$ versus temperature curve is approximated as a line
    - $R_{DS(ON)}$ = 1, T = 25° C
    - $R_{DS(ON)}$ = 2, T = 160° C
  - Here $R_{DS(ON)}$ is normalized with respect to the 25° C value
- The iteration spreadsheet is shown on the following page
  - The die temperature is around 125° C

Iteration Spreadsheet

Thermal resistance	100	K/W		Thermal resistance	1.11	K/W
Current	4	A		Current	8	A
Step	Temperature	Rdson		Step	Temperature	Rdson
		0.0140				0.0285
1	85.00	0.0202		1	125.81	0.0245
2	117.36	0.0236		2	125.53	0.0244
3	122.72	0.0241		3	125.53	0.0244
4	123.61	0.0242		4	125.53	0.0244
5	123.76	0.0242		5	125.53	0.0244
6	123.79	0.0242		6	125.53	0.0244
7	123.79	0.0242		7	125.53	0.0244
8	123.79	0.0242		8	125.53	0.0244
9	123.79	0.0242		9	125.53	0.0244

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Calculation of Temperature After the 8A, Two Second Long Pulse

- For estimation of the heating effect of the short 2 second pulse, we used the thermal resistance junction-to-case
- This assumes that
  - the die heats up in that short time (see thermal impedance curve in the datasheet)
  - the PCB does not heat up in that time
- For the short pulse, the extra heating is only a few degrees, so there is not expected to be a problem with this pulse
  - Full thermal modeling and verification by experiment is needed to validate this

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case TO-252	1.11	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-252	100	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-252, 1in^2 copper pad area	52	°C/W

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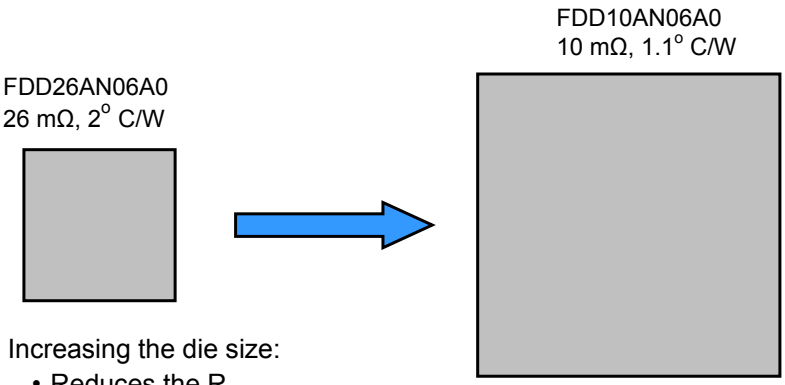
Die Size: Impact on Thermal Characteristics



Increasing the die size:

- Reduces the $R_{DS(ON)}$
- Increases the cost
- Increases the size of the package needed
- Reduces the thermal resistance
- Increases the thermal capacitance

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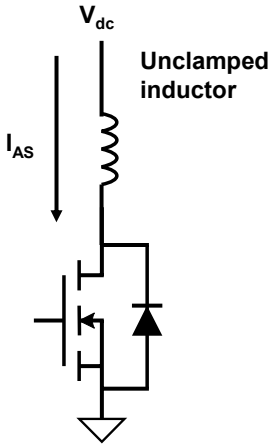
Avalanche Rating

- The avalanche rating, or unclamped inductive stress (UIS) rating is an indication of the robustness of a device to stress caused from external spikes and stray or load inductances
- The device is turned on until desired I_{AS} is reached, and then switched off



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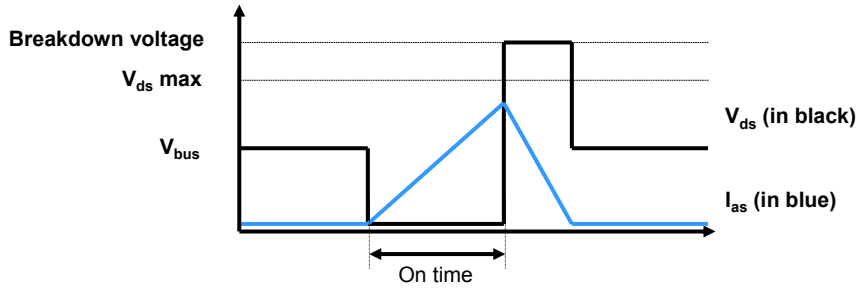
Avalanche Rating



- The inductor induces a voltage of V_{bus} + Ldi/dt onto the drain of the MOSFET
- The MOSFET breaks down and acts like a Zener, absorbing the energy from the inductor
- Avalanche stress ratings are stated as the maximum avalanche current, and as the maximum avalanche energy

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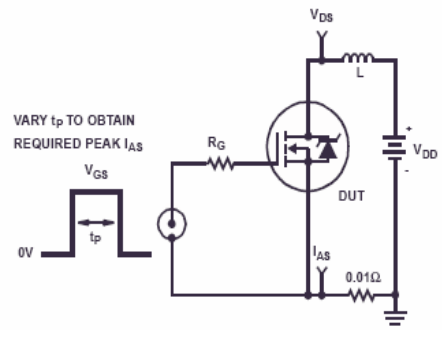
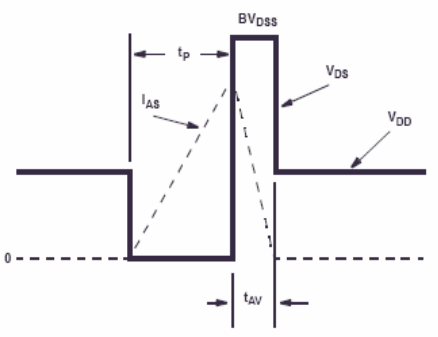
Avalanche Test Circuit and Waveforms

FDD16AN08A0



Unclamped Energy Test Circuit



Unclamped Energy Waveforms

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The Importance of Avalanche Current

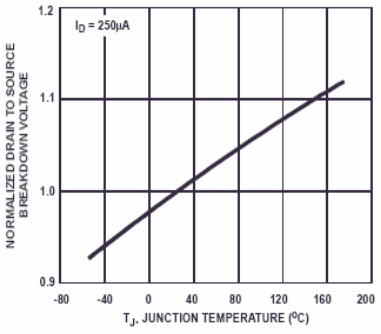
- The avalanche current I_{AS}, together with the time in avalanche, t_{AV}, are the factors determining whether a part will fail in avalanche or not
  - The failure mode which will destroy a device in avalanche is triggered by an effect involving heating

$$\text{maxenergy} = I_{AS}^{\ 2} \times \text{constant} \times t_{AV}$$
$$I_{AS}^{\ 2} \times t_{AV} = \text{constant2}$$

- The avalanche energy is less important

Effect of Temperature on Breakdown Voltage

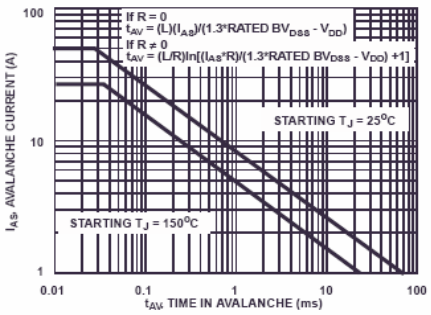
- The breakdown voltage increases with temperature
  - As the avalanche process heats up the die, the effective breakdown voltage is often higher, typically 30%
- At low temperatures, the breakdown voltage and the ability to block voltage drops



Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

Avalanche Rating for Medium Voltage MOSFETs

- The maximum I_{AV} specification needs to be derated for higher temperature operation
- For Fairchild Semiconductor automotive-rated parts, we provide curves showing the I_{AV} at junction temperatures of 25° C and 150° C



FDD16AN08A0: Unclamped Inductive Switching Capability

$$t_{AV} = \frac{LI_{AS}}{B_{VDSS} - V_{DD}} \qquad E_{AS} = \frac{1}{2} LI_{AS}^2 \times \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

FAIRCHILD SEMICONDUCTOR

Avalanche Rating for High Voltage MOSFETs

- **For high voltage MOSFETs, we specify I_{AS} max and E_{AS} max at 25° C**

Absolute Maximum Ratings T_C = 25°C unless otherwise noted

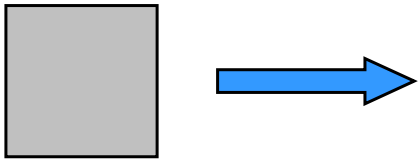
Symbol	Parameter		FCP11N60	FCPF11N60	Units
I_D	Drain Current - Continuous (T_C = 25°C)		11	11*	A
	Drain Current - Continuous (T_C = 100°C)		7	7*	A
I_{DM}	Drain Current - Pulsed	(Note 1)	33	33*	A
V_{GSS}	Gate-Source Voltage		± 30		V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	340		mJ
I_{AR}	Avalanche Current	(Note 1)	11		A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	12.5		mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5		V/ns

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. I_{AS} = 5.5A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 11A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

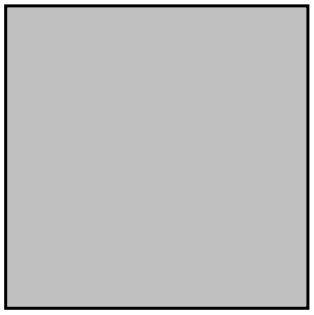
FAIRCHILD SEMICONDUCTOR

Die Size: Impact on Avalanche Rating

FDD26AN06A0
26 mΩ, I_{as} = 29A



FDD13AN06A0
13 mΩ, I_{as} = 50A



Increasing the die size:

- Reduces the $R_{DS(ON)}$
- Increases the cost
- Increases the size of the package needed
- Reduces the thermal resistance
- Increases the thermal capacitance
- Increases avalanche capability

Process design also contributes to increased robustness

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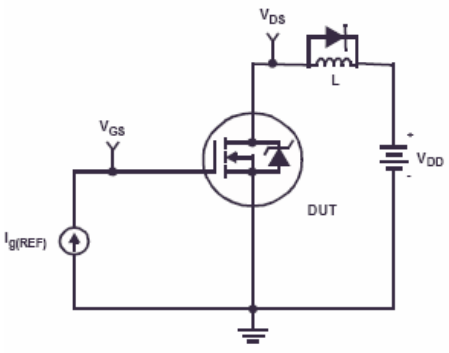
MOSFET Switching of Inductive Loads

- The MOSFET gate charge characteristics are defined and tested for inductive load switching
  - The current is initially set up to the desired test value using a similar approach to the avalanche test
  - The MOSFET is switched off
  - Then it is switched on and tested
- The MOSFET gate is driven with a constant current source



Gate Charge Test Circuit

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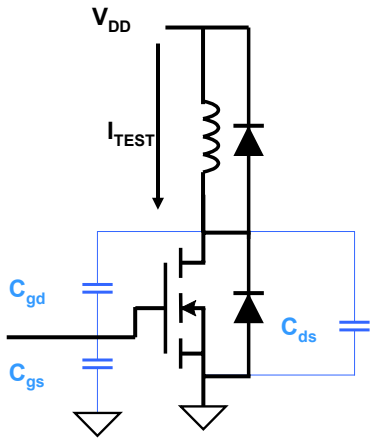
Internal Capacitances Affecting Losses

- The diagram shows the three capacitances that affect switching losses
- These capacitances cause energy losses in two ways:
  - C_{gd} and C_{gs} slow down the switching on of the MOSFET, which increases the switching losses
  - The energy loss from charging the capacitances back and forth during switching cycles



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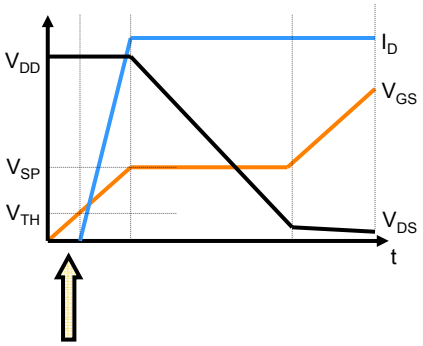
First Stage of Switching

- During the first stage of switching, nothing much happens
- The gate is charged up to the V_{TH} threshold
- Some energy, but not much is needed to charge C_{gs} and C_{gd} to this level



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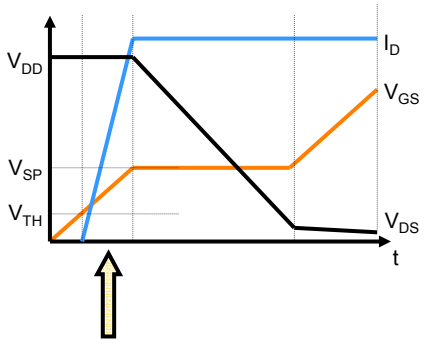
Second Stage of Switching

- When the gate voltage exceeds the threshold voltage, current starts to flow through the MOSFET
- The MOSFET is now working as follows:
  $I_D=gm(V_{GS}-V_{TH})$
- The gate voltage increases, which increases the drain current until the test current in the inductor is reached
- This happens at the voltage $V_{SP}=I_D/gm+V_{TH}$



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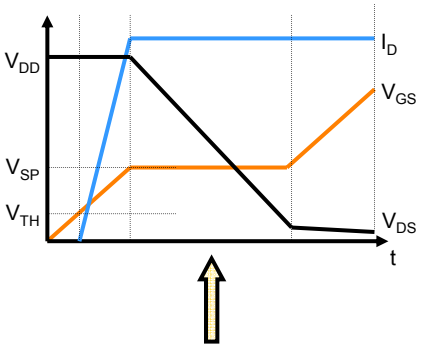
Third Stage of Switching

- The high drain voltage is now sustained only by the C_{gd} capacitance
- During the third stage, the capacitor is discharged
  - The energy in this capacitance is relatively small
  - But it slows down the voltage waveform and has a major effect on the switching losses



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Gate Loss Calculation

- Before we calculate the losses for the third stage, we will introduce the concept of charge, rather than capacitance
  - We note Q=CV and Q=It
- The stray capacitances C_{gd}, C_{gs} etc. are normally expressed as gate charges Q_{gd}, Q_{gs} etc.
  - This simplifies the loss calculation to

    Time to charge Q_{gd} = Q_{gd} / Gate drive current

Q: charge, C: capacitance, V:voltage, I: current, L: inductance, t: time

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Third Stage of Switching Example

- Take the datasheet test conditions as an example
  - I_D = 50A
  - V_{DD} = 40V
  - I_g = 1mA
- From datasheet
  - Q_{gd} = 7.2nC
  - Assume V_{SP} = 4V
- Energy loss in C_{gd} is
  - 0.5 x Q x V
  - 0.5 x 7.2nC x (40-4)V
  - Loss = 0.129mJ
- Time to charge Qgd is
  - t = Q_{gd}/I_g
  - t = 7.2nC/1mA = 7.2µs
- Power loss in third stage
  - P = average V x current
  - P = 0.5 x 40V x 50A
  - P = 1000W (for 7.2µs)
- Energy loss per cycle due to slower switching
  - 1000W x 7.2µs = 7.2mJ

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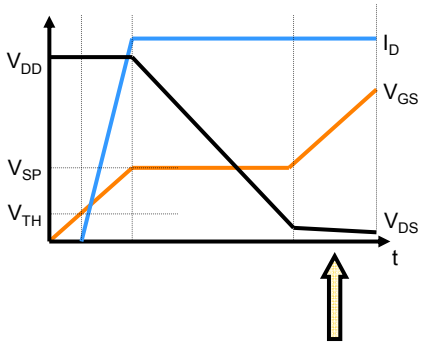
Final Stage of Switching

- The gate driver charges up the gate up until the maximum specified gate voltage
- All capacitances are charged up to their final value



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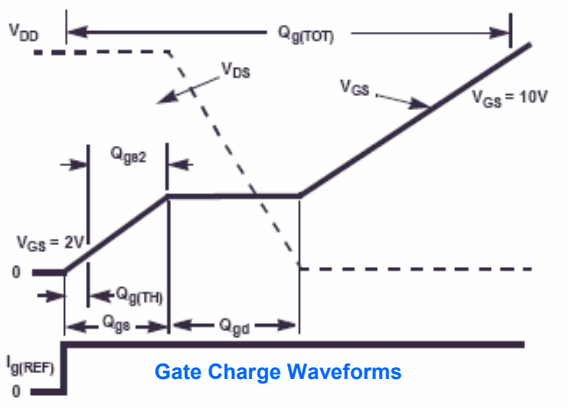
Gate Charge Elements for Medium Voltage MOSFETs



Gate Charge Waveforms

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Summary of Switching on Losses

- Stage 1: Charging up to V_{TH}
  - Small gate losses — No ramp up losses
- Stage 2: Current ramp up
  - Small gate losses — 5.7mJ loss in ramp up
- Stage 3: V_{DS} ramp down
  - Small gate losses — 7.2mJ loss in ramp up
- Stage 4: Final charging of gate
  - Small gate losses — No ramp up losses

- Total gate losses using $Q_{g(tot)}$ of 47nC
  - 0.5 x 47nC x 10V = 0.235 mJ

- **Total losses: 5.7mJ + 7.2mJ + 0.235mJ = 13.135 mJ**

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Total Switching Losses

- Up until now, we have considered the switch on losses
  - The switch off behavior is identical to the switch on behavior, only in reverse
- So the total switching losses are
  - Switch on losses + switch off losses
- The switching energy is converted to switching power loss by multiplying by frequency
  - $P_{sw} = (E_{on} + E_{off})$ x frequency
  - So for 200Hz switching:
  - P_{sw} = (13.1+13.1)mJ x 200Hz = 5.24W

$$P_{SW} = \left(\frac{V_{IN} \times I_{OUT}}{2}\right)(F_{SW})\left(\frac{Q_{GS2} + Q_{GD}}{I_{DRIVER(H-L)}} + \frac{Q_{GS2} + Q_{GD}}{I_{DRIVER(L-H)}}\right)$$

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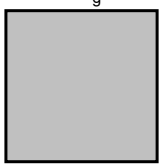
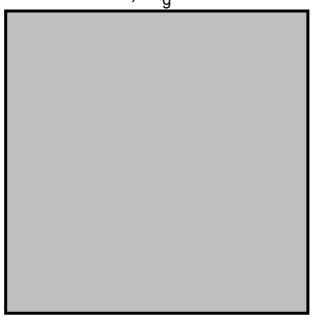
Die Size: Impact on Gate Charge

FDD26AN06A0
26 mΩ, Q_g = 17nC



FDD13AN06A0
13 mΩ, Q_g = 29nC



Increasing the die size:

- Reduces the $R_{DS(ON)}$
- Increases the cost
- Increases the size of the package needed
- Reduces the thermal resistance
- Increases the thermal capacitance
- Increases avalanche capability
- **Increases gate charge**

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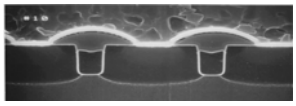
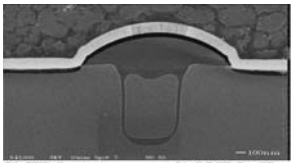
Technology Trends: Switching Losses

Trench

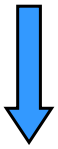


Reduce Q_g using thick bottom oxide

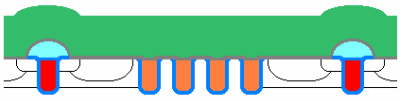
Trench – thick bottom oxide



Integrate Schottky diode into the MOSFET array



SyncFET technology



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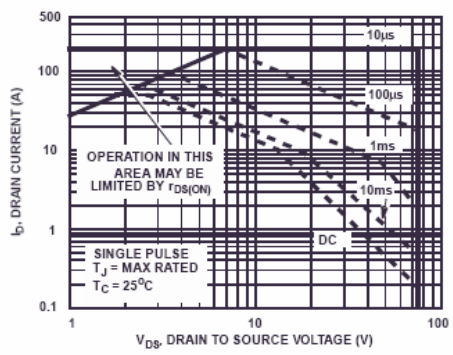
Safe Operating Area

- During switching (at the end of the second stage), we have a peak power dissipation of 2000W
  - V_{DS} = 50V
  - I_D = 40A
- The safe operating area plots shows which voltages and currents can be sustained for which time, if T_J max is not exceeded



Forward Bias Safe Operating Area

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Gate Oscillation Revisited

- Earlier we noted that gate oscillation can cause an overshoot on the gate, which could destroy the silicon
- A second problem with gate oscillation is that the maximum current and maximum voltage point of the safe-operating area will be crossed multiple times
  - This could destroy the part, or at best, greatly increase the switching losses

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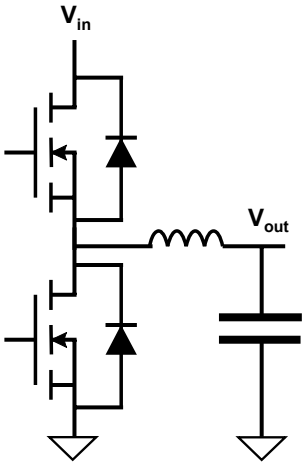
Synchronous Buck Topology

- Our session objective was to understand MOSFET selection for the synchronous buck topology
- The synchronous buck topology output stage is similar to a classical PWM output stage on a microcontroller followed by a filter
- The duty cycle D is controlled to give the right output voltage
  - In steady state D = V_{out} / V_{in}



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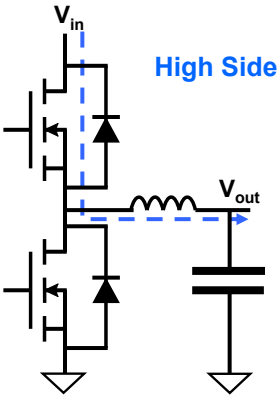
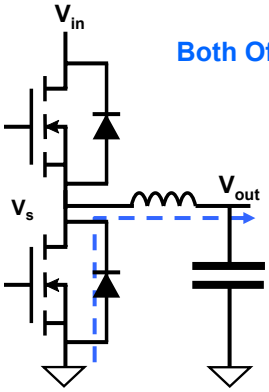
Synchronous Buck Topology



- In the steady state condition, consider the case with the high side device ON
- The low side device is OFF
- Current flows through the high side device into the inductor



- The high side device switches OFF
- As the low side device is OFF, the inductor current will be taken up by the low side diode
- The switching node voltage V_s is therefore NEGATIVE

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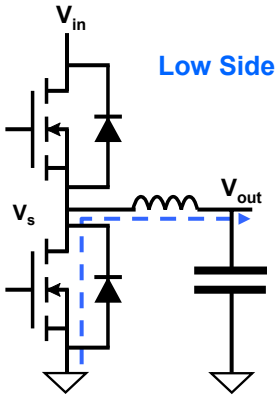
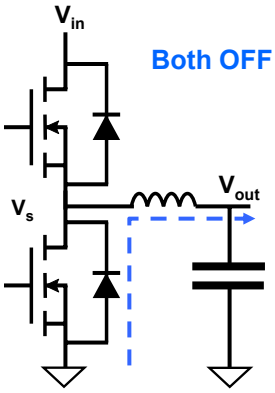
Synchronous Buck Topology



Low Side ON

- The low side device switches ON
- It is important to make sure that the high side switch is turned off to avoid cross-conduction (also called shoot through)
- Current flows upwards
- The switching node voltage V_s is still negative



Both OFF Again

- The low side device switches OFF
- As the high side device is OFF, the inductor current will be taken up by the low side diode
- The switching node voltage V_s is still NEGATIVE

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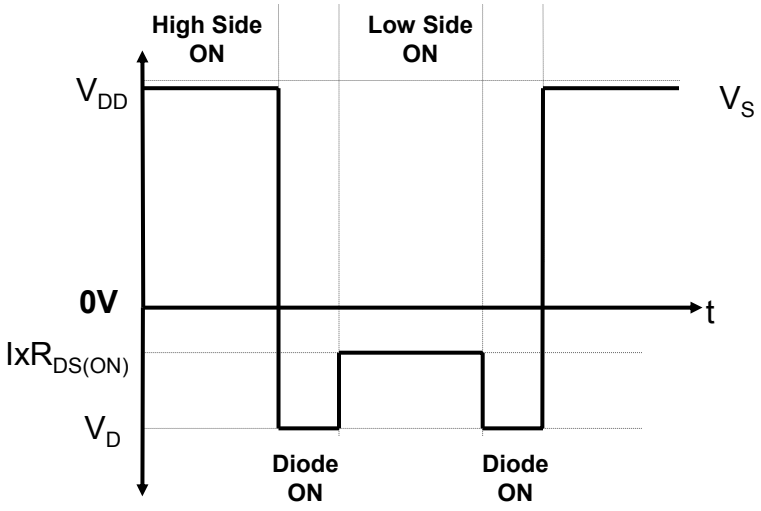
Voltage on V_S During Switching



The negative voltage scale has been exaggerated

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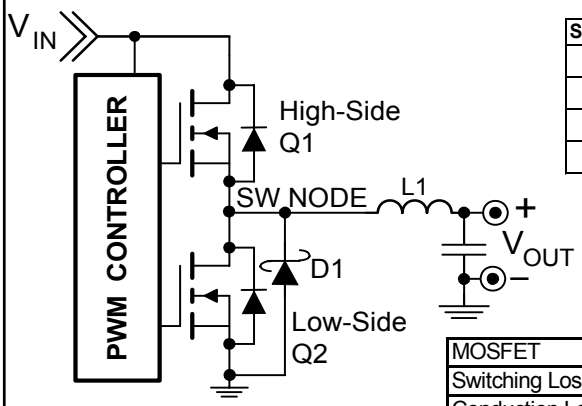
Synchronous Buck Switches

- Application presumed to be 12V input, 1.5V output
- The High Side switch will be ON for a short time as the duty cycle will be low
  - Switching losses per cycle will be high as the full current and the full input voltage need to be switched
  - Due to the low duty cycle, the conduction losses will be less dominant than for an equivalent Low Side switch
- The Low Side switch is ON for most of the time
  - Conduction losses will therefore dominate
  - Switching losses per cycle are lower as the full input current is switched at the diode voltage

Synchronous Buck Loss Summary



System Parameters		
V_{IN}	12	V
V_{OUT}	1.5	V
I_{OUT}	15	A
F_{SW}	300	kHz

	High-Side	Low-Side		
MOSFET	FDD6644	FDB6676	Total	
Switching Loss	1.09	0.31	**1.40**	W
Conduction Loss	0.21	1.15	**1.36**	W
Other Losses			**0.26**	W
Total Losses	**1.30**	**1.46**	**3.02**	W
Output Power			**22.5**	W
Efficiency			**88%**	

Selecting Power MOSFETs for Synchronous Buck Applications: Step 1

- Calculate the high side conduction loss per mΩ of $R_{DS(ON)}$:

$$P_{CONDHS} = I_{OUT}^{2} \times \frac{V_{OUT}}{V_{IN}} \times 10^{-3}$$

- and the switching loss per nC of gate charge:

$$P_{SWHS} = V_{IN} \times I_{OUT} \times F_{SW} \times \left(\frac{1}{I_{DRIVER}} \right) \times 10^{-9}$$

- Calculate the low side conduction loss per milliohm of $R_{DS(ON)}$:

$$P_{CONDLS} = \left(1 - \frac{V_{OUT}}{V_{IN}} \right) \times I_{OUT}^{2} \times 10^{-3}$$

- and approximate the switching loss per nC of gate charge:

$$P_{SWLS} \approx 1 \times I_{OUT} \times F_{SW} \times \left(\frac{1}{I_{DRIVER}} \right) \times 10^{-9}$$

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Selecting Power MOSFETs for Synchronous Buck Applications: Step 2

- We will consider two different examples to show how the operating conditions affect the MOSFET choice

Sync. Buck data input		
Vin	5	V
Vout	3.3	V
Iout	10	A
fsw	230000	Hz
Idrv	1.7	A

conduction loss per mOhm			
high side	0.06600	low side	0.03400
switching loss per nC.			
high side	0.00676	low side	0.00135

Sync. Buck data input		
Vin	12	V
Vout	1.2	V
Iout	20	A
fsw	300000	Hz
Idrv	1.7	A

conduction loss per mOhm			
high side	0.04000	low side	0.36000
switching loss per nC.			
high side	0.04235	low side	0.00353

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Selecting Power MOSFETs for Synchronous Buck Applications: Step 3

- Build a spreadsheet for the selected devices, calculate the loss. Select the MOSFET based on package, cost and loss data. Check the results in a more detailed calculation and lab test
- Use FDD8896 HS and LS for example 1
  - FDD8874 is slightly better for the low side, but we recommend using just one part type
- Use FDS6294 HS and FDD8870 LS for example 2
  - If no cooling area is allowed, use two FDD8870 devices

				Example 1 loss in W		Example 2 loss in W	
part		Rdson	Qg typ	HS1	LS1	HS2	LS2
FDD8870	DPAK	3.9	91	0.87	0.25	4.01	1.73
FDD8874	DPAK	5.1	54	0.70	0.25	2.49	2.03
FDD8896	DPAK	5.7	46	0.69	0.25	2.18	2.21
FDD8876	DPAK	8.2	34	0.77	0.32	1.77	3.07
FDD8880	DPAK	10	23	0.82	0.37	1.37	3.68
FDS6294	SO-8	11.3	10	0.81	0.40	0.88	4.10
FDD8878	DPAK	15	19	1.12	0.54	1.40	5.47

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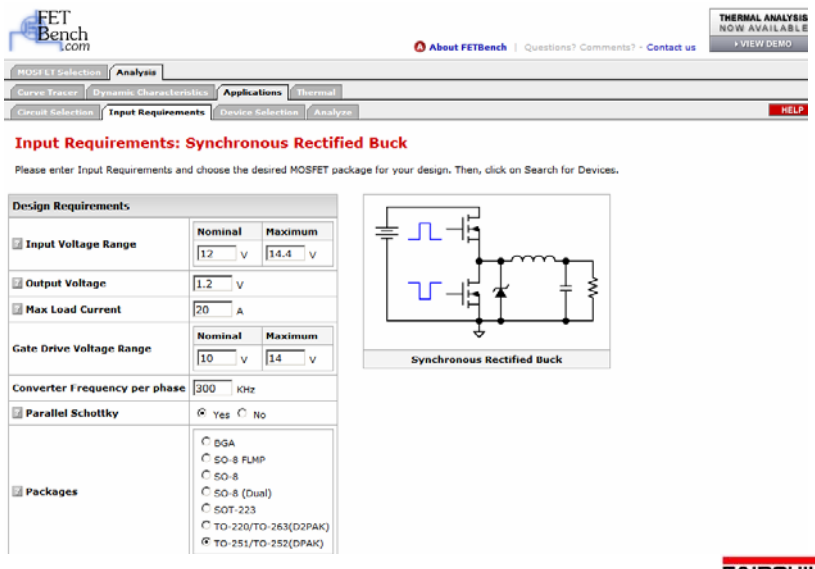
FETBench Based Selection



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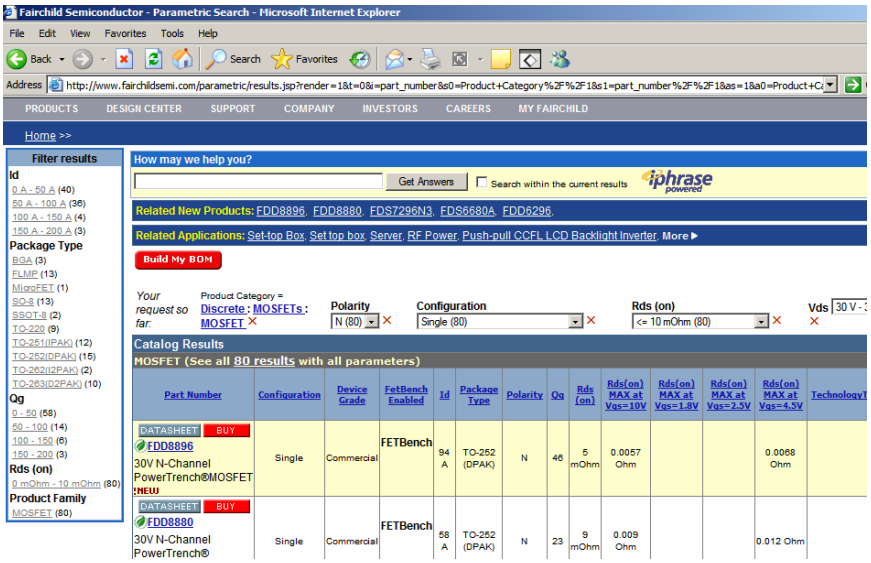
Parametric Search



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