8-Bit MCU
HR7P153

Datasheet

☐ **Brief**

☑ **Datasheet**

☐**Specifications**

SHANGHAI EASTSOFT MICROELECTRONICS Co., LTD

2017.12.08

Application Notes

Power On/Off Sequences

Eastsoft MCUs are designed with separate power pins. If a MCU is applied in a system which has multiple power supplies, the MCU should be powered on first, then other devices are involved in the system. Conversely, the MCU should be powered off after all other devices are powered off. Reversed steps may cause excessive voltage or current on the MCU internal components, which is likely to cause malfunction of MCU and weaken components performances. For details, please refer to the datasheet

Resets

Eastsoft MCUs provide an internal power-on reset circuit, which could possibly be invalid in different fast/slow power on/off systems. To ensure a proper reset function, the following reset modes are recommended: external reset, brown-out reset, watchdog reset, etc.. The triode reset circuit or the RC reset circuit is recommended when the external reset circuit is used for system design. Otherwise, it is suggested to connect the reset pin to power supply with a resistor or to use power-supply-jitter processing circuit or other protection circuits. For details, please refer to the datasheet.

Clocks

Eastsoft MCUs offer internal and external clock sources. The internal clock may produce some frequency offset due to unstable temperature or voltage, which may affect the accuracy of the clock source. When a ceramic or crystal oscillator circuit is used as an external clock source, it is suggested to enable the oscillator start-up timer delay. When a RC oscillator circuit is used, it is suggested to take account of the capacitor matching and resistor matching. When an external active oscillator or external clock input is used, the input high-voltage/low-voltage should be considered. For details, please refer to the datasheet

Initialization

For different application systems, it is necessary to initialize registers, memories and function modules, especially the multiplexed I/O pins, in order to avoid the unknown status of I/O pins when MCU is powered on.

Pins

Eastsoft MCUs are designed with wide-range input voltages. It is suggested that the input high-level voltage should be higher than V_{IHMIN}, the input low-level voltage should be lower than V_{ILMAX}. To avoid the noise influencing MCU, the input voltage should not be set between V_{IHMIN} and V_{ILMAX}. The unused I/O pins are suggested to be set to input mode, and should be connected to VDD via pull-up resistors or to GND via pull-down resistors. Alternatively, set unused pins to output mode with fixed voltage and leave them floating. The ways of handling the unused pin vary from application to application and it is important to follow the specific application specification and instructions.

ESD Protection

Eastsoft MCUs have industrial ESD standard protection circuits. It is suggested to take proper protection measures depending on application/storage environment to prevent MCUs from static electricity. Special attention should be paid to the humidity of application environment. Do not use the insulators which could cause static electricity. Use anti-static-electricity container/shields or conductive materials to store and transport the MCUs. Ground all the testing tools, measuring tools, including the workbench. Use anti-static-electricity belts or gloves, and do not touch the MCU with fingers directly.

EFT Protection

Eastsoft MCUs have industrial EFT standard protection circuits. When MCUs are used in PCB systems, the

related design requests should be satisfied, including wiring of VDD or GND (i.e. separation of digital/analog power supply, single-point/multi-point grounding and so on), protection circuits for reset pins, decoupling capacitors between VDD and GND, separate processing of high/low frequency circuits, selection of single-layer/multi-layer board and so on.

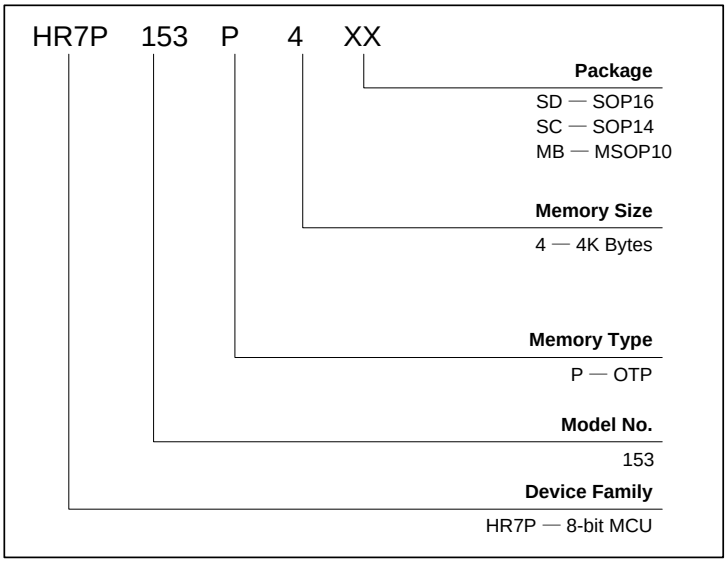
Development Environment

Eastsoft MCUs have a complete software/hardware development environment with protected intellectual property.. When using the development tools, such as assembler, compiler, burner and firmware emulator of Shanghai Eastsoft IC Co, Ltd. or by the appointed third party, please follow the related specifications and instructions.

Note: For any questions arising from product development, please contact us through the sales department or other ways.

Ordering Information

Part No.	OTP	SRAM	I/O	Timer	PWM	ADC	LVD	Package
HR7P153P4SD	2K Words	64B	13+1Input	8-bit X 2	2	12-bit x 6 ch	1	SOP16
HR7P153P4SC			11+1Input					SOP14
HR7P153P4MB			7+1Input			12-bit x 6 ch		MSOP10



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Revision History

Date	Summary
2017-12-8	Initial version, based on the HR7P153_Datasheet_c_v1.4

Note: Should you have any questions, please refer to the corresponding version of the HR7P153_Datasheet_C.

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  - Machine cycle: 2 system clock cycle
  - Reset vector is located at 000_H and interrupt vector is located at 004_H
  - Interrupt handler, 12 interrupt sources available
  - Maximum operating frequency
    - 2MHz (VDD=2.1~5.5V)
    - 20MHz (VDD=3.0~5.5V)
- Memories
  - 2K Words OTP program memory and 8-level program stack
  - 64 Bytes SRAM data memory
  - Direct addressing, relative addressing and look-up table read operation available in program memory
  - Direct address and indirect addressing available in data memory
- I/O Ports
  - Up to 13 ports and 1 input port
    - Port A (PA): PA0~PA7
    - Port B (PB): PB0~PB5
  - 4 external port interrupts
  - 1 external key interrupt KINT with up to 8 inputs available (KIN0~KIN7)
  - Independent configurable internal weak pull-up/down
    - Matching accuracy within ±3% at room temperature (VDD = 5V)
  - Configurable high drive ports
- Resets and Clock
  - Power-on reset POR
  - Brown-out reset BOR
  - Low voltage detection interrupt circuit
  - External reset
  - Independent hardware watchdog timer
    - WDT period register
  - Internal high frequency 16MHz RC oscillator clock source
    - Internal programmable frequency division, down to 32KHz
    - Factory calibration accuracy±2% (at room temperature 25℃)

- ◇ Internal low frequency 32KHz RC oscillator clock source (clocking WDT, and can be configured as the system clock source)
- ◇ External oscillator clock source
  - Clock frequency: 32KHz~20MHz
- ◇ System clock switching between high and low speed

◆ Peripherals

- ◇ 2x 8-bit PWM time-based timer T8P1/T8P2
  - Timer mode
  - Configurable prescaler and postscaler
  - Programmable reload counter value
  - Up to 9-bit resolution of PWM output
  - PWM complementary outputs with software configurable dead-band time
  - Interrupt capability
- ◇ Analog-to digital converter ADC
  - 12-bit resolution
  - 6 analog channel inputs available
  - Supply voltage detection with voltage division options
  - External reference source
  - Internal reference sources (VDD/4V/3V/2.1V)
  - Interrupt capability

◆ Low Power Consumption

- ◇ IDLE current
  - 3uA (typical) @5.0V, BOR/WDT enabled, 25℃
- ◇ Dynamic current
  - 20uA (typical) @32KHz, 3.0V, 25℃
  - 2mA (typical)@16MHz,5.0V,25℃

◆ Programming and Debug Interface

- ◇ In-system programming ISP interface
- ◇ Encrypted programming code

◆ Design and Technology

- ◇ Low consumption, high speed OTP CMOS technology
- ◇ MSOP10 package
- ◇ SOP14/SOP16 packages

◆ Operating Conditions

- ◇ Operating voltage: 2.1V ~ 5.5V
- ◇ Operating temperature: -40 ~ 85℃

1. 2 Application Fields

The HR7P153 is an ideal solution for mobile power banks, digital panel meters , small home appliances and etc. .

1. 3 Block Diagram

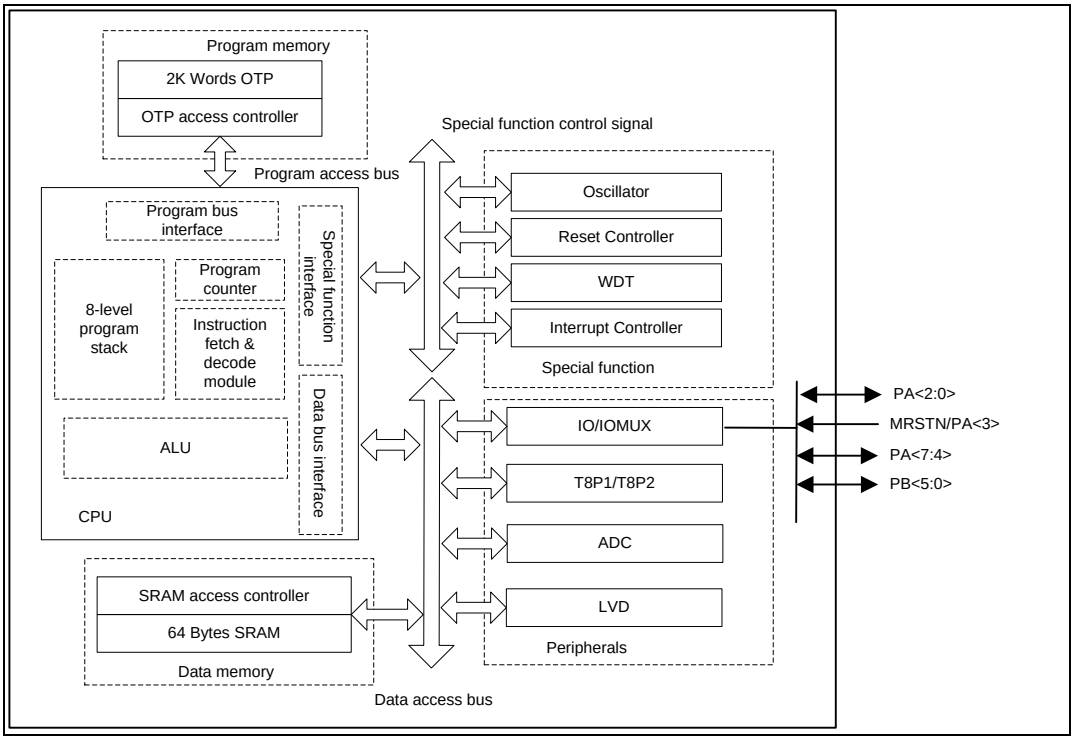


Figure 1-1 HR7P153 Block Diagram

1. 4 Pin Diagrams

1. 4. 1 SOP16

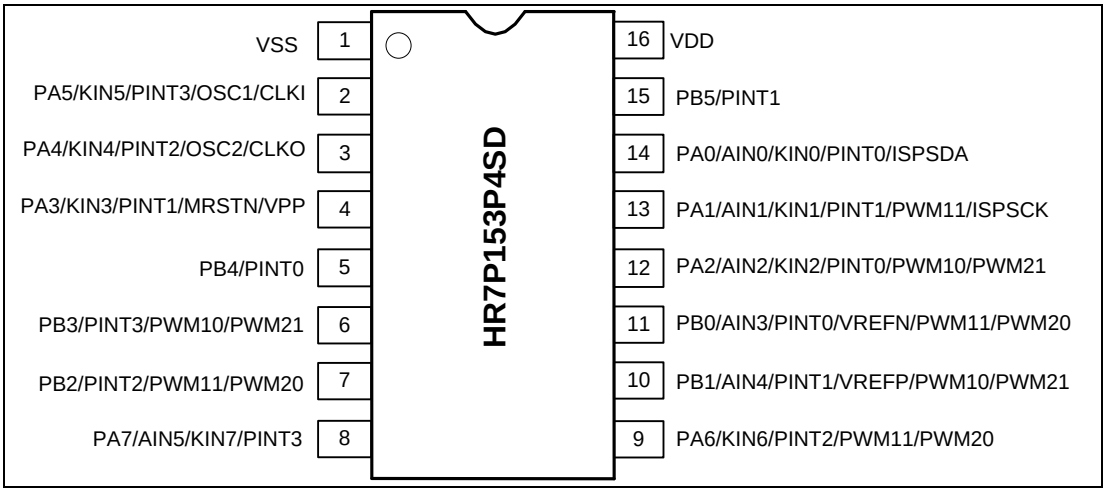


Figure 1-2 SOP16 Package Top View

1. 4. 2 SOP14

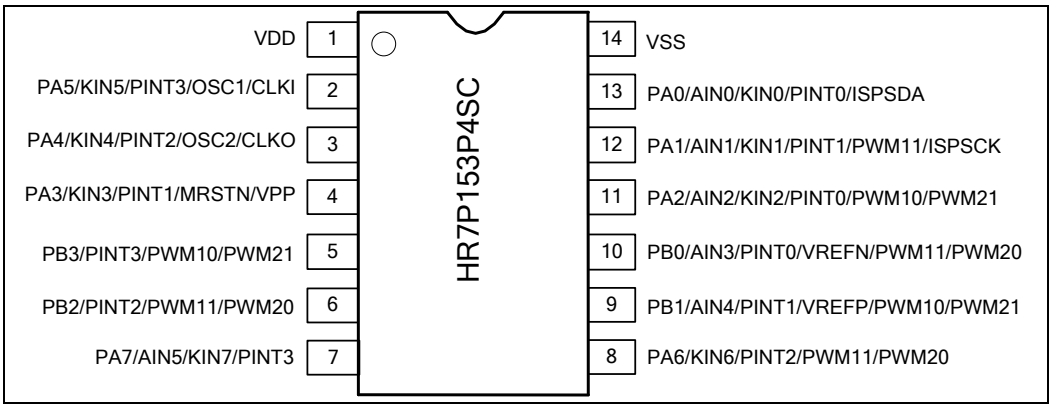


Figure 1-3 SOP14 Package Top View

1. 4. 3 MSOP10

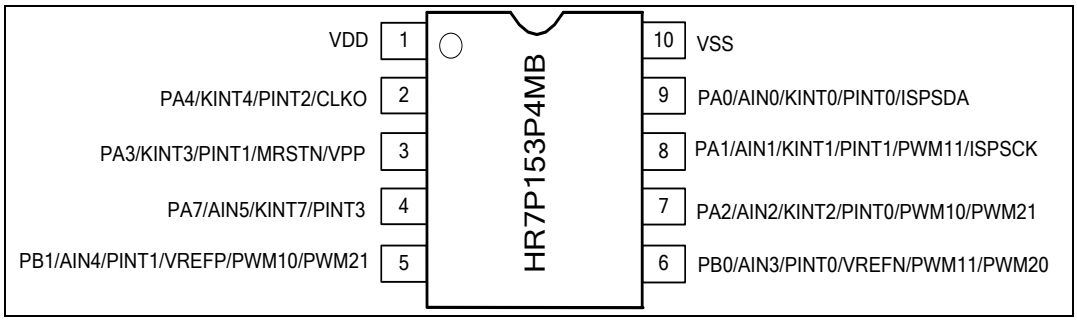


Figure 1-4 MSOP10 Package Top View

Note1: MRSTN is active low.

Note2: For some packages, if the number of packaged pins are less than the maximum number of pins, the unpackaged pins and unused pins should be set to output low; otherwise it might lead to irregular power consumption and the stability of the device performance might also be affected.

Note3: The user must ensure the VPP voltage is less than the power supply VDD; otherwise it might lead to irregular behaviors of the device. If voltage overshoot occurs on the VPP pin, the pulse voltage must be limited not more than VDD+0.5V and the pulse width must be not more than 100us.

1. 5 Pin Descriptions

1. 5. 1 Pin Allocation

Pin Name	HR7P153		
	SOP16	SOP14	MSOP10
PA0/AIN0/KIN0/PINT0/ISPSDA	14	13	9
PA1/AIN1/KIN1/PINT1/PWM11/ISPSCK	13	12	8
PA2/AIN2/KIN2/PINT0/PWM10/PWM21	12	11	7
PA3/KIN3/PINT1/MRSTN/VPP	4	4	3
PA4/KIN4/PINT2/OSC2/CLKO	3	3	2
PA5/KIN5/PINT3/OSC1/CLKI	2	2	—
PA6/KIN6/PINT2/PWM11/PWM20	9	8	—
PA7/AIN5/KIN7/PINT3	8	7	4
PB0/AIN3/PINT0/VREFN/PWM11/PWM20	11	10	6
PB1/AIN4/PINT1/VREFP/PWM10/PWM21	10	9	5
PB2/PINT2/PWM11/PWM20	7	6	—
PB3/PINT3/PWM10/PWM21	6	5	—
PB4/PINT0	5	—	—
PB5/PINT1	15	—	—
VDD	16	1	1
VSS	1	14	10

Table 1-1 Pin Allocation

1. 5. 2 Pin Multiplexing Descriptions

Pin Name	Multiplexing	Input Type	Output Type	A/D	Description	Remarks
PA0/AIN0/KIN0/PINT0/ ISPSDA	PA0	TTL	CMOS	D	GPIO	Individually enabled weak pull-up/down
	AIN0	—	—	A	ADC analog channel 0	
	KIN0	TTL	—	D	External key interrupt input 0	
	PINT0	TTL	—	D	External port interrupt input 0	
	ISPSDA	TTL	CMOS	D	Serial programming data in and out	
PA1/AIN1/KIN1/PINT1/ PWM11/ISPSCK	PA1	TTL	CMOS	D	GPIO	Individually enabled weak pull-up/down
	AIN1	—	—	A	ADC analog channel 1	
	KIN1	TTL	—	D	External key interrupt inpu1	
	PINT1	TTL	—	D	External port interrupt input 1	
	PWM11	—	CMOS	D	T8P1 PWM output	
	ISPSCK	TTL	—	D	Serial programming clock input	
PA2/AIN2/KIN2/PINT0/ PWM10/PWM21	PA2	TTL	CMOS	D	GPIO	Individually enabled weak pull-up/down
	AIN2	—	—	A	ADC analog channel 2	
	KIN2	TTL	—	D	External key interrupt input 2	
	PINT0	TTL	—	D	External port interrupt input 0	
	PWM10	—	CMOS	D	T8P1 PWM complementary output	
	PWM21	—	CMOS	D	T8P2 PWM output	
PA3/KIN3/PINT1/ MRSTN/VPP	PA3	TTL	CMOS	D	General-purpose input	Individually enabled weak pull-up
	KIN3	TTL	—	D	External key interrupt input 3	
	PINT1	TTL	—	D	External port interrupt input 1	
	MRSTN	TTL	—	D	Main reset input	
	VPP	Power	—	—	OTP programming voltage	
PA4/KIN4/PINT2/ OSC2/CLKO	PA4	TTL	CMOS	D	GPIO	Individually enabled weak pull-up/down
	KIN4	TTL	—	D	External key interrupt input 4	
	PINT2	TTL	—	D	External port interrupt input 2	
	OSC2	—	CMOS	A	Crystal oscillator /resonator output	
	CLKO	—	CMOS	D	Fosc/16 output	
PA5/KIN5/PINT3/ OSC1/CLKI	PA5	TTL	CMOS	D	GPIO	Individually enabled weak
	KIN5	TTL	—	D	External key interrupt	

Pin Name	Multiplexing	Input Type	Output Type	A/D	Description	Remarks
					input 5	pull-up/down
	PINT3	TTL	—	D	External port interrupt input 3	
	OSC1	TTL	—	A	Crystal oscillator /resonator input	
	CLKI	TTL	—	A/D	Clock input	
PA6/KIN6/PINT2/ PWM11/PWM20	PA6	TTL	CMOS	D	GPIO	Individually enabled weak pull-up/down
	KIN6	TTL	—	D	External key interrupt input 6	
	PINT2	TTL	—	D	External port interrupt input 2	
	PWM11	—	CMOS	D	T8P1 PWM output	
	PWM20	—	CMOS	D	T8P2 PWM complementary output	
PA7/AIN5/KIN7/PINT3*	PA7	TTL	CMOS	D	GPIO	Individually enabled weak pull-up/down
	AIN5	—	—	A	ADC analog channel 5	
	KIN7	TTL	—	D	External key interrupt input 7	
	PINT3	TTL	—	D	External port interrupt input 3	
PB0/AIN3/PINT0/ VREFN/ PWM11/ PWM20	PB0	TTL	CMOS	D	GPIO	Individually enabled weak pull-up/down
	AIN3	—	—	A	ADC analog channel 3	
	PINT0	TTL	—	D	External port interrupt input 0	
	VREFN	—	—	A	ADC external reference negative port	
	PWM11	—	CMOS	D	T8P1 PWM output	
	PWM20	—	CMOS	D	T8P2 PWM complementary output	
PB1/AIN4/PINT1/ VREFP/PWM10/ PWM21*	PB1	TTL	CMOS	D	GPIO	Individually enabled weak pull-up/down
	AIN4	—	—	A	ADC analog channel 4	
	PINT1	TTL	—	D	External port interrupt input 1	
	VREFP	—	—	A	ADC external reference positive port	
	PWM10	—	CMOS	D	T8P1 PWM complementary output	
	PWM21	—	CMOS	D	T8P2 PWM output	
PB2/PINT2/PWM11/ PWM20	PB2	TTL	CMOS	D	GPIO	Individually enabled weak pull-up/down
	PINT2	TTL	—	D	External port interrupt input 2	
	PWM11	—	CMOS	D	T8P1 PWM output	
	PWM20	—	CMOS	D	T8P2 PWM	

Pin Name	Multiplexing	Input Type	Output Type	A/D	Description	Remarks
					complementary output	
PB3/PINT3/PWM10/ PWM21	PB3	TTL	CMOS	D	GPIO	Individually enabled weak pull-up/down
	PINT3	TTL	—	D	External port interrupt input 3	
	PWM10	—	CMOS	D	T8P1 PWM complementary output	
	PWM21	—	CMOS	D	T8P2 PWM output	
PB4/PINT0	PB4	TTL	CMOS	D	GPIO	Individually enabled weak pull-up/down
	PINT0	TTL	—	D	External port interrupt input 0	
PB5/PINT1	PB5	TTL	CMOS	D	GPIO	Individually enabled weak pull-up/down
	PINT1	TTL	—	D	External port interrupt input 1	
VDD	VDD	Power	—	—	Power supply	—
VSS	VSS	Power	—	—	Ground (0V)	—

Table 1-2 Pin Multiplexing Descriptions

Note1: A = Analog, D = Digital, MRSTN is active low.
Note2: Except for PA3 which is a TTL input, all other GPIOs are TTL Schmitt input and CMOS output.
Note3: The PWM output and complementary output pins of T8P1 and T8P2 are configurable.

Chapter2 CPU Core

2. 1 CPU Overview

◇ Core features

- High performance Harvard architecture RISC CPU
- 79 RISC
- System clock operating frequency up to 20MHz
- Machine cycle = 2 system clock cycles
- Interrupt handler, 12 interrupt sources available

2. 2 System Clock and Machine Cycle

The system clock Fosc of the device can operate up to 20MHz. With two system clock cycles as inputs, the on-chip clock generator produces two non-overlapping orthogonal clocks termed as phase1 (p1) and phase2 (p2), which compose one machine cycle. If the system clock operates at 4MHz, one machine cycle is 500ns.

2. 3 Instruction Set Overview

The device uses 79 RISC instructions of HR7P series.

Most of the instructions are executed within a single (machine) cycle, except the instructions of some conditional jumps and program control operations, whose executions take two (machine) cycles. A single machine cycle is 500ns if the system clock frequency is 4 MHz.

For details, please refer to Appendix 1 Instruction Set.

2. 4 Special Function Registers

The CPU related registers include 11-bit program counter registers PCRL/PCRH, program status word register PSW and accumulator A register AREG. The program status register PSW stores status flags, including program stack overflow/underflow, negative flag, overflow flag, zero flag, half carry/borrow bit and carry/borrow bit.

PSW: Program Status Word Register								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	—	UF	OF	N	OV	Z	DC	C
R/W	—	R	R	R/W	R/W	R/W	R/W	R/W
POR	x	0	0	x	x	x	x	x

"x": Unknown

Bit 7 Not in used

Bit 6 UF: Pop underflow flag bit
0: No underflow
1: Underflow occurred

Bit 5 OF: Push overflow flag bit

0: No overflow
1: Overflow occurred

Bit 4 N: Negative flag bit
0: The result of a signed arithmetical or logical operation is positive
1: The result of a signed arithmetical or logical operation is negative

Bit 3 OV: Overflow flag bit
0: No overflow in signed arithmetical operations
1: Overflow occurred

Bit 2 Z: Zero flag bit
0: The result of an arithmetical or logical operation is non zero.
1: The result of an arithmetical or logical operation is zero.

Bit 1 DC: Half carry or half borrow bit
0: No carry or one borrow on lower 4 bits
1: One carry or no borrow on lower 4 bits

Bit 0 C: Carry or borrow bit
0: No carry or one borrow
1: One carry or no borrow

Note1: Only the following instructions can be written to the PSW register, including JDEC, JINC, SWAP, BCC, BSS, BTT, MOVA and SETR. Other instructions can only affect corresponding flags depending on the operation results.

Note2: OF and UF are read-only, and can only be cleared by power on reset, reset instruction and MRSTN reset. Other reset operations do not affect OF or UF.

AREG: Accumulator Register								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	AREG<7:0>							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	x	x	x	x	x	x	x	x

"x": Unknown

Bit 7~0 AREG<7:0>: the value of accumulator

PCRL: Program Counter Register Low Byte								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	PCR<7:0>							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 PCR<7:0>: program counter low byte

PCRH: Program Counter Register High Byte								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	—	—	—	—	—	PCR<10:8>		
R/W	—	—	—	—	—	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~3 Not in used

Bit 2~0 PCR<10:8>: program counter high 3 bits

Chapter3 Memories

3. 1 Overview

The MCU employs Harvard bus architecture, by which the program addressing space and data addressing space are independent of each other.

On-chip memories include:

- ◇ 2K words OTP program memory
- ◇ 64 bytes SRAM

The OTP program memory is mapped to program addressing space while the SRAM is mapped to data addressing space.

3. 2 Program Memory

3. 2. 1 Overview

The 2K words OTP program memory stores the user program and has a program addressing space from 000_H~$7FF_H$, where the space from $7E0_H$~$7FF_H$ is reserved. Each access address has a corresponding 16-bit wide memory location. The 11-bit program counter PC is used for program addressing.

The reset vector is at 000_H and the interrupt vector is at 004_H. An 8-level hardware stack is supported.

3. 2. 2 Program Address Mapping

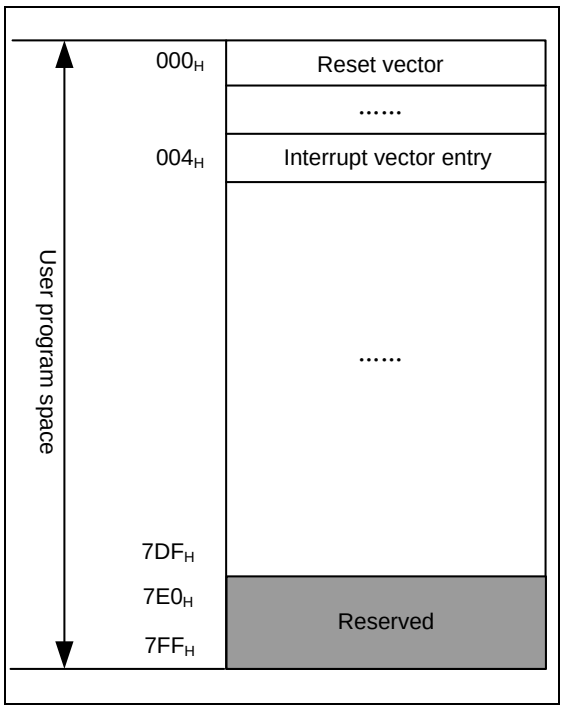


Figure 3-1 Program Address Mapping

3. 2. 3 Program Counter (PC)

The program counter stores the address of the very next instruction to be executed, and automatically increments after each instruction cycle unless the PC value is modified by instructions or interrupts. The 11-bit program counter PC<10:0> is not readable or writeable and has no physical address. It is capable of addressing the 2K word program memory space from 000_H ~ $7FF_H$ and accessing an address outside the range will make the PC to restart from 000_H. The PC<7:0> can be read or written by reading or writing the PCRL register while the PC<10:8> is indirectly assigned a value through the PCRH register using instructions such as RCALL, CALL and GOTO etc.

On a device reset, the PCRL, PCRH and PC will be cleared. The hardware stack operation does not affect the PCRH value.

How the PC value is affected by different instructions.

1. When directly modifying the PC value through instructions, if the PCRL is the destination register, it can be directly modified by PC<7:0>=PCRL<7:0>; at the same time, it will execute PC<10:8>=PCRH<2:0>. Thus, when modifying the PC value, the PCRH<2:0> should be modified first then PCRL<7:0>.
2. When executing a RCALL instruction, PC<7:0> is the value of register R and PC<10:8>=PCRH<2:0>
3. When executing a CALL and GOTO instruction, the PC<10:0> is the 11-bit immediate I (operand) of the instruction
4. The LCALL instruction is a double-word instruction, which has a 16-bit immediate (operand). PC<10:0> will be modified to the lower 11 bits of the 16-bit immediate and PCRH<2:0> will be modified to the value of I<10:8>
5. The AJMP instruction is also a double-word instruction, which has a 16-bit immediate. PC<10:0> will be modified to the lower 11 bits of the 16-bit immediate and PCRH<2:0> will be modified to I<10:8>.
6. When executing PAGE instruction, PCRH<7:3> will be replaced with the immediate of the instruction. (Due to that the program memory has a capacity of 2K words, the PCRH<7:3> are fixed to all 0s. The PC value will not be influenced by a PAGE instruction.
7. When executing other instructions, the PC value will automatically increase by 1.

Application example: an instruction application program for the PCRL being the destination register

```
……
MOVI    pageaddr
MOVA    PCRH        ; Set page address for the table
MOVI    tableaddr   ; Set offset to register A
CALL    TABLE       ; Call subroutine for table operation
……
TABLE:
ADD     PCRL, F     ; Add offset to PC to specify the accessed address
RETIA   0X01
RETIA   0X02
RETIA   0X03
……
```

3. 2. 4 Program Stack

The on-chip 8-level hardware stack has the same bit width as PC and it is used for the push and pop instruction. When the CALL, LCALL and RCALL instruction are being executed or interrupts are being serviced, the PC is automatically pushed. When the RET, RETIA or RETIE is being executed, the stack restores the most recent pushed value to the PC.

The 8-level program stack only supports 8-level buffering. This means that the stack only holds the 8 recent pushed values and the 9th push overwrites the 1st push. Likewise, the 9th pop may cause the program flow out of control. After a device reset, the stack pointer points to the top of the stack.

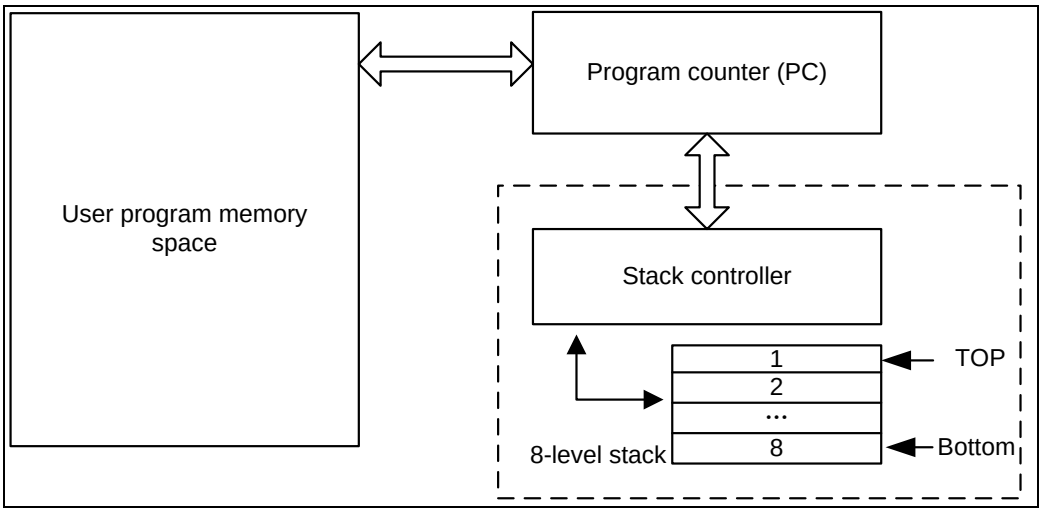


Figure 3-2 Stack Diagram

3. 3 IAP Accessing OTP Operations

3. 3. 1 OTP Memory

The OTP memory is a one-time programmable memory. The unprogrammed OTP memory location can be software programmed through an IAP operation when a high voltage 8.45V is applied to the VPP pin. The IAP operation writes in word and addresses through the FRA (FRAH:FRAL). During IAP writing the OTP memory, the CPU core is halted while the peripherals continue running. When the IAP finishes writing, the CPU core resumes operating.

3. 3. 2 Look-up Table Instruction

The HR7P 79 instruction set contains 8 look-up table instructions.

The look-up table read instructions read the word of the OPT memory location specified by the FRA (FRAH:FRAL) into the ROMD (ROMDH:ROMDL).

TBR
TBR#1

TBR_1
TBR1#

Look-up table write instructions are reserved.

TBW
TBW#1
TBW_1
TBW1#

See Appendix 1 Instruction Set for detailed operations.

3. 3. 3 In Application Programming IAP

An IAP operation writes to the OTP memory location specified by the FRA (FRAH: FRAL) with the content of the ROMD (ROMDH: ROMDL) through the IAPC register. The IAP operation is capable of accessing the address space from 200_H~$7DF_H$. It is considered good programming practice to verify that program memory writes agree with the intended value. Do not proceed with the programming until the readouts agree with the intended value. A single address programming takes at least 2ms.

Application example 1: IAP operation

```
MOVI    0x02            ; Write 55AA_H to 0210_H in OTP memory
MOVA    FRAH
MOVI    0x10
MOVA    FRAL
MOVI    0xAA
MOVA    ROMDL
MOVI    0x55
MOVA    ROMDH
BSS     IAPC, IAPEN     ; Enable IAP operation
BSS     IAPC, IAPGO     ; Trigger IAP operation
WAIT:
JBC      IAPC, IAPGO
        GOTO    WAIT
        ......
```

Application example 2:IAP look-up table read operation

```
MOVI    0x02            ;Read from 0210_H in data memory
MOVA    FRAH
MOVI    0X10
MOVA    FRAL
TBR                     ;Read data to ROMDH/L using look-up table read instruction
MOV     ROMDH, 0
… …
MOV     ROMDL, 0
… …
```

3. 3. 4 Special Function Registers

FRAL: Look-Up Table Address Low Byte								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FRA<7:0>							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	x	x	x	x	x	x	x	x

"x": Unknown

Bit 7~0 FRA<7:0>: look-up table address low byte

FRAH: Look-Up Table Address High Byte								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	FRA<15:8>							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	x	x	x	x	x	x	x	x

"x": Unknown

Bit 7~0 FRA<15:8>: look-up table address high byte

ROMDL: Look-Up Table Data Low Byte								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	ROMD<7:0>							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	x	x	x	x	x	x	x	x

"x": Unknown

Bit 7~0 ROMD<7:0>: look-up table data low byte

ROMDH: Look-Up Table Data High Byte								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	ROMD<15:8>							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	x	x	x	x	x	x	x	x

"x": Unknown

Bit 7~0 ROMD<15:8>: look-up table data high byte

IAPC:IAP Control Register								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	IAPEN	—	—	—	—	—	IAPGO	—
R/W	R/W	—	—	—	—	—	R/W	—
POR	0	0	0	0	0	0	0	0

"x": Unknown

Bit 7 IAPEN: IAP enable bit
0: Disabled
1: Enabled (only valid when VPP is input with a high voltage)

Bit 6~2	Not in used
Bit 1	IAPGO: IAP go bit 0: IAP operation not started or complete 1: Start IAP operation (start IAP operation by software writing 1; automatically cleared on completion of the operation) (only valid when VPP is input with a high voltage)
Bit 0	Not in used

3. 4 Data Memory

3. 4. 1 Overview

◇ The data memory consisting of

- General Purpose Register GPR
- Special Function Register SFR

◇ General Purpose Register GPR

- Total 1 memory section
- 64 bytes, address range from 0000_H through $003F_H$

◇ Special Function Register SFR

- 128 special function registers
- Address range from $FF80_H$ through $FFFF_H$

◇ Addressing modes

- Direct addressing
- Indirect addressing

3. 4. 2 Data Address Mapping

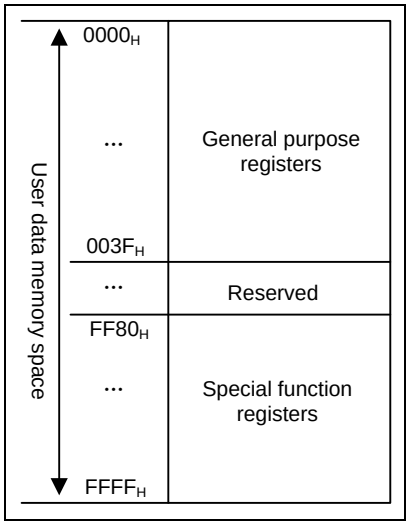


Figure 3-3 Data Address Mapping

3. 4. 3 General Purpose Registers (GPR)

General purpose registers store the data and control information for a short term, and are readable and writeable under program control. The GPR space has a size of 64 bytes, capable of addressing from 0000_H through $003F_H$. The content of the GPR is unknown following a power-on reset; however, the GPR will maintain its content after any other resets (no power outage occurred)

3. 4. 4 Special Function Registers

Special function registers control and configure the operations to the peripherals. There are total 128 special function registers in the address range from $FF80_H$ through $FFFF_H$. Most of the SFRs are readable and writeable, and only a few are reserved. See the

corresponding chapter for detailed description.

$FF80_H$	IAD	$FFA0_H$	INTG	$FFC0_H$	T8P1PEX
$FF81_H$	IAAL	$FFA1_H$	LVDC	$FFC1_H$	T8P2PEX
$FF82_H$	IAAH	$FFA2_H$	INTF1	$FFC2_H$	—
$FF83_H$	—	$FFA3_H$	INTE1	$FFC3_H$	—
$FF84_H$	PSW	$FFA4_H$	INTC1	$FFC4_H$	—
$FF85_H$	AREG	$FFA5_H$	OSCCAL	$FFC5_H$	—
$FF86_H$	IAPC	$FFA6_H$	WDTCAL	$FFC6_H$	ADCCL
$FF87_H$	FRAL	$FFA7_H$	PWRC	$FFC7_H$	ADCCH
$FF88_H$	FRAH	$FFA8_H$	OSCC	$FFC8_H$	ADCRL
$FF89_H$	ROMDL	$FFA9_H$	WKDC	$FFC9_H$	ADCRH
$FF8A_H$	ROMDH	$FFAA_H$	OSCP	$FFCA_H$	ADCTR
$FF8B_H$	PCRL	$FFAB_H$	WDTC	$FFCB_H$	—
$FF8C_H$	PCRH	$FFAC_H$	PWEN	$FFCC_H$	—
$FF8D_H$	—	$FFAD_H$	—	$FFCD_H$	—
$FF8E_H$	PA	$FFAE_H$	—	$FFCE_H$	—
$FF8F_H$	PAT	$FFAF_H$	—	$FFCF_H$	CALPROT
$FF90_H$	PB	$FFB0_H$	WDTP	$FFD0_H$	—
$FF91_H$	PBT	$FFB1_H$	—	$FFD1_H$	—
$FF92_H$	—	$FFB2_H$	T8P1	$FFD2_H$	—
$FF93_H$	—	$FFB3_H$	T8P1C	$FFD3_H$	—
$FF94_H$	N_PAD	$FFB4_H$	T8P1P	$FFD4_H$	—
$FF95_H$	N_PBD	$FFB5_H$	T8P1R	$FFD5_H$	—
$FF96_H$	N_PAU	$FFB6_H$	T8P1PMC	.....	.....
$FF97_H$	N_PBU	$FFB7_H$	T8P1OC		
$FF98_H$	—	$FFB8_H$	T8P2	$FFF8_H$	—
$FF99_H$	—	$FFB9_H$	T8P2C	$FFF9_H$	—
$FF9A_H$	—	$FFBA_H$	T8P2P	$FFFA_H$	—
$FF9B_H$	PINTS	$FFBB_H$	T8P2R	$FFFB_H$	—
$FF9C_H$	ANS	$FFBC_H$	T8P2PMC	$FFFC_H$	—
$FF9D_H$	INTF0	$FFBD_H$	T8P2OC	$FFFD_H$	—
$FF9E_H$	INTE0	$FFBE_H$	T8P1PDT	$FFFE_H$	—
$FF9F_H$	INTC0	$FFBF_H$	T8P2PDT	$FFFF_H$	—

Note: “— “ is reserved.

Figure 3-4 Special Function Register Space

3. 4. 5 Addressing Modes

The SRAM data memory supports two addressing modes: direct addressing and indirect addressing.

3. 4. 5. 1 Direct Addressing

In the direct addressing mode, the 8-bit address information of an instruction is used to address the GPR and SFR. If the 8-bit address information R<7:0> is less than 80_H, the GPR map is directly addressed. If the R<7:0> is greater than or equal to 80_H, the SFR map is then directly addressed.

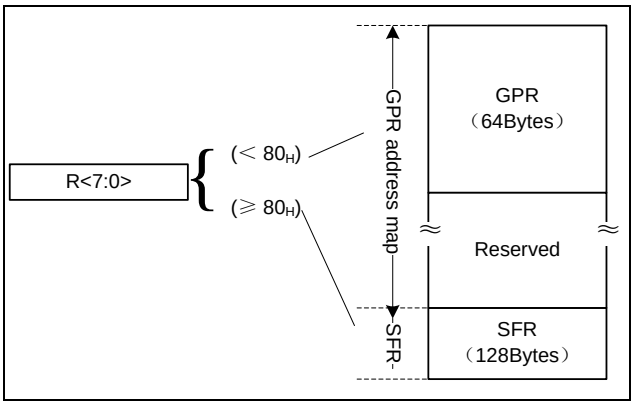


Figure 3-5 Direct Addressing Diagram

3. 4. 5. 2 Indirect Addressing

The indirect addressing involves a 16-bit indirect addressing address register IAA (IAAH and IAAL) and a virtual 8-bit indirect addressing data register IAD, and is capable of addressing from 0000_H~ $FFFF_H$. Store the destination address onto the IAA and read/write the IAD with instructions. Any instruction that accesses the IAD register actually accesses the destination register at the address specified by the IAA.

Due to that the IAD itself is mapped to the address $FF80_H$ of the data memory, when the IAA stores the address value $FF80_H$, reading/writing the IAD is equivalent to access the IAD itself using indirect addressing. In this case, the readout is always 00_H and a write operation is considered as a NOP (status bits may be effected).

The ISTEP instruction is used to calculate the offset for the 16-bit register IAA (IAAH:IAAL). On executing this instruction, augment the signed 8-bit immediate value of the ISETP instruction to a signed 16-bit value, which is then added to the IAA value and the result is saved back to the IAA register. The ISTEP instruction can result in an offset range -128~127. The ISTEP instruction is a 16-bit calculation although there is only one 8-bit immediate value. The result of calculation is stored on IAAL and IAAH.

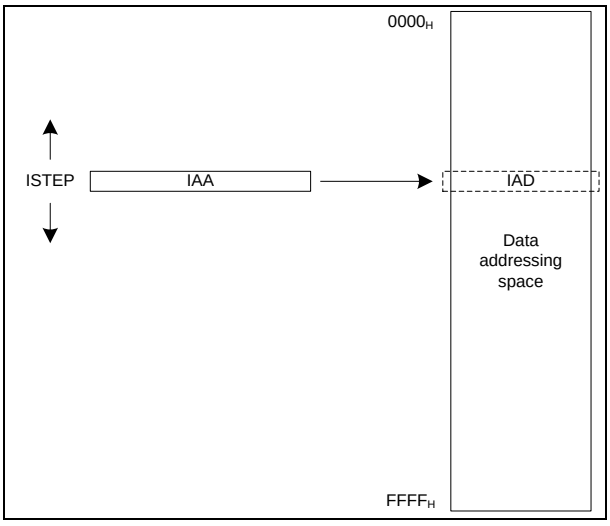


Figure 3-6 Indirect Addressing Diagram

Application example: using indirect addressing to clear the registers at the address 020_H ~ $02F_H$

```
……
CLR     IAAH
MOVI  0X20          ; initialize the pointer
MOVA IAAL           ; IAA points to RAM
NEXT1:
CLR    IAD          ; clear IAD
ISTEP 0X01          ; add 1 to IAA content
JBS    IAAL, 4      ;
GOTO NEXT1          ; not finished, go to the next register to clear
CONTINUE:           ; finished and continue to execute the next program
……
```

3. 4. 6 Special Function Registers

IAD: Indirect Addressing Data Register

Bit	7	6	5	4	3	2	1	0
Name	IAD<7:0>							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 IAD<7:0>: indirect addressing data

IAAL: Indirect Addressing Address Low Byte

Bit	7	6	5	4	3	2	1	0
Name	IAA<7:0>							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 IAA<7:0>: Indirect addressing address low byte

IAAH: Indirect Addressing Address High Byte

Bit	7	6	5	4	3	2	1	0
Name	IAA<15:8>							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 IAA<15:8>: Indirect addressing address high byte

Chapter4 I/O Ports

4. 1 Overview

The device is designed with up to 13 I/O pins and 1 input-only pin. All I/O pins are TTL and Schmitt inputs and CMOS outputs, except for the PA3 which is the TTL input-only.

◇ Port A (PA) features

- 7 bidirectional I/Os and 1 input
- TTL/SMT input and CMOS output
- Port A input/output control register (PAT)
- Port A weak pull-up control register (N_PAU)
- Port A weak pull-down control register (N_PAD)
- PA0~PA7 support the external key interrupt function
- Analog select register (ANS) for PA0, PA1,PA2 and PA7

◇ Port B (PB) features

- 6 bidirectional I/Os
- TTL/SMT input and CMOS output
- Port B input/output control register (PBT)
- Port B weak pull-up control register (N_PBU)
- Port B weak pull-down control register (N_PBD)
- PB0~PB5 support the external port interrupt function
- Analog select register (ANS) for PB0 and PB1

Note: When a port is configured as an output or external oscillator clock port, the internal weak pull-up/down is automatically disabled.

4. 2 Block Diagram

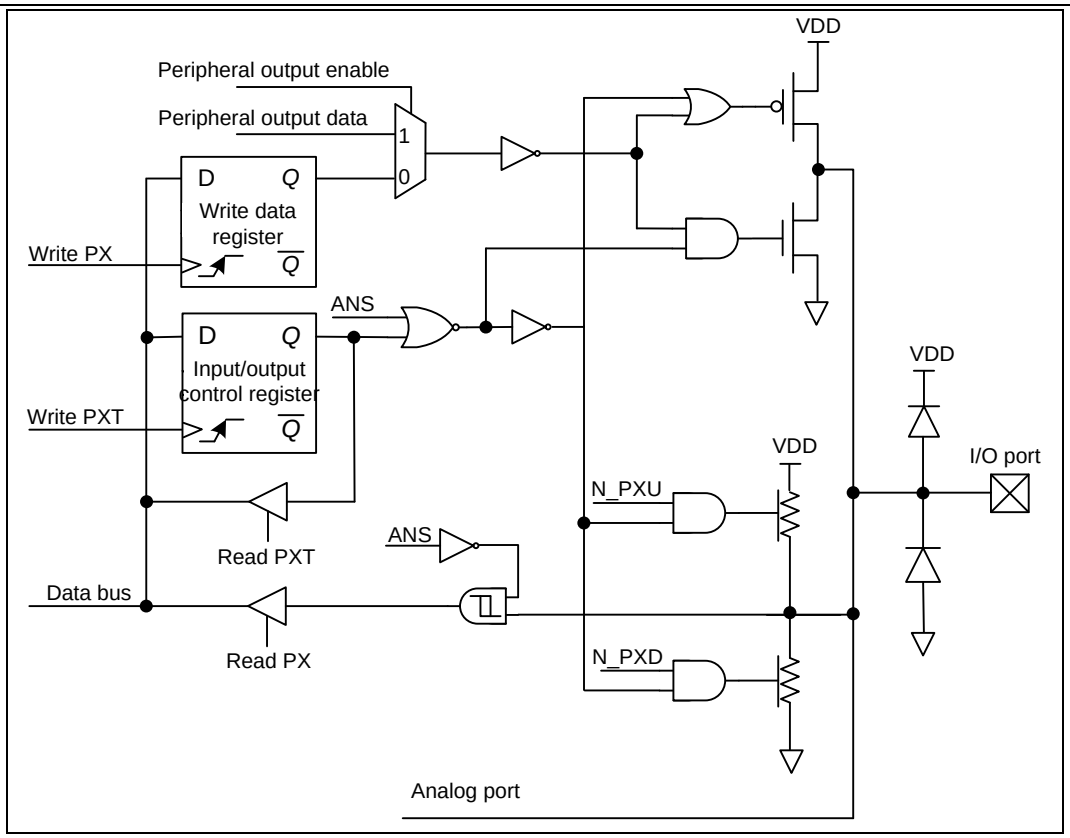


Figure 4-1 I/O Port Block Diagram (PA0, PA1, PA2, PA7, PB0 and PB1)

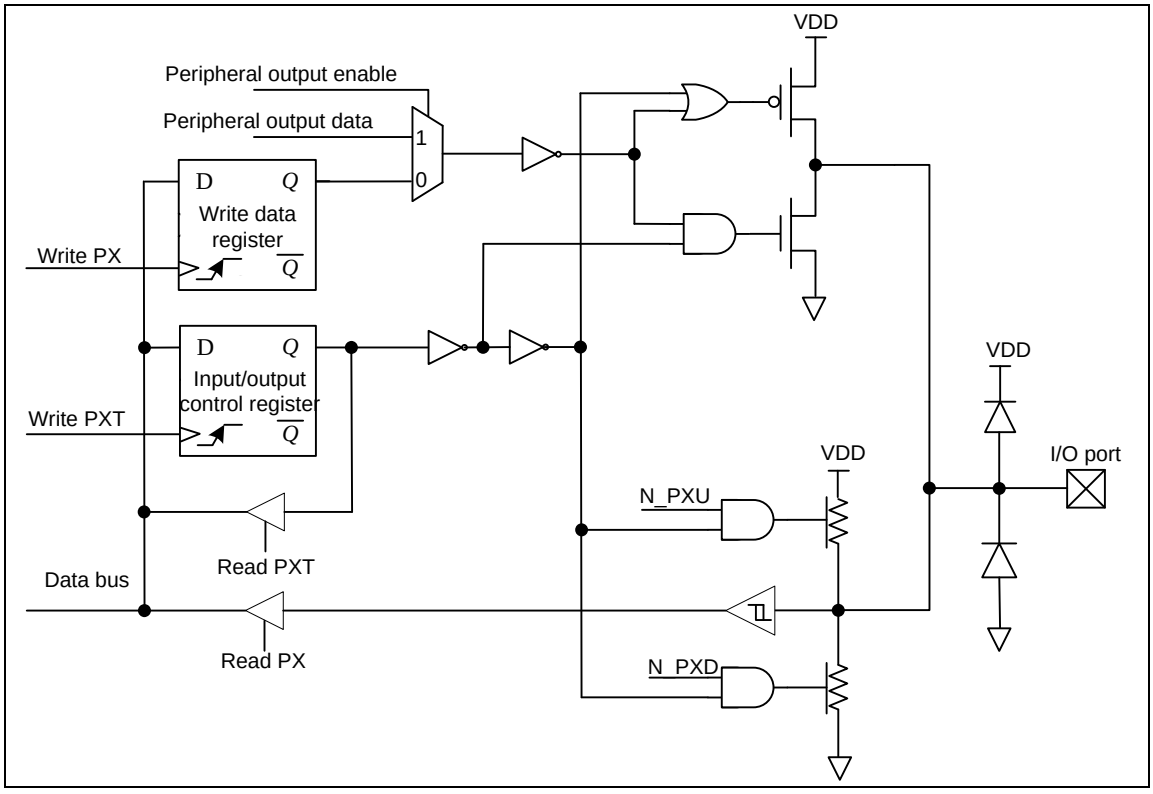


Figure 4-2 I/O Port Block Diagram (PA4, PA5, PA6, PB2, PB3, PB4 and PB5)

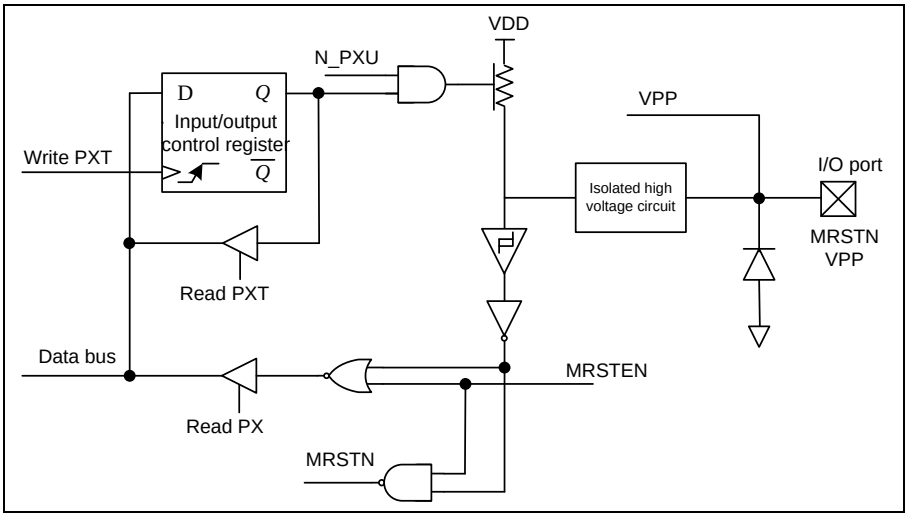


Figure 4-3 Input-only Port Block Diagram (PA3)

Note1: The corresponding control bit for PA3 in the PAT register is always 1, meaning that PA3 is an input-only port.

Note2: Except ISP/IAP operation, the voltage of PA3/MRSTN/VPP port must exceed the supply voltage.

4. 3 I/O Port Configuration

4. 3. 1 Input and Output Control

All I/O ports can be configured as inputs or outputs, controlled by the PxT register. When an I/O port is configured as a digital output, it outputs the content of the Px register which actually outputs the status of the corresponding pin, and reading the Px register reads the status of the corresponding pins. When an I/O port is configured as a digital input, reading the Px register actually reads the status of the corresponding pins.

4. 3. 2 Weak Pull-up/down Function

Many applications require the pin to connect with a pull-up or pull-down resistor to maintain a fixed and stable status, to prevent interference from outside. Only PA3 is weak pull-up enabled by default. All other ports have independent weak pull-up/down control registers.

Port	0	1	2	3	4	5	6	7
PA	Support	Support	Support	Support	Support	Support	Support	Support
PB	Support	Support	Support	Support	Support	Support	-	-

Table 4-1 I/O Port Weak Pull-up

Port	0	1	2	3	4	5	6	7
PA	Support	Support	Support	-	Support	Support	Support	Support
PB	Support	Support	Support	Support	Support	Support	-	-

Table 4-2 I/O Port Weak Pull-down

4. 3. 3 I/O Port High Drive Capability

PA (PA7~PA4, PA2~PA0) and PB (PB5~PB0) ports high drive capability can be controlled by N_PBD<5> bit of PLCS register.

4. 3. 4 Analog Digital Select Function

When an I/O pin is multiplexed with both analog and digital mode, it must be set to the proper mode prior to using the digital or analog function. PA0, PA1, PA2, PA7, PB0 and PB1 have independent analog and digital mode, selected by the ANS register. When an I/O pin is set to analog mode, reading the corresponding Px register will get 0.

4. 3. 5 I/O Pin Multiplexing

In order to optimize the use of resources, most of the I/O pins are multiplexed. When an I/O pin is multiplexed with several functions, the pin level is determined by the selected function.

4. 4 Port Interrupts

4. 4. 1 Key Interrupt (KINT)

The device supports 1 external key interrupt with up to 8 key inputs (KIN<7:0>). 8 key inputs share the same interrupt enable bit KIE (INTE<0>) and interrupt flag bit KIF (INTF<0>). Each input can be masked by the corresponding KMSKn (INTC0<7:0>). A key interrupt generated by any key input will affect the interrupt flag bit KIF.

When the pin associated with the KINn is set to a digital input, a key interrupt KINT will be generated if the pin level changes. If the key interrupt is used, the corresponding registers need to be configured and the internal weak pull-up resistor needs to be enabled. The pin level on the key input is compared to the last input value of the latch register. Prior to clearing the interrupt flag, it is a must to read/write the associated port register; otherwise the interrupt flag cannot be cleared. Before setting KMSKn =1 and KIE =1, execute a write or read operation on the port registers to clear the interrupt flag. A key interrupt is capable of waking up from idle mode.

Port	Input pin	Key mask	Interrupt enable	Interrupt flag
PA0	KIN0	KMSK0	KIE	KIF
PA1	KIN1	KMSK1		
PA2	KIN2	KMSK2		
PA3	KIN3	KMSK3		
PA4	KIN4	KMSK4		
PA5	KIN5	KMSK5		
PA6	KIN6	KMSK6		
PA7	KIN7	KMSK7		

Table 4-3 Key Interrupt

4. 4. 2 External Port Interrupt (PINT)

There are 4 external port interrupts and the external interrupt source is selected by PINT3S~PINT0S (PINTS<7:0>). Each external port interrupt is enabled by the corresponding enable bits PIE3~PIE0 (INTE1<3:0>). PEG3~PEG0 (INTC1<3:0>) select the triggering edge, rising edge or falling edge. When the pin associated with the PINTn is set to a digital input, an external port interrupt will be generated on the corresponding PINTn if the trigger condition goes true. An external port interrupt can set the corresponding interrupt flag PIFn (INTF1<3:0>) high, and also wake up from idle mode.

Port	Interrupt source select bits	Input pin	Edge select	Interrupt	Interrupt enable	Interrupt flag
PA0 PA2 PB0 PB4	PINT0S<1:0>	PINT0	PEG0	PINT0	PIE0	PIF0
PA1 PA3 PB1 PB5	PINT1S<1:0>	PINT1	PEG1	PINT1	PIE1	PIF1
PA6 PA4 PB2	PINT2S<1:0>	PINT2	PEG2	PINT2	PIE2	PIF2
PA7 PA5 PB3	PINT3S<1:0>	PINT3	PEG3	PINT3	PIE3	PIF3

Table 4-4 External Port Interrupt

4. 5 I/O Port Operation Consideration

If a port register is the destination of an operation except bitwise operation instruction, it actually performs a read-modify-write operation, where the register is read, the data is modified and the result is stored. A bitwise operation instruction only can influence the selected bit, the other bits are not influenced. It is recommended to use the bitwise operation instruction for single I/O modification. When the multiplexing function of an I/O pin is being switched, it is suggested to check the output values of the port register and determine whether to initialize the port register.

4. 6 Special Function Registers

The settings of the I/O ports are controlled by a few registers. The Px register indicates the pin level; the PxT register controls the input mode and output mode of the Px; the N_PXU and N_PXD respectively control the weak pull-up and weak pull-down function and the ANS register selects the analog mode or digital mode.

PA: Port A Voltage Level Status Register								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	x	x	x	x	x	x	x	x

"x": unknown

Bit 7~0 PA<7:0>: Port A voltage level
0: low level
1: high level

PAT: Port A Input/ Output Control Register								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	PAT7	PAT6	PAT5	PAT4	PAT3	PAT2	PAT1	PAT0
R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
POR	1	1	1	1	1	1	1	1

Bit 7~6 PAT<7:6>: Input and output mode select bits
0: output mode
1: input mode

Bit 5~4 PAT<5:4>: Input and output mode select bits
0: output mode
1: input mode
When PA5 and PA4 are used as external oscillator pins, they are analog ports and are fixed to 1 by hardware.

Bit 3 PAT3: fixed to 1 by hardware, input-only

Bit 2~0 PAT<2:0>: Input and output mode select bits
0: output mode
1: input mode

PB: Port B Voltage Level Status Register								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	—	—	PB5	PB4	PB3	PB2	PB1	PB0
R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	x	x	x	x	x	x

"x": unknown

Bit 7~6 Not in used

Bit 5~0 PB<5:0>: Port B voltage level
0: low level
1: high level

PBT: Port B Input/ Output Control Register								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	—	—	PBT5	PBT4	PBT3	PBT2	PBT1	PBT0
R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	1	1	1	1	1	1

Bit 7~6 Not in used

Bit 5~0 PBT<5:0>: Input and output select bits

0: output mode

1: input mode

N_PAU: Port A Weak Pull-up Control Register								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	N_PAU7	N_PAU6	N_PAU5	N_PAU4	N_PAU3	N_PAU2	N_PAU1	N_PAU0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	1	1	1	1	0	1	1	1

Bit 7~0 N_PAU <7:0>: Port A internal weak pull-up enable bits

0: Enabled

1: Disabled

N_PBU: Port B Weak Pull-up Control Register								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	—	—	N_PBU5	N_PBU4	N_PBU3	N_PBU2	N_PBU1	N_PBU0
R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	1	1	1	1	1	1

Bit 7~6 Not in used

Bit 5~0 N_PBU <5:0>: Port B internal weak pull-up enable bits

0: Enabled

1: Disabled

N_PAD: Port A Weak Pull-down Control Register								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	N_PAD7	N_PAD6	N_PAD5	N_PAD4	—	N_PAD2	N_PAD1	N_PAD0
R/W	R/W	R/W	R/W	R/W	—	R/W	R/W	R/W
POR	1	1	1	1	1	1	1	1

Bit 7~4 N_PAD <7:4>: Port A internal weak pull-down enable bits

0: Enabled

1: Disabled

Bit 3 Not in used

Bit 2~0 N_PAD <2:0>: Port A internal weak pull-down enable bits

0: Enabled

1: Disabled

N_PBD: Port B Weak Pull-down Control Register								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	—	—	PLCS	N_PBD4	N_PBD3	N_PBD2	N_PBD1	N_PBD0
R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	1	1	1	1	1	1

Bit 7~6 Not in used

Bit 5 PLCS: high drive enable bit for PA (PA7-4, PA2-0) and PB (PB5-0)
0: Disabled
1: Enabled

Bit 4~0 N_PBD <4:0>: Port B internal weak pull-down enable bits
0: Enabled
1: Disabled

Note: The PB5 port weak pull down function is disabled by hardware.

ANS: Analog/Digital Select Register								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	PWM20NS	PWM10NS	ANPA7	ANPB1	ANPB0	ANPA2	ANPA1	ANPA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 PWM20NS: PWM20 output polarity control bit
0: Inverting output of PWM21
1: Non-inverting output of PWM21

Bit 6 PWM10NS: PWM10 output polarity control bit
0: Inverting output of PWM11
1: Non-inverting output of PWM11

Bit 5 ANPA7:PA7 analog/digital select bit (AIN5)
0: Analog mode
1: Digital mode

Bit 4 ANPB1:PB1 analog/digital select bit (AIN4)
0: Analog mode
1: Digital mode

Bit 3 ANPB0:PB0 analog/digital select bit (AIN3)
0: Analog mode
1: Digital mode

Bit 2 ANPA2:PA2 analog/digital select bit (AIN2)
0: Analog mode
1: Digital mode

Bit 1 ANPA1:PA1 analog/digital select bit (AIN1)
0: Analog mode
1: Digital mode

Bit 0 ANPA0:PA0 analog/digital select bit (AIN0)
0: Analog mode
1: Digital mode

Chapter5 Special Functions and Operations

5. 1 System Clock and Oscillators

5. 1. 1 Overview

The clock for device operation is sourced from oscillators. Different oscillator options allow users to maximize functions in different applications. The device provides an external high frequency crystal/ceramic resonator XTAL, internal high-speed RC oscillator (16 MHz) and internal low speed RC oscillator (32 KHz). Flexible options optimize the speed and power consumptions. The external LP oscillator and internal low-speed RC oscillator also supply the clock source for the watchdog timer etc.

◇ Oscillator mode

- External oscillator (HS/XT/LP)
- Internal 16MHz RC oscillator (INTOSC and INTOSCO)
- Internal 32KHz RC oscillator

◇ Internal 16MHz RC oscillator

- 8-bit calibration register (OSCCAL)
- Factory calibration accuracy±2% at room temperature
- Multiple divided clocks available

◇ Internal 32KHz RC oscillator

- 8-bit calibration register (WDTCAL)

◇ System clock switching

- Clock switching between HS/XT/INTOSCH 16MHz oscillator clock and internal low-speed 32KHz INTOSCL
- Clock switching between external LP oscillator clock and internal high-speed 16MHz INTOSCH 16MHz

◇ Halt

- In idle 0 mode, the oscillator halts.
- In idle 1 mode, the oscillator continues to run but the system clock halts.

5. 1. 2 Clock Source

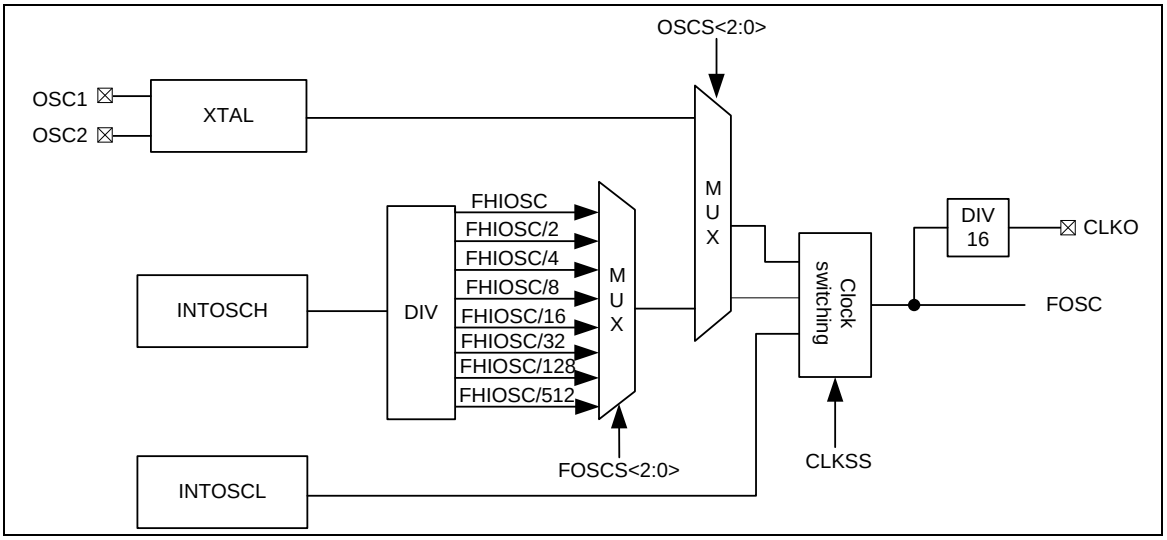


Figure 5-1 System Clock Block Diagram

5. 1. 2. 1 External Clock

For crystal/ceramic resonator, simply connecting the crystal between OSC1 and OSC2 can generate the required phase shift and feedback. To ensure the accuracy of oscillation frequency, two small capacitors C1 and C2 are required to connect to VSS. The specific capacitance is dependent on the used crystal/ceramic resonator and range is between 15-33pF. The configuration word OSCS<2:0> controls the operating mode of the external oscillator (User can configure the operating mode through the programming interface).

When OSCS<2:0> = 000, LP mode is selected.
When OSCS<2:0> = 010, HS mode is selected.
When OSCS<2:0> = 100, XT mode is selected.

In HS and XT mode, the crystal start up time is 512 system clock cycles. In low power LP mode, the start-up-stable time is approximately 1s.

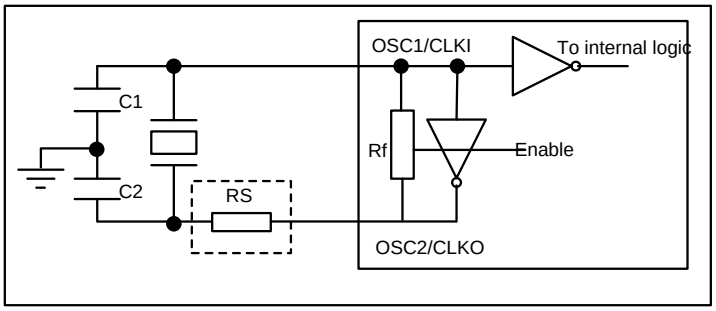


Figure 5-2 Crystal/Ceramic Oscillator Circuit (HS, XT and LP)

Note: Rs is optional.

Osc. type	Crystal frequency	C1*	C2*
LP	32KHz	33pF	33pF
XT	1MHz	15 ~ 33pF	15 ~ 33pF
	4MHz		
HS	8MHz		
	20MHz	15pF	15pF

Table 5-1 Oscillator Matching Capacitance Reference

Note: The capacitance can be slightly adjusted depending on the crystal oscillator frequency and the peripheral circuit.

5. 1. 2. 2 Internal High Speed 16MHz RC Oscillator (INTOSCH)

The built-in 16MHz RC oscillator requires no additional external device.

When the OSCS<2:0> = 000/110/111 and the CLKSS =1 of the OSCC register, the internal 16MHz RC oscillator INTOSCH is selected as the system clock source. PA2 and PA3 are used as general purpose I/O pins. The 16MHz RC oscillator can be divided down to 32KHz.

The RC oscillator has been calibrated at room temperature before leaving factory. When power on, the calibration value is automatically loaded and no any other operation is required on the calibration register OSCCAL.

5. 1. 2. 3 Internal Low Speed 32kHz RC Oscillator (INTOSCL)

The built-in 16MHz RC oscillator requires no additional external device, and can be souring the WDT counter and the system clock.

When the OSC<2:0> = 010/100/110/111 and the CLKSS = 0 of the OSCC register, the internal 32KHz RC oscillator is selected as the system clock source. PA2 and PA3 are used as general purpose I/O pins.

When power on, the calibration value is automatically loaded and no any other operation is required on the calibration register WDTCAL.

5. 1. 3 System Clock Switching

A high frequency clock enables the system to have higher performance while a low frequency clock consumes lower power. The flexible clock switching between high and low frequency allows the system designer to optimize power consumption versus process speed.

The CLKSS (OSCC<7>) selects the high or low speed system clock. When the system powers up, the CLKSS defaults to 0 and the system operates with the low speed system clock.

Four types of clock switching are available:

◇ Internal 32KHz INTOSCL is switched to internal high speed INTOSCH or external high speed HS/XT clock

- Write OSCS<2:0> = 010/100/110/111 of the configuration word CFG_WD
- Set CLKSS=1 of the OSSCC register
- Poll the HSOSCF bit of the OSCC register until HSOSCF=1
- Wait for one NOP instruction
- Poll the SW_HS bit of the PWEN register until SW_HS=1

◇ Inter high speed INTOSCH/external high speed HS/XT clock is switched to internal low speed INTOSCL clock

- Write OSCS<2:0>=010/100/110/111 of the configuration word CFG_WD
- Set CLKSS=0 of the OSSCC register
- Poll the WDTOSCF bit of the OSCC register until WDTOSCF =1
- Wait for one NOP instruction
- Poll the SW_WDT bit of the PWEN register until SW_WDT =1

◇ External LP clock is switched to internal INTOSCH clock

- Write OSCS<2:0>=000 of the configuration word CFG_WD
- Set CLKSS =1 of the register OSCC
- Poll the HSOSCF bit of the OSCC register until HSOSCF=1
- Wait for one NOP instruction
- Poll the SW_HS bit of the PWEN register until SW_HS=1

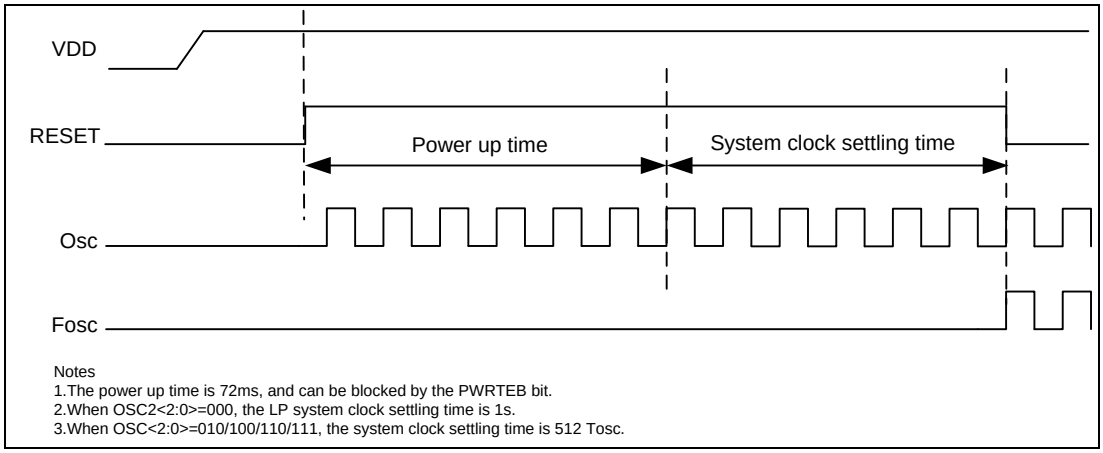
◇ Internal INTOSCH clock is switched to external LP clock

- Write OSCS<2:0>=000 of the configuration word CFG_WD
- Set CLKSS=0 of the OSSCC register
- Poll the LPOSCF bit of the OSCC register until LPOSCF =1
- Wait for one NOP instruction
- Poll the SW_LP bit of the PWEN register until SW_LP =1

System clock source	OSCS<2:0>	CLKSS
LP	000	0
HS	010	1
XT	100	1
INTOSCH	000	1
	110	1
	111	1
INTOSCL	010	0
	100	0
	110	0
	111	0

Table 5-2 Clock Switching Configuration

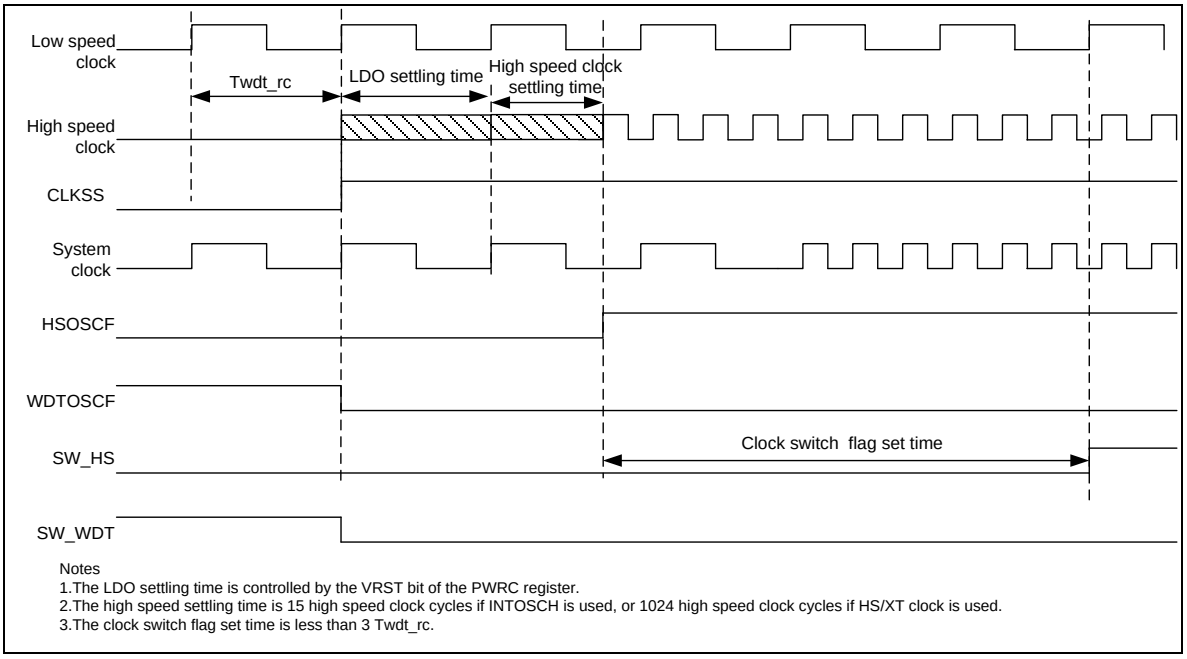
5. 1. 3. 1 Power-on Timing



Notes
1.The power up time is 72ms, and can be blocked by the PWRTEB bit.
2.When OSC2<2:0>=000, the LP system clock settling time is 1s.
3.When OSC<2:0>=010/100/110/111, the system clock settling time is 512 Tosc.

Figure 5-3 Power-on Timing

5. 1. 3. 2 System Clock Switching Timing



Notes
1.The LDO settling time is controlled by the VRST bit of the PWRC register.
2.The high speed settling time is 15 high speed clock cycles if INTOSCH is used, or 1024 high speed clock cycles if HS/XT clock is used.
3.The clock switch flag set time is less than 3 Twdt_rc.

Figure 5-4 INTOSCL Switching to INTOSCH/HS/XT Clock

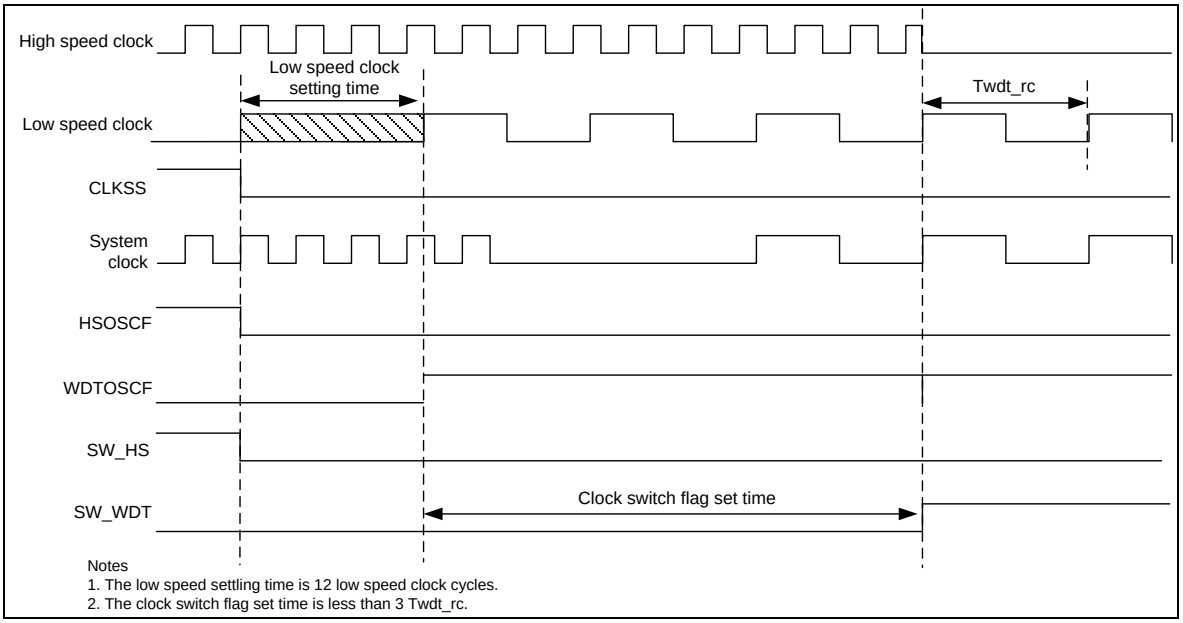


Figure 5-5 INTOSCH/HS/XT Switching to INTOSCL Clock

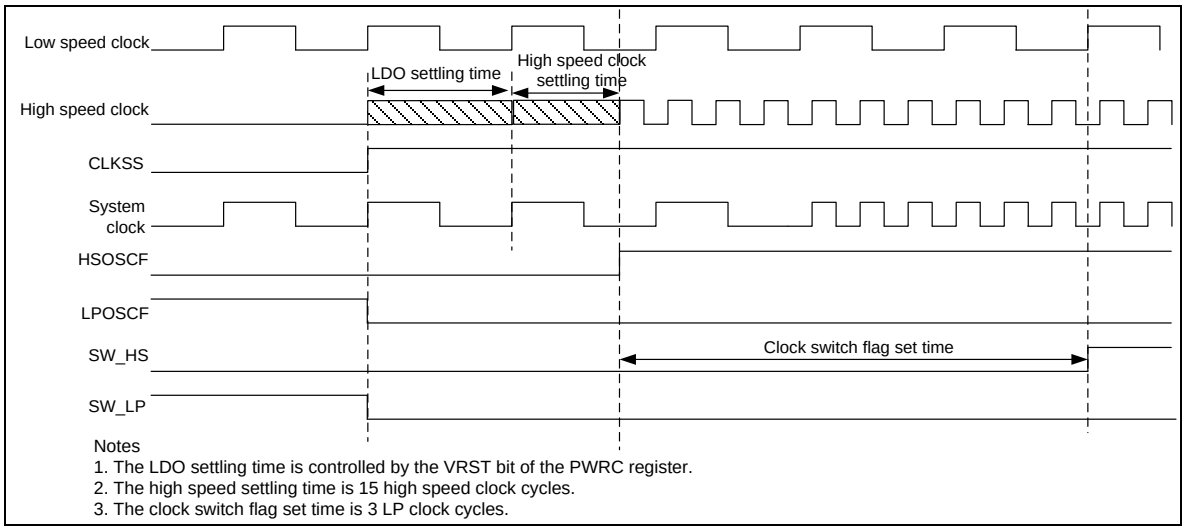


Figure 5-6 Low Speed LP Clock Switching to INTOSCH Clock

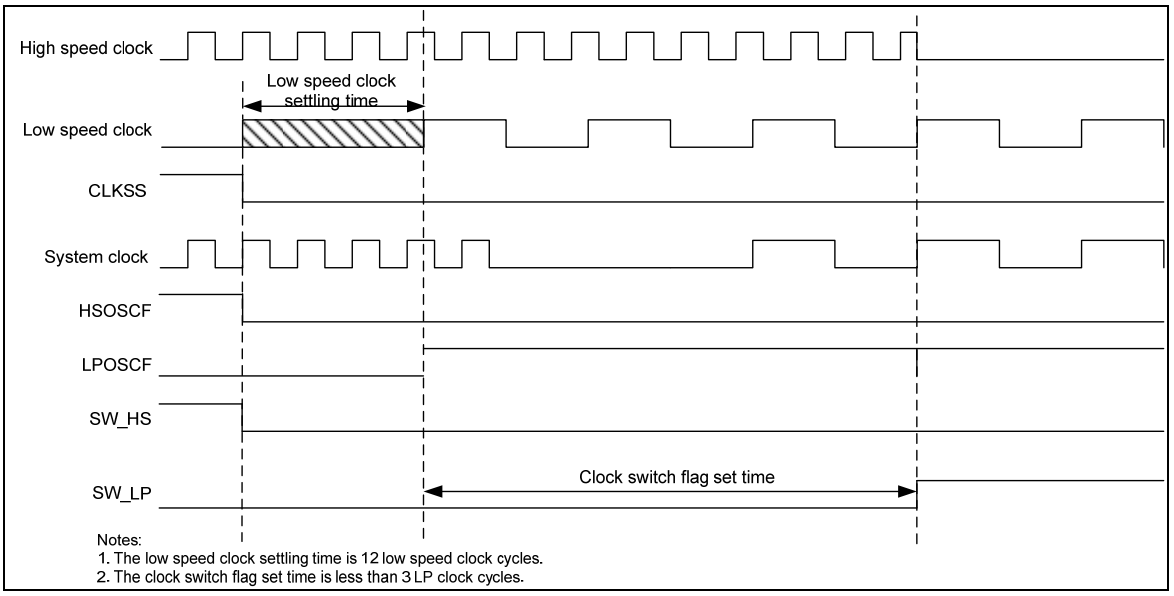


Figure 5-7 INTOSCH Clock Switching to Low Speed LP Clock

5. 1. 4 System Clock Frequency Division

When the internal 16MHz INTOSCH clock is sourcing the system clock, the system clock can be divided down to 32KHz with a maximum division rate of 1:512, selected by the FOSC<2:0> bits of the OSSC register.

5. 1. 5 Special Function Registers

CALPROT: Calibration Protection Register								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	—	—	—	—	—	—	—	CALPROT0
R/W	—	—	—	—	—	—	—	R/W
POR	0	0	0	0	0	0	0	1

Bit 7~1 Not in used

Bit 0 CALPROT0: Calibration value protect bit

1: The calibration value is under protection.

0: The calibration value is not under protection.

Writing 55H to the CALPROT register removes the protection; writing other values to the register enables the protection.

Note: The OSCCAL and WDTCAL registers are under protection of the CALPROT register.

OSCCAL: Internal 16MHz RC Oscillator Calibration Register								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	OSCCAL<7:0>							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	1	0	1	0	1	0	0	1

Bit 7~0 OSCCAL<7:0>: Internal 16MHz clock calibration value

Note: The OSCCAL register is protected by the CALPROT register and used for the internal 16MHz clock calibration. The oscillator has already been calibrated to 16MHz before leaving factory. If there is no special requirements, the user need not to set this register to avoid overwriting the default calibration value.

OSCC: Oscillator Control Register

Bit	7	6	5	4	3	2	1	0
Name	CLKSS	FOSCS<2:0>			—	WDTOSCF	HSOSCF	LPOSCF
R/W	R/W	R/W	R/W	R/W	—	R	R	R
POR	0	1	1	0	0	1	0	x

Bit 7 CLKSS: Clock switching select bit
When OSCS<2:0>=000,
0: External low speed LP 32KHz clock source
1: Internal high speed 16MHz INTOSCH clock source
When OSCS<2:0>=010/100/110/111,
0: Internal low speed 32KHz INTOSCL clock source
1: Internal high speed 16MHz INTOSCH clock or external high speed HS/XT clock source

Bit 6~4 FOSCS<2:0>: System clock select bits
000:32KHZ
001:125KHZ
010:500KHz
011:1MHz
100:2MHz
101:4MHz
110:8MHz
111:16MHz

Bit 3 Not in used

Bit 2 WDTOSCF: Internal 32KHz ready flag bit
0: Not ready
1: Ready

Bit 1 HSOSCF: High speed clock ready flag bit
0: Not ready
1: Ready

Bit 0 LPOSCF: External LP oscillator ready flag bit
0: Not ready
1: Ready

OSCP: Oscillator Protection Register

Bit	7	6	5	4	3	2	1	0
Name	OSCP<7:0>							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	1	1	1	1	1	1	1	1

Bit 7~0 OSCP<7:0>: Oscillator write-protection bits

Writing 55_H to the OSCP bits to modify the FOSCS and CLKSS bits. When the FOSCS and CLKSS are being written, the OSCP bits will be reset to FF_H. When the OSCP bits are written to values other than 55_H, any write to the FOSCS and CLKSS will be ignored.

PWEN: Power Enable Register								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	—	SW_WDT	SW_HS	SW_LP	—	—	RCEN	—
R/W	—	R	R	R	—	—	R/W	—
POR	0	1	0	0	0	0	1	1

Bit 7,3~2 Not in used

Bit 6 SW_WDT: Switch to internal 32KHz clock status bit
0: Switching not complete
1: Switching complete

Bit 5 SW_HS: Switch to HS/XT/16MHz INTOSCH clock status bit
0: Switching not complete
1: Switching complete

Bit 4 SW_LP: Switch to external LP clock status bit
0: Switching not complete
1: Switching complete

Bit 1 RCEN:WDT internal RC clock enable bit (set 1 to enable WDT internal RC clock by software)
When CLKSS=1 in idle mode
0: Disable the WDT internal RC clock
1: Enable the WDT internal RC clock
In non-idle mode, the RC clock is always enabled regardless of the status of the RCEN.
When CLKSS=0,
The RCEN is fixed to 1 and not writeable.

Bit 0 Not in used

Note1: It is recommended to set RCEN to 1 by software to enable WDT internal RC clock.
Note2: If frequent clock switching is required, the SW_LP, SW_HS and SW_WDT must be checked to determine if the switching is completed.

5. 2 Watchdog Timer (WDT)

5. 2. 1 Overview

The watchdog timer is used to reset the device when the software fails. If the system enters into a false working state, the watchdog timer is able to reset the chip within a reasonable time. When the watchdog timer is enabled, if the user program fails to clear the watchdog timer, the system will be reset within the preset time.

◇ WDT

- 8-bit WDT counter (no physical address, not readable/writable)
- 8-bit prescaler (no physical address, not readable/writable)
- WDT control register (WDTC)
- WDT counter period register (WDTP)
- Wake-up
- Reset

◇ Internal WDT RC oscillator

- WDT clock source options: internal 32KHz RC clock and external LP oscillator clock
- 8-bit WDT calibration register (WDTCAL)
- Factory-calibrated accuracy within±15% at room temperature. See Electrical Characteristics for the WDT overflow time influenced by the temperature.

5. 2. 2 Block Diagram

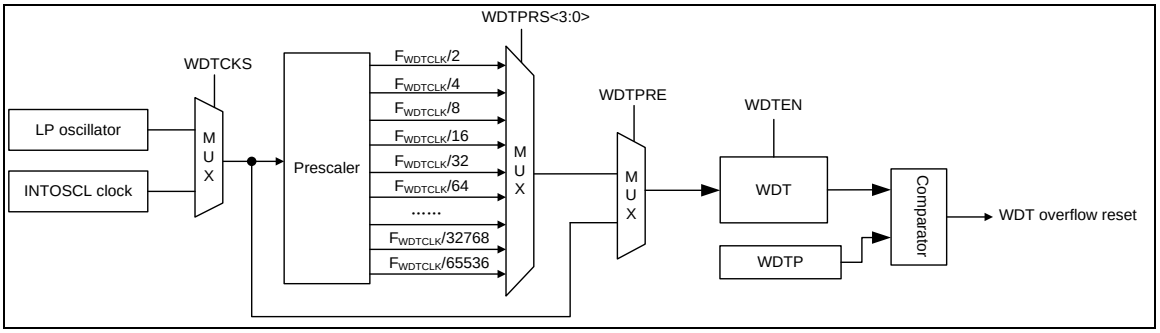


Figure 5-8 Watchdog Timer Block Diagram

5. 2. 3 WDT Timer

The 8-bit WDT counter is enabled by setting the WDTEN = 1, and disabled by clearing the WDTEN.

When the OSCS<2:0> selects the LP mode, the WDT clock source can either be the internal 32KHz RC clock or the external LP oscillator. If the WDTCKS = 0, the RC clock is selected. If the WDTCKS = 1, the external LP oscillator is then selected.

A prescaler is available and the prescale ratio can be selected by the WDTPRS <3:0> of the WDTC register. The prescaled clock will be used as the WDT counter clock. When the WDTPRE (WDTC<4>) is cleared, the prescaler is disabled and the WDT clock is 32KHz. When the WDTPRE (WDTC<4>) is set, the prescaler is enabled.

The period register WDTP is read and write accessible. When the counter value reaches the set period, an overflow will occur, which can wake up from idle mode. Besides, a WDT overflow can also reset the device. In order to avoid unnecessary resets, using the CWDT instruction to clear the WDT counter from time to time.

When the prescale ratio is set to 1:2 and the WDTP value is set to FF_H, if the internal 32KHz clock is used as the WDT clock source, the overflow time is about 16ms at room temperature; if the prescale is disabled, the overflow time is about 8ms. Refer to Characteristic Graphs for specific WDT overflow time under other conditions.

It is important to note that when RCEN = 0, the WDT is only disabled in idle mode. In other operating modes, the RC clock is always enabled regardless of the status of the RCEN.

Note: The RCEN (PWEN<1>) must be set to 1 for the WDT to operate.

5. 2. 4 Special Function Registers

The function control of the WDT involves the WDTC register and the chip configuration word. The configuration word enables the WDT, and the WDTC register selects the clock source, enables the prescaler and selects the prescale ratio. In addition, the WDTP configures the WDT counter period and the WDTCAL calibrates the internal 32KHz clock.

WDTCAL: WDT Clock Calibration Register

Bit	7	6	5	4	3	2	1	0
Name	WDTCAL<7:0>							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	1	0	0	0	0	1	0	0

Bit 7~0 WDTCAL<7:0>: Internal 32KHz clock calibration value

Note: The WDTCAL register is protected by the CALPROT register and used for the internal 132KHz clock calibration. The oscillator has already been calibrated to 32KHz before leaving factory. Users are prohibited to modify this register, or else it might lead to exceptions.

WDTC: WDT Control Register

Bit	7	6	5	4	3	2	1	0
Name	WDTCKS	—	—	WDTPRE	WDTPRS<3:0>			
R/W	R/W	—	—	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	1	0	1	1	1

Bit 7 WDTCKS: WDT counter clock source select bit
0: Internal WDT RC clock
1: External LP oscillator clock

Bit 6~5 Not in used

Bit 4 WDTPRE: WDT prescaler enable bit
0: Disabled
1: Enabled

Bit 3~0 WDTPRS <3:0>: WDT prescale ratio select bits

0000:1:2
0001:1:4
0010:1:8
0011:1:16
0100:1:32
0101:1:64
0110:1:128
0111:1:256 (default)
1000:1:512
1001:1:1024
1010:1:2048
1011:1:4096
1100:1:8192
1101:1:16384
1110:1:32768
1111:1:65536

WDTP: WDT Counter Period Register								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	WDTP<7:0>							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	1	1	1	1	1	1	1	1

Bit 7~0 WDTP<7:0>: WDT counter period

5. 3 Reset Module

5. 3. 1 Overview

- ◇ Power-on Reset POR
- ◇ Brown-out Reset BOR
- ◇ External Reset MRSTN, active low
- ◇ WDT overflow Reset
- ◇ Software reset RST

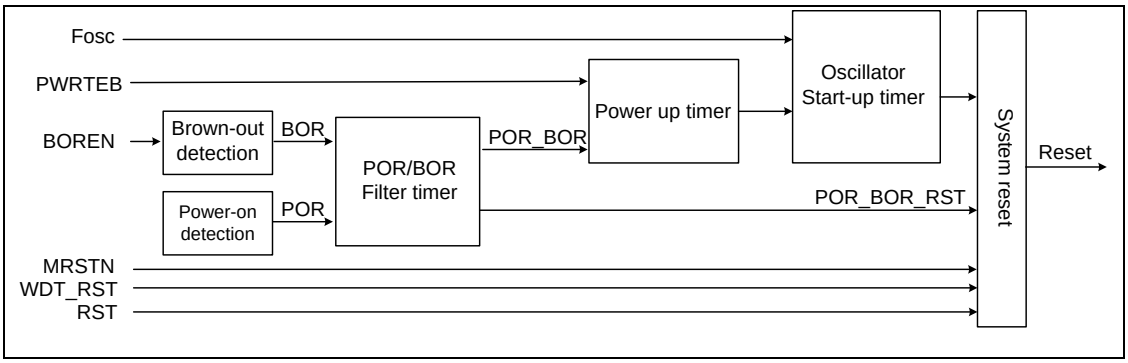


Figure 5-9 Chip Reset Diagram

5. 3. 2 Power-on Reset

A power-on reset signal is generated during power up and remains until VDD rises up to operating voltage for normal operation. And it takes time for VDD to reach the normal operating voltage. The POR timing is as follows.

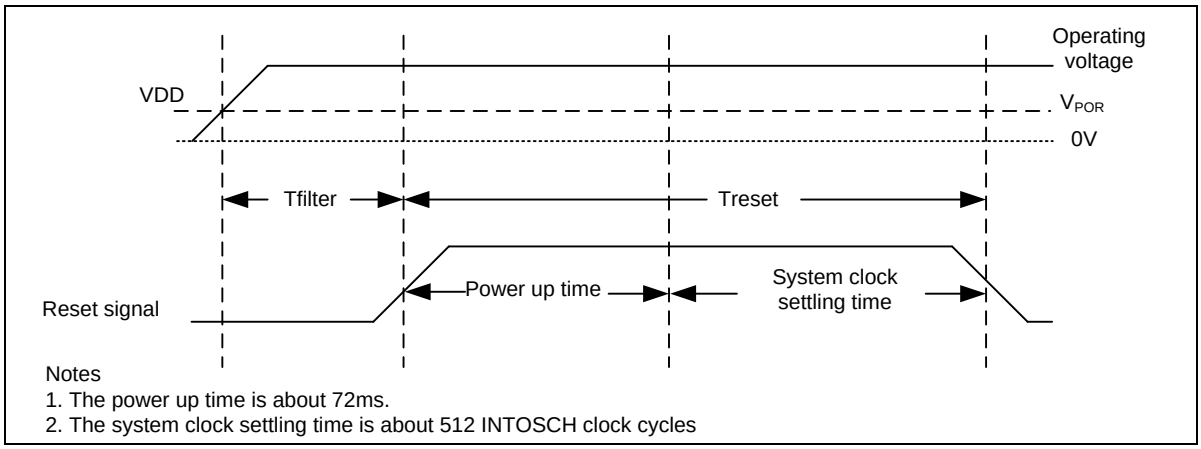


Figure 5-10 POR Timing Diagram

5. 3. 3 Brown-out Reset

A brown-out reset places the device into reset when the system voltage falls below a preset level, for instance, changing batteries. A voltage drop may lead to device irregular behaviors and BOR ensures the device to stay in reset state to avoid program execution errors.

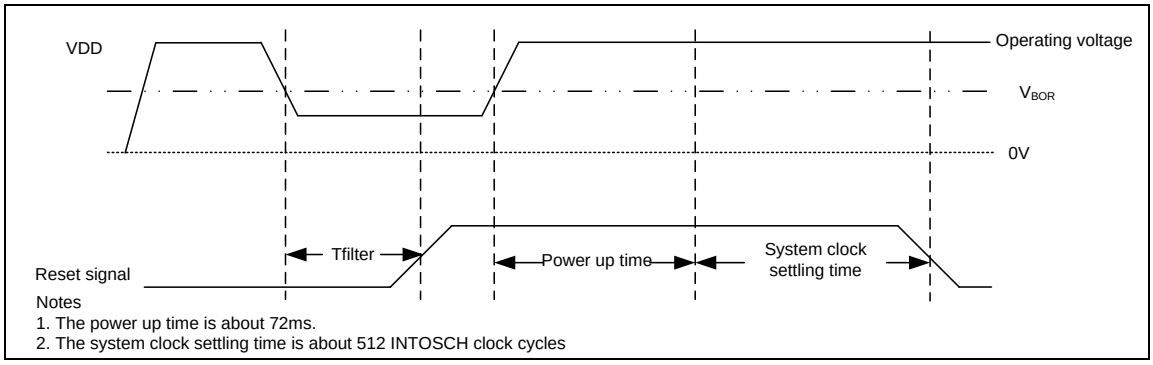


Figure 5-11 BOR Timing Diagram

Note1: The power up time 72ms can be blocked by the PWRTEB.

Note2: When the HS/XT/16MHz INTOSCH is configured for, the system clock settling time is 512x Tosc; when the LP mode is configured for, the system clock settling time is 1s.

The BORVS<1:0> bits enable the BOR and configure the BOR voltage threshold.

BORVS<1:0>	BOR Voltage Threshold	BOR Enable
11	Device reset if below 3.4V	Enable
10	Device reset if below 2.7V	Enable
01	Device reset if below 2.2V	Enable
00	—	Disable

Table 5-3 BOR Voltage Threshold Configuration

5. 3. 4 MRSTN Pin Reset

When the MRSTEN of the CFG_WD is set to 1, the pin is used for system reset. When the reset pin is input with a low level signal, the system resets. When the reset pin is input with a high level signal, the system functions normally. It is important to note that the MRSTN pin must be input high level after the system power-on is completed, otherwise the system will stay in reset state. More important, the MRSTN pin is not allowed to be directly tied to VDD, and the voltage on the MRSTN pin cannot be more than VDD.

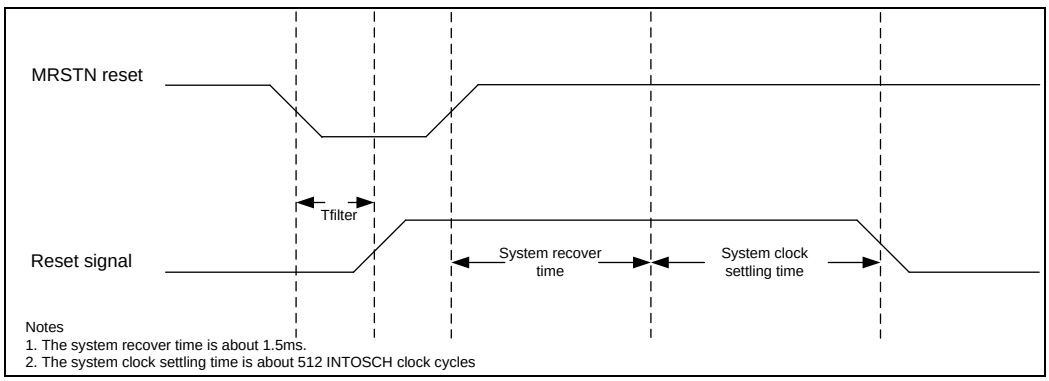


Figure 5-12 MRSTN Pin Reset

Two typical external reset circuits are introduced below.

1. RC Reset

The RC reset circuit is one of the simplest N_MRST resets which is used when the requirement for the external environment is low.

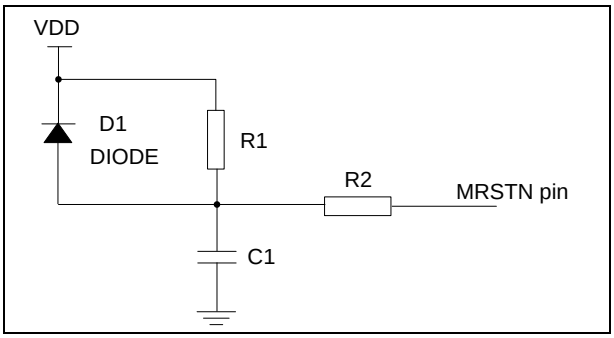


Figure 5-13 MRSTN Reset Reference Circuit 1

Note: In RC reset, 47KΩ≤R1≤100KΩ, C1=0.1μF, R2 is a current limiting resistor, 0.1KΩ≤R2≤1KΩ.

2. PNP Reset

A PNP reset is used in a circuit where the interference from power line is relatively strong.

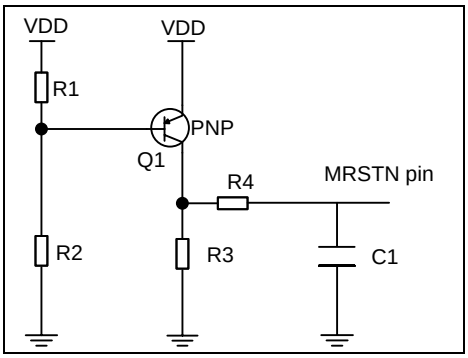


Figure 5-14 MRSTN Reset Reference Circuit 2

Note: In PNP transistor reset circuit, the voltage divided by R1 (2KΩ) and R2 (10KΩ) is used as a base input; the emitter is connected to VDD. One end of the collector is connected to ground through R3 (20KΩ), the other is connected to ground through R4 (1KΩ) and C1 (0.1μF). The ungrounded end of C1 is used as an input to MRSTN pin.

5. 3. 5 WDT Overflow Reset

A watchdog overflow reset is considered as a system protection. In normal operation, the watchdog timer is cleared by program. If the system goes wrong and enters into an unknown state, the watchdog timer which cannot be cleared by program will overflow; consequently a reset will then occur. After the watchdog reset has occurred, the system will reboot.

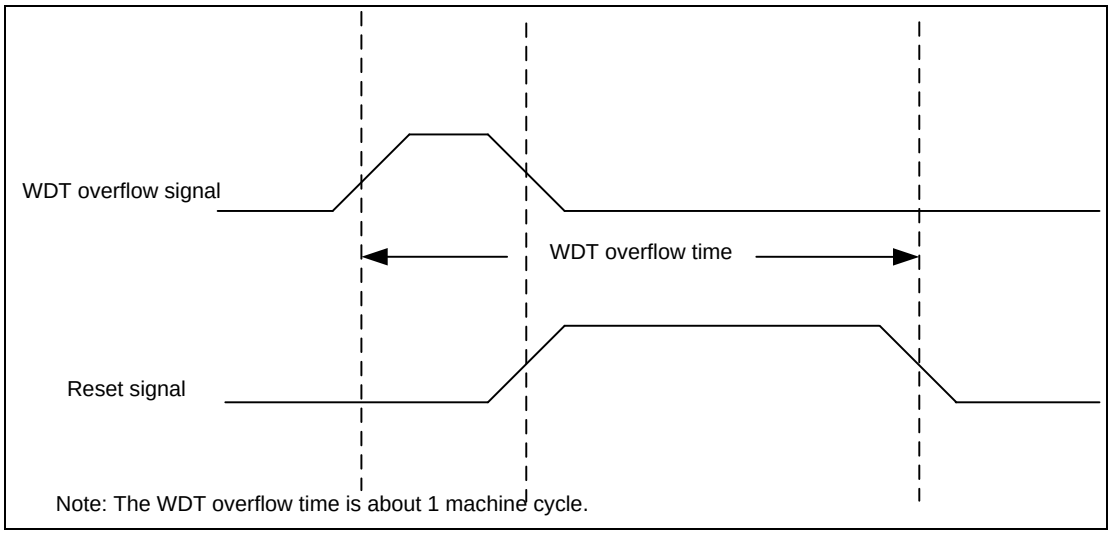


Figure 5-15 WDT Overflow Reset

5. 3. 6 RST Instruction Reset

The RST instruction can be executed to reset the device. Following a reset, all status bits are affected.

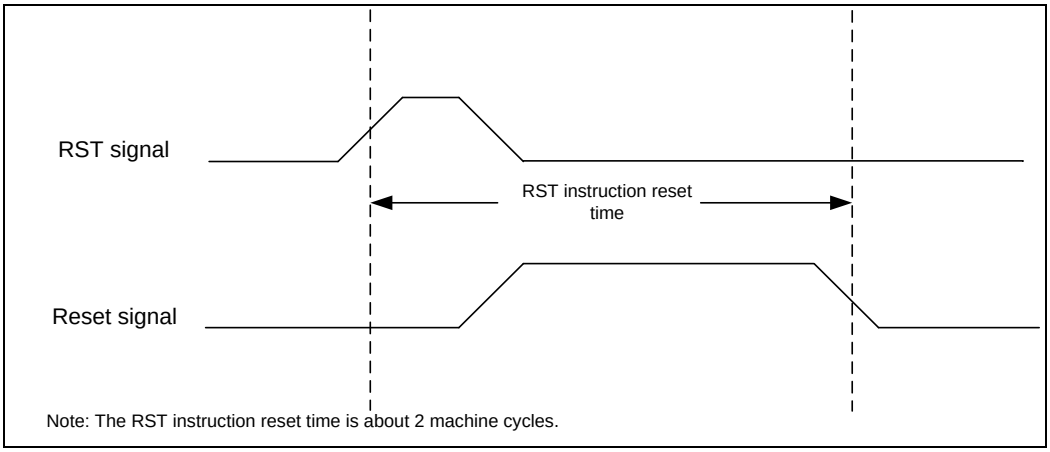


Figure 5-16 RST Instruction Reset

5. 3. 7 Special Function Registers

PWRC: Power Reset Control Register								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	LPM	VRST<1:0>		N_RSTI	N_TO	N_PD	N_POR	N_BOR
R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W
POR	0	1	0	1	1	1	0	x

"x": unknown

Bit 7 LPM: Low power mode select bit
0: IDLE0 mode
1: IDLE1 mode

Bit 6~5 VRST<1:0>: LDO settling time select bits
When CLKSS=1,

00: LDO settling time is 16 internal 32KHz clock cycles
01: LDO settling time is 32 internal 32KHz clock cycles
10: LDO settling time is 64 internal 32KHz clock cycles
11: LDO settling time is 128 internal 32KHz clock cycles
When CLKSS=0,
11: LDO settling time is 128 internal 32KHz clock cycles
Others: LDO settling time is 64 internal 32KHz clock cycles

Bit 4 N_RSTI: Reset instruction flag bit
0: The reset instruction has been executed (must be set to 1 by software)
1: No reset instruction has been executed.

Bit 3 N_TO: WDT overflow flag bit
0: Cleared when WDT overflows
1: Set after POR or executing CWDT and IDLE instruction

Bit 2 N_PD: Power down flag bit
0: Cleared after executing IDLE instruction
1: Set after POR or executing CWDT instruction

Bit 1 N_POR:POR flag bit
0: POR occurred (must be set to 1 after POR)
1: No POR occurred

Bit 0 N_BOR: BOR flag bit
0: BOR occurred (must be set to 1 after BOR)
1: No BOR occurred

Note: The LDO is a built-in power module to supply power to the internal circuit.

5. 4 Low Power Consumption

5. 4. 1 MCU Low Power Mode

The chip supports two idle modes, idle 0 and idle 1, configured by the LPM bit of the PWRC register.

◇ IDLE 0

- When the LPM =0, the idle 0 mode is entered by executing the IDLE instruction.
- The clock source stops (except 32KHz RC clock source) and the system clock stops.
- Program and synchronous module are suspended while asynchronous module continues to run. And device power is reduced.
- Supports low power wake-up with configurable wake-up time. LDO settling time should be considered.
- All I/Os maintain the status they had before entering idle 0
- If WDT is enabled, WDT will be cleared but keeps running.
- N_PD is cleared and N_TO is set.

◇ IDLE1

- When the LPM =1, the idle 1 mode is entered by executing the IDLE instruction.
- The clock source continues to run but the system clock stops.
- Program and synchronous module are suspended while asynchronous module continues to run. And device power is reduced.
- Supports low power wake-up with configurable wake-up time, minimum 1 machine cycle
- All I/Os maintain the status they had before entering idle 1
- If WDT is enabled, WDT will be cleared but keeps running.
- N_PD is cleared and N_TO is set.

5. 4. 2 Low Power Mode Configuration

The LPM bit of the PWRC register is used to select a idle mode. When LPM = 0, the idle instruction is executed and idle 0 is entered. When LPM =1, the idle instruction is executed and idle 1 is entered.

Low power mode	LPM
Idle 0	0
Idle 1	1

Table 5-4 Low Power Mode Configuration

All I/O pins should be tied to VDD or VSS to reduce the power consumption. The I/O pins with high-impendance input should be externally pulled high or pulled low, and the MRSTN pin must be stay logical high to avoid the switching current caused by the floating pins.

5. 4. 3 Wake-up from Idle

The program is halted after the system enters the low power mode. The device can wake up from idle through one of the following events.

No.	Wake-up source	Interrupt mask	Interrupt enable	Interrupt mode	Remark
1	MRSTN	-	-	-	External reset
2	WDT	-	-	-	WDT overflow
3	KINT0	KMSK0	KIE	Default	External key interrupt
	KINT1	KMSK1			
	KINT2	KMSK2			
	KINT3	KMSK3			
	KINT4	KMSK4			
	KINT5	KMSK5			
	KINT6	KMSK6			
	KINT7	KMSK7			
4	PINT0	-	PIE0	Default	External port interrupt 0
5	PINT1	-	PIE1	Default	External port interrupt 1
6	PINT2	-	PIE2	Default	External port interrupt 2
7	PINT3	-	PIE3	Default	External port interrupt 3

Table 5-5 Wake-up Events from Idle

Note1: For the device to wake up through an interrupt event, the corresponding interrupt enable bit must be enabled. Wake-up will occur regardless of the state of the global interrupt enable GIE. If a peripheral interrupt is generated, the system will still wake up from the low power mode even if the GIE=0. However, the interrupt service routine will not be executed.

Note2: For the external key interrupt, before enabling the interrupt and the mask bit, it is necessary to read/write the port registers and clear the KIF to avoid generating unwanted interrupts.

5. 4. 4 Wake-up Timing

When a wake-up event has occurred, execute the following operations depending on the OSCS<2:0> setting.

◇ When the OSCS<2:0> is configured for the HS/XT/INTOSCO/INTOSC mode

- In idle 0 mode (LPM=0), it needs to wait for VRwkdly time (set by VRST (PWRC<6:5>)) which is called the LDO settling time. After that, the next instruction after the IDLE instruction will be executed after the system clock has been running for Twkdly time which is called the wake-up delay, set by register WKDC.
- In idle 1 mode (LPM=1), the next instruction after the IDLE instruction will be

executed after the device has been running for Twkdly time. No VRwkdly time is required.

◇ When OSCS<2:0> is configured for LP mode,

- In idle 0 mode (LPM=0), it needs to wait for VRwkdly time (set by VRST (PWRC<6:5>)) which is called the LDO settling time, followed by LPwkdly time which is called the external crystal oscillator settling time. After that, the next instruction after the IDLE instruction will be executed after the system clock has been running for Twkdly time which is called the wake-up delay, set by the register WKDC.
- In idle 1 mode (LPM=1), the next instruction after the IDLE instruction will be executed after the device has been running for Twkdly time. No VRwkdly time or LPwkdly time is required.

OSCS configuration	Low power mode	Calculation
All modes	Idle 1	(WKDC[7:0]+1) × 2 Tosc
Non LP mode	Idle 0	VRwkdly + (WKDC[7:4] + 1) × 16 × 2 Tosc
LP mode		VRwkdly + LPwkdly + (WKDC[7:4] + 1) × 16 × 2 Tosc

Table 5-6 Wake-up Time Calculations

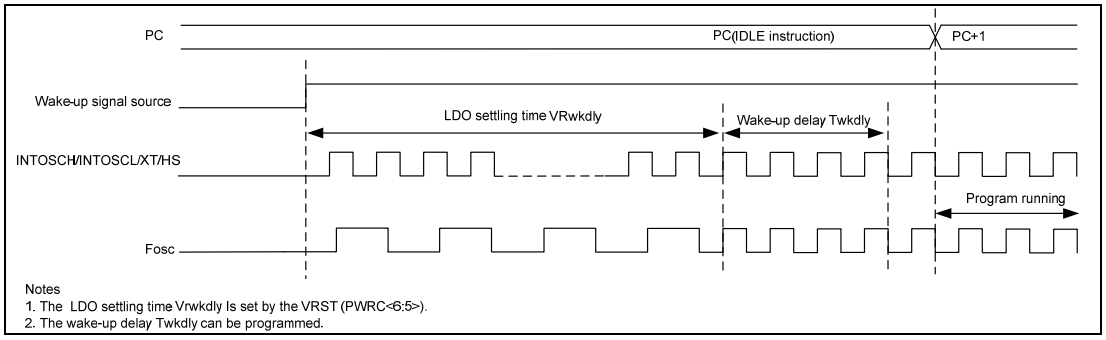


Figure 5-17 Wake-up Timing from Idle 0 under HS/XT/INTOSCO/INTOSC Mode

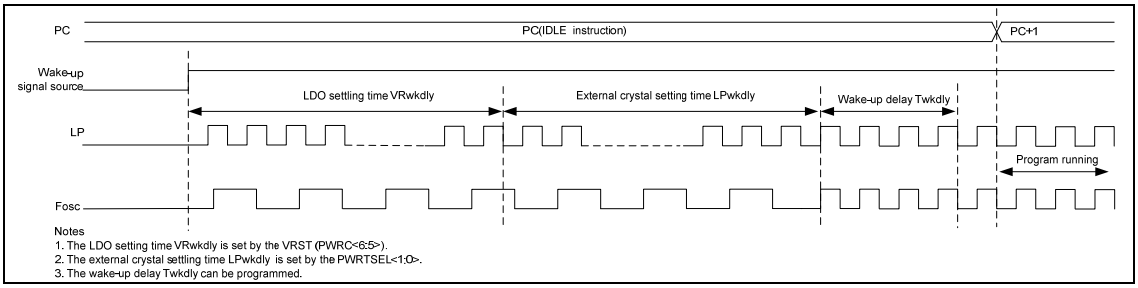


Figure 5-18 Wake-up Timing from Idle 0 under LP Mode

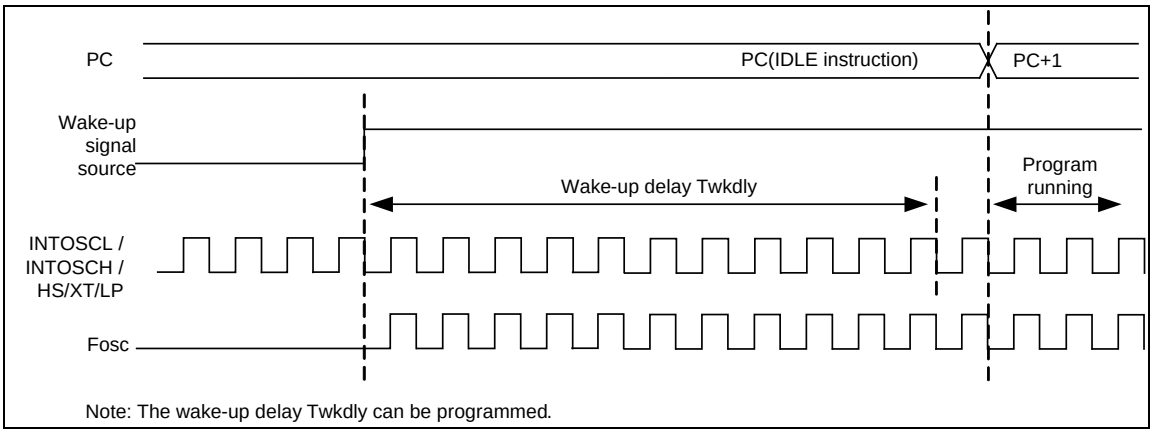


Figure 5-19 Wake-up Timing from Idle 1 under HS/XT/INTOSCO/INTOSC/LP Mode

5. 4. 5 Special Function Registers

WKDC: Wake-up delay control register								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	WKDC<7:0>							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	1	1	1	1	1	1	1	1

Bit 7~0 WKDC<7:0>: wake-up delay set bits

00_H: Shortest delay

……

FF_H: Longest delay

Chapter6 Peripherals

6. 1 8-bit PWM Time-based Timers (T8P1/T8P2)

6. 1. 1 Overview

This MCU offers two PWM time-based timers, T8P1 and T8P2. Two operating modes are available: timer mode and PWM mode. Timer mode works according to the time set by the register, allowing the timer to generate interrupt requests or complete other operations in a selective manner. PWM mode is used for PWM output.

◇ Two operating modes (clocked by Fosc/2)

- Timer mode
- PWM mode, up to 11-bit average resolution, complementary PWM outputs with software configurable dead-band time

◇ T8Pn functional registers

- 4-bit prescaler and 8-bit postscaler (no physical addresses, not readable/writeable by software)
- 8-bit counter (T8Pn)
- 8-bit resolution register (T8PnR)
- 8-bit period register (T8PnP)
- 8-bit period buffer (PRDBUF, no physical addresses, not readable/writeable by software)
- 8-bit resolution buffer (RESBUF, no physical addresses, not readable/writeable by software)
- 8-bit T8Pn PWM dead-band time register (T8PnPDT)
- Control register (T8PnC)
- Postscale ratio expand register (T8P1PEX/T8P2PEX)
- Period match control register (T8P1PMC/T8P2PMC)
- Output control register (T8P1OC)

◇ Interrupt and halt

- Timer interrupt flag (T8PnTIF) and period interrupt flag (T8PnPIF)
- Interrupt handler
- In idle mode, the T8Pn stops operating.

6. 1. 2 Block Diagram

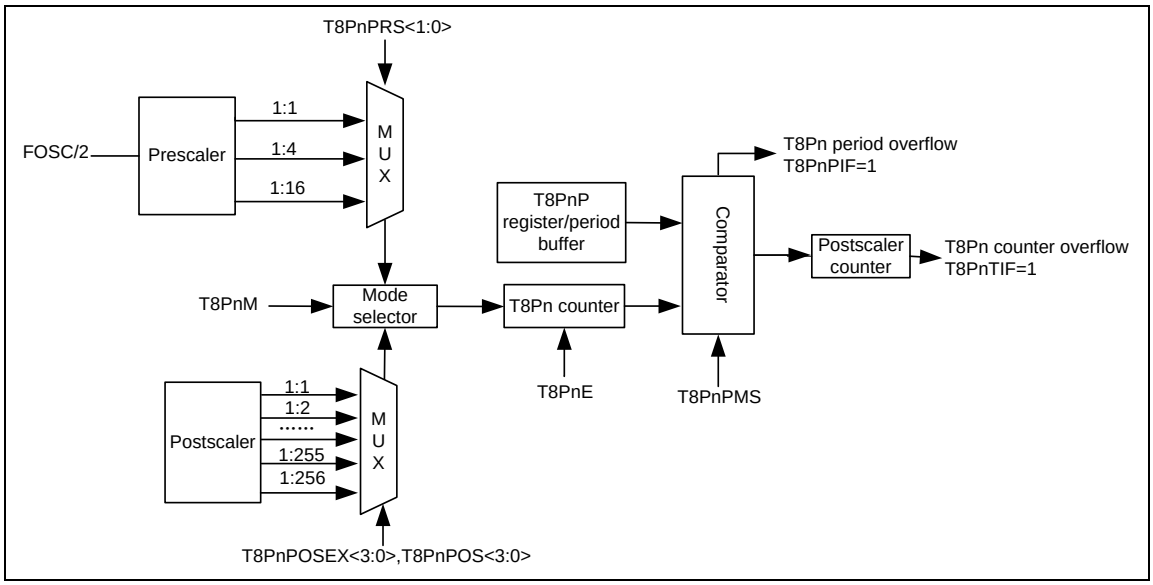


Figure 6-1 T8P1/T8P2 Block Diagram

6. 1. 3 Operating Modes

The 8-bit PWM time-based timer has two operating modes: timer mode and PWM mode, selected by the T8PnM bit of the T8PnC register. The prescaler and postscaler are both available under timer mode and PWM mode. The T8Pn counter clock operates from the Fosc/2.

T8PnM	Operating modes
0	Timer mode
1	PWM mode

Table 6-1 T8Pn Operating Mode Configuration

6. 1. 4 Prescaler and Postscaler

The T8Pn module offers a 4-bit prescaler and an 8-bit configurable postscaler, which can extend the period of an overflow and interrupt. The counter value of the prescaler and postscaler is not read or write accessible. Altering the T8Pn control register or counter register will clear the prescaler and postscaler, but their ratios will not be affected. The T8PnPRS <1:0> bits of the T8PnC register select the prescale ratio in the range 1:1~1:16. The T8PnPOS <3:0> bits of the T8PnC register select the postscale ratio in the range 1:1~1:256.

T8PnPRS<1:0>	T8PnPOSEX<3:0>,T8PnPOS<3:0>	T8Pn match interrupt
00	00000000	Counter and period register match once
00	00000001	Counter and period register match twice
00	00000010	Counter and period register match thrice
00	00000011	Counter and period register match 4 times
00	……	……

T8PnPRS<1:0>	T8PnPOSEX<3:0>,T8PnPOS<3:0>	T8Pn match interrupt
00	11111110	Counter and period register match 255 times
00	11111111	Counter and period register match 256 times
Other values	—	—

Table 6-2 T8P1/T8P2 Postscaler Configuration

6. 1. 5 Timer Mode

When the T8PnM=0 and T8PnE=1, the T8Pn works in timer mode.

In timer mode, the counter clock is sourced from the Fosc/2. Prescaling can be performed on the clock source and the prescaled clock will be the counter clock of the counter.

When the T8PnPMS=0, the T8Pn counter value is compared to the T8PnP value without updating the period buffer PRDBUF; when the T8PnPMS=1, update the PRDBUF with the T8PnP value, and the T8Pn counter value is compared to the PRDBUF value.

When the T8Pn counter value matches the T8PnP value (when T8PnPMS=0) or the PRDBUF value (when T8PnPMS=1), the period interrupt flag T8PnPIF will be set which needs to be cleared by software. Meanwhile, the T8Pn counter will automatically be cleared and restart counting, and the postscaler counter will be incremented. When the postscaler counter value matches the postscale ratio, the postscale will be reset and the timer interrupt flag T8PnTIF will be set which needs to be cleared by software.

The following content gives the description on how the period buffer PRDBUF is updated in timer mode:

On a starting cycle, first write T8PnM = 0 and T8PnPMS= 1, then T8PnE=1, in order to update the PRDBUF with the T8PnP value.

When the starting cycle ends, the period buffer will automatically get updated every time the T8Pn counter value matches the PRDBUF value.

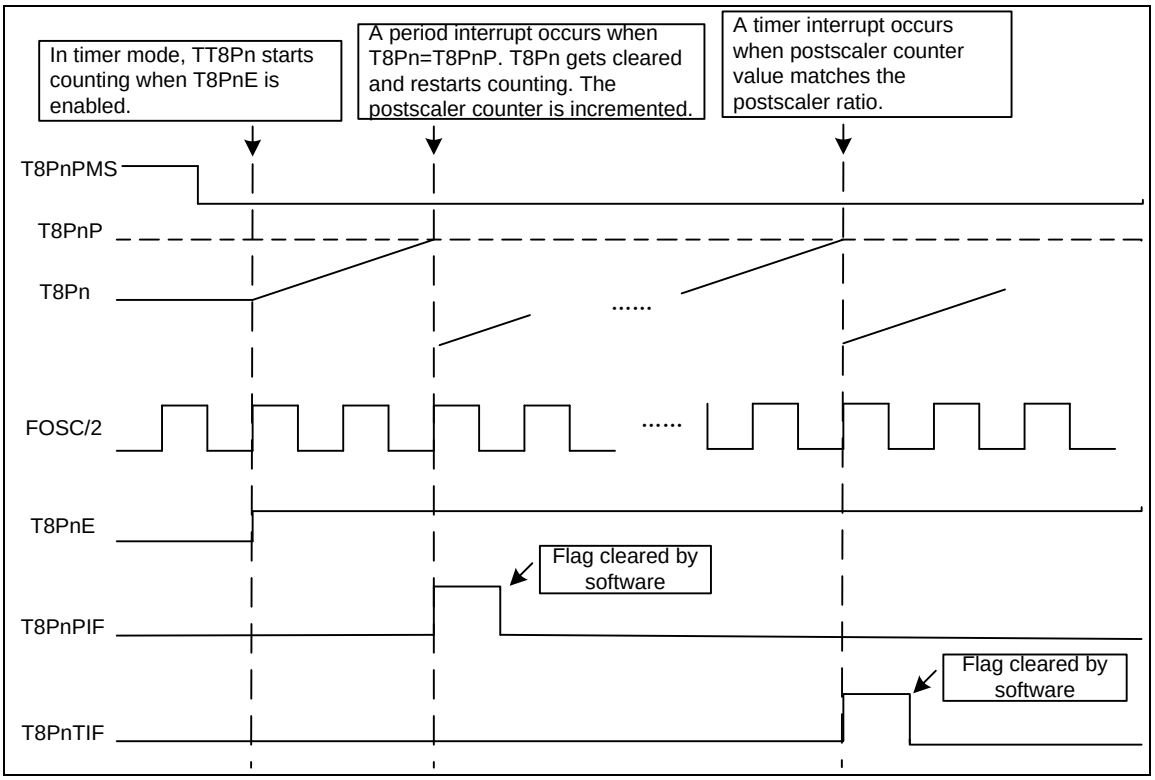


Figure 6-2 T8Pn Timer Mode Timing Diagram

6. 1. 6 PWM Mode

When the T8PnM = 1 and T8PnE = 1, the T8Pn works in PWM mode.

In PWM mode, the counter clock is sourced from the Fosc/2 and the prescaler is available. The setting of the postscaler does not affect the PWM output period or the duty cycle, but only affects the interrupt flag T8PnTIF. See Table 6-3 T8Pn Postscaler Configuration.

The T8PnTRN controls the PWM output.

When the T8PnTRN=1, PWM always outputs 0, and the period buffer PRDBUF or resolution buffer RESBUF will not get updated with the T8PnP value or T8PnR value, respectively.

When the T8PnTRN=0, the PWM output is activated and starts to output 1. The period buffer PRDBUF and resolution buffer RESBUF will get updated with the T8PnP value and T8PnR value, respectively (buffers are not software accessible), and the T8Pn counter then increments from 0. When the T8Pn counter value reaches the RESBUF value, the PWM output changes to 0 and the counter value continues counting up. When the counter value matches the PRDBUF value, the PWM output goes back to 1. Meanwhile, the PRDBUF and RESBUF are again loaded with the T8PnP value and T8PnR value, respectively, and the interrupt flag T8PnPIF is set, which needs to be cleared by software. At the same time, the T8Pn counter gets automatically cleared and restarts counting, and the postscaler is incremented. At this point, a complete PWM cycle is finished and it goes on for a new PWM cycle. When the postscaler counter is

equal to the postscale ratio, the postscaler is reset, and the T8PnTIF is set, which needs to be cleared by software.

The following content gives the description on how the resolution buffer RESBUF and period buffer PRDBUF are updated in PWM mode.

On a starting cycle, first write T8PnM=1, T8PnPMS=1and T8PnE=1, then T8PnTRN=0.

When the starting cycle ends, the period buffer will automatically get updated every time the T8Pn counter value matches the PRDBUF value.

Note1: If the RESBUF value is 0, the PWM output stays at 0 in the current PWM cycle. If the RESBUF is not less than the PRDBUF value, then PWM output stays at 1 in the current PWM cycle.

Note2: On reads of T8PnTRN returns the inverted value of the written value. Writing 0 returns 1 while writing 1 returns 0.

Note3: If the T8PnTRN=1, PWM outputs 0 and the period buffer does not get updated. The PRDBUF value is either the initialized value FF_H or the last updated value when T8PnTRN=0

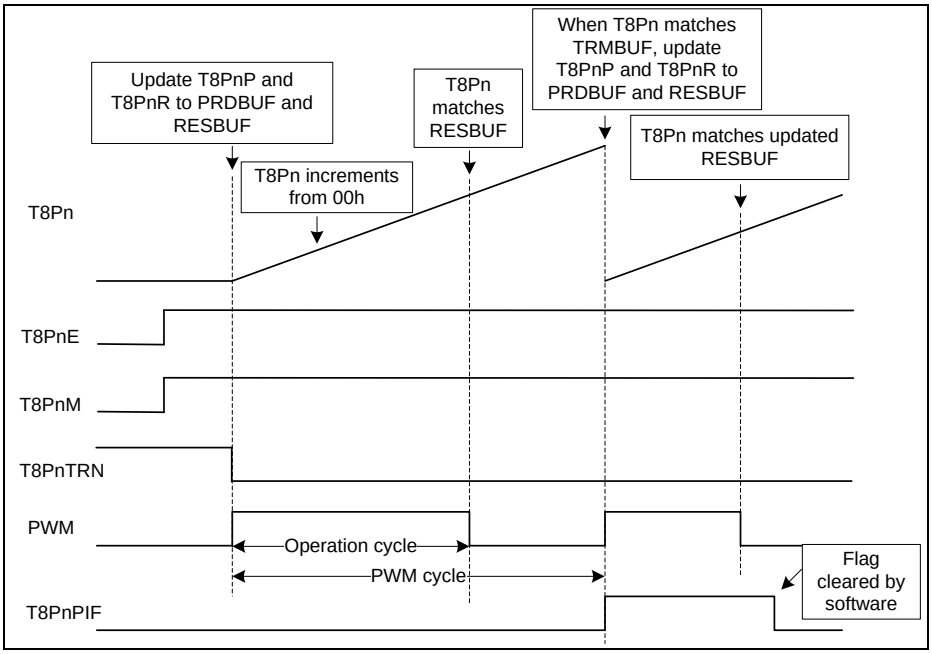


Figure 6-3 T8Pn PWM Mode Timing Diagram

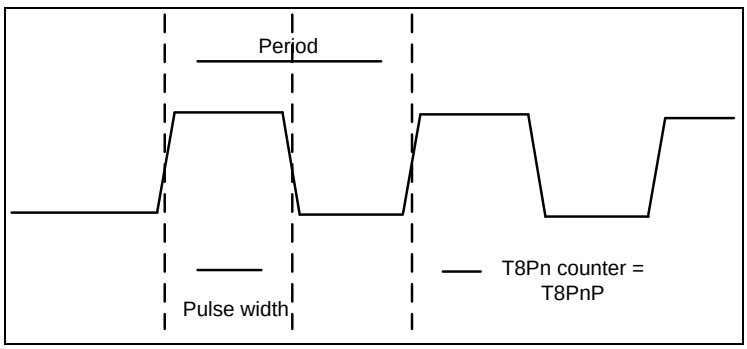


Figure 6-4 PWM Output Diagram

PWM related calculations:

PWM period = [(T8PnP)+1]×2×Tosc×(T8Pn prescale ratio)

PWM frequency = 1/ (PWM period)

When select 9-bit resolution PWM output:
PWM pulse width = (T8PnR×2 +1 + T8PnREX)×Tosc×(T8Pn prescale ratio)
The PWM resolution register T8PnR is an 8-bit register, one expand bit T8PnREX can be added as the lowest bit of the T8PnR. The pulse width depends on the prescale ratio.

When select 8-bit resolution PWM output:
PWM pulse width = (T8PnR +1) ×2×Tosc×(T8Pn prescale ratio)

PWM duty cycle = [PWM pulse width] / [PWM period]

PWM maximum resolution calculation:

$$\mathrm{Re}\,solution = \frac{\log(\frac{Fosc}{Fpwm*[\mathrm{prescale\ ratio}]})}{\log 2}$$

Note: Tosc = 1/Fosc and Fpwm = 1/ (PWM period)

6. 1. 7 PWM Average Resolution

The PWM maximum resolution can be up to 9 bits. Moreover, the PWM average resolution can be further increased through the T8PxRE<1:0> bits (T8PxOC<5:4>), where an LSB is alternately added to the pulse width in continuous output mode, increasing the pulse width by (Tosc x Prescale Ratio).

The resolution expand value can be set to 0, 1/4, 2/4 and 3/4. It is equivalent to further increase the average resolution by 2 bits.

For instance, when the T8PxRE<1:0> selects the 2/4, among 4 pulse widths, 2 will be added an LSB which is distributed evenly over the 4 pulse widths. As shown in the figure below, given the pulse width is n, the average pulse width would be n+1/2, where a relatively high resolution is achieved without increasing the clock frequency.

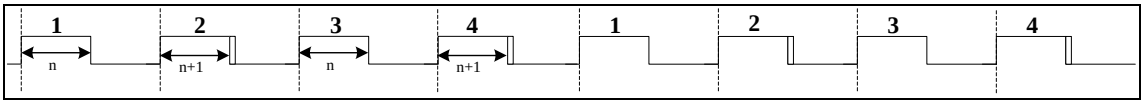


Figure 6-5 PWM Resolution Expanding Diagram

6. 1. 8 PWM Output Pins

T8Pn each has a pair of complementary PWM output pins: PWMn0 andPWMn1, with configurable dead-band time set by the T8PnPDT register.

PWM dead-band time = T8PnPDT<7:0> x Tosc

T8PnPEN<1:0> and T8PnNEN<1:0> of the T8PnOC register select the PWM output pins.

The output polarity can be set through the ANS<7:6> (PWM20NS and PWM10NS).

Note that, prior to enabling the PWM output, set the I/O pin associated with the PWM to output mode, or else no PWM waveform will be output.

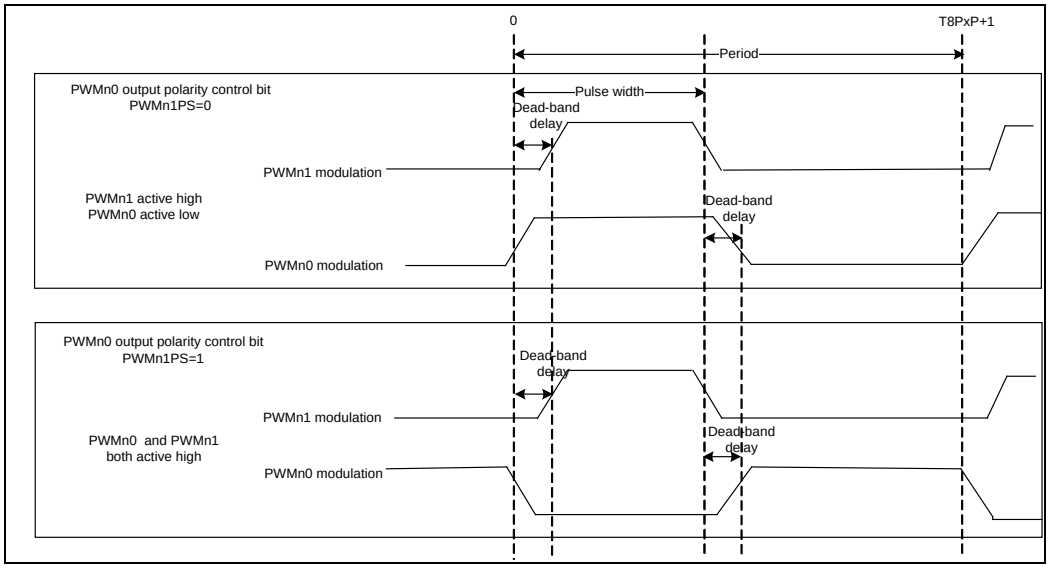


Figure 6-6 Complementary PWM Outputs with Dead-band Diagram

6. 1. 9 Special Function Registers

T8Pn:T8Pn Counter (T8P1/T8P2)								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	T8Pn <7:0>							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 T8Pn <7:0>:T8Pn counter value, 00_H ~FF_H

T8PnP: T8Pn Period Register (T8P1P/T8P2P)								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	T8PnP < 7:0>							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	1	1	1	1	1	1	1	1

Bit 7~0 T8PnP < 7:0>: PWM period value

T8PnR:T8Pn Resolution Register (T8P1R/T8P2R)								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	T8PnR <7:0>							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 T8PnR <7:0>: resolution value

T8PnC:T8Pn Control Register (T8P1C/ T8P2C)								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	T8PnM	T8PnPOS<3:0>				T8PnE	T8PnPRS<1:0>	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 T8PnM:T8Pn operating mode select bit
0: Timer mode
1: PWM mode

Bit 6~3 T8PnPOS<3:0>:T8Pn postscale ratio select bits
0000: 1:1
0001: 1:2
0010: 1:3
…
1111: 1:16
The 8-bit postscale ratio consits of two parts, upper 4 bit from the T8PnPEX register and lower 4 bits from the T8PnPOS <3:0> bits. A prescale ratio can be selected from the range 1:1 ~ 1:256.

Bit 2 T8PnE:T8Pn module enable bit
0: Disabled
1: Enabled

Bit 1~0 T8PnPRS<1:0>:T8Pn prescale ratio select bits
00: 1:1
01: 1:4
1x: 1:16

T8PnPEX:T8Pn Postscaler Expand Register (T8P1PEX/T8P2PEX)								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	—	—	—	—	T8PnPOSEX<3:0>			
R/W	—	—	—	—	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~4 Not in used

Bit 3~0 T8PnPOSEX<3:0>: postscaler ratio expand bits (upper 4 bits)

T8PnPMC:T8Pn Period Match Control Register (T8P1PMC/T8P2PMC)								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	—	—	—	—	—	—	T8PnRS	T8PnPMS
R/W	—	—	—	—	—	—	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~2 Not in used

Bit 1 T8PnRS: PWM resolution select bit
1: 9-bit resolution
0: 8-bit resolution

Bit 0 T8PnPMS: Period match select bit in timer mode

0: Compare the T8Pn counter value to the T8PnP value
1: Compare the T8Pn counter value to the PRDBUF value

T8P1OC:T8P1 Output Control Register								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	T8P1TRN	T8P1REX	T8P1RE<1:0>		T8P1NEN<1:0>		T8P1PEN<1:0>	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 T8P1TRN: PWM output enable bit
1: Disabled (Resets output and counter)
0: Enabled (Outputs PWM waveform)
Bit 6 T8P1REX: Resolution expand bit in PWM mode
Bit 5~4 T8P1RE<1:0>:T8P1 PWM1 average resolution expand select bits
00:0
01:1/4
10:2/4
11:3/4
Bit 3~2 T8P1NEN<1:0>:T8P1 PWM1 complementary output pin select bits
00:PWM10 output disabled
01:PA2 outputs PWM10
10:PB1 outputs PWM10
11:PB3 outputs PWM10
Bit 1~0 T8P1PEN<1:0>:T8P1 PWM1 output pin select bits
00:PA1 outputs PWM11
01:PB0 outputs PWM11
10:PA6 outputs PWM11
11:PB2 outputs PWM11

T8P2OC:T8P2 Output Control Register								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	T8P2TRN	T8P2REX	T8P2RE<1:0>		T8P2NEN<1:0>		T8P2PEN<1:0>	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 T8P2TRN: PWM output enable bit
1: Disabled (Resets output and counter)
0: Enabled (Outputs PWM waveform)
Bit 6 T8P2REX: Resolution expand bit in PWM mode
Bit 5~4 T8P2RE<1:0>:T8P2 PWM2 average resolution expand select bits
00:0
01:1/4
10:2/4
11:3/4
Bit 3~2 T8P2NEN<1:0>:T8P2 PWM2 complementary output pin select bits
00:PWM20 output disabled

01:PB0 outputs PWM20
10:PA6 outputs PWM20
11:PB2 outputs PWM20

Bit 1~0 T8P2PEN<1:0>:T8P2 PWM2 output pin select bits
00:PA2 outputs PWM21
01:PB1 outputs PWM21
10:PB3 outputs PWM21
11:PWM21 output disabled

T8PnPDT:T8Pn PWM Dead-band Time Register								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	T8PnPDT <7:0>							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 T8PnPDT <7:0>: PWM dead-band time = T8PnPDT x Tosc

6. 2 Analog-to-Digital Converter (ADC)

6. 2. 1 Overview

The chip features a 12-bit ADC. The ADC is connected to a 6-channel analog multiplexer. Analog signals are first input from the multiplexer, followed by a sample-hold circuit, then go to the ADC. The 12-bit conversion result in binary is stored in ADCRH and ADCRL.

◇ ADC Features

- 12-bit resolution
- 6 analog input channels + 2 power supply detection channels
- Data alignment: right-aligned or left-aligned
- External and internal reference voltage options
- Power supply detection, selectable voltage division rate
- Configurable AD conversion clock frequency
- Clock source: Fosc

◇ Main Function Registers

- ADC result register (ADCRL,ADCRH)
- ADC control register (ADCCL,ADCCH)
- Analog port select register (ANSL,ANSH)
- ADC trigger register (ADCTR)

◇ Interrupt

- AD conversion interrupt(ADIE/ADIF)

6. 2. 2 Block Diagram

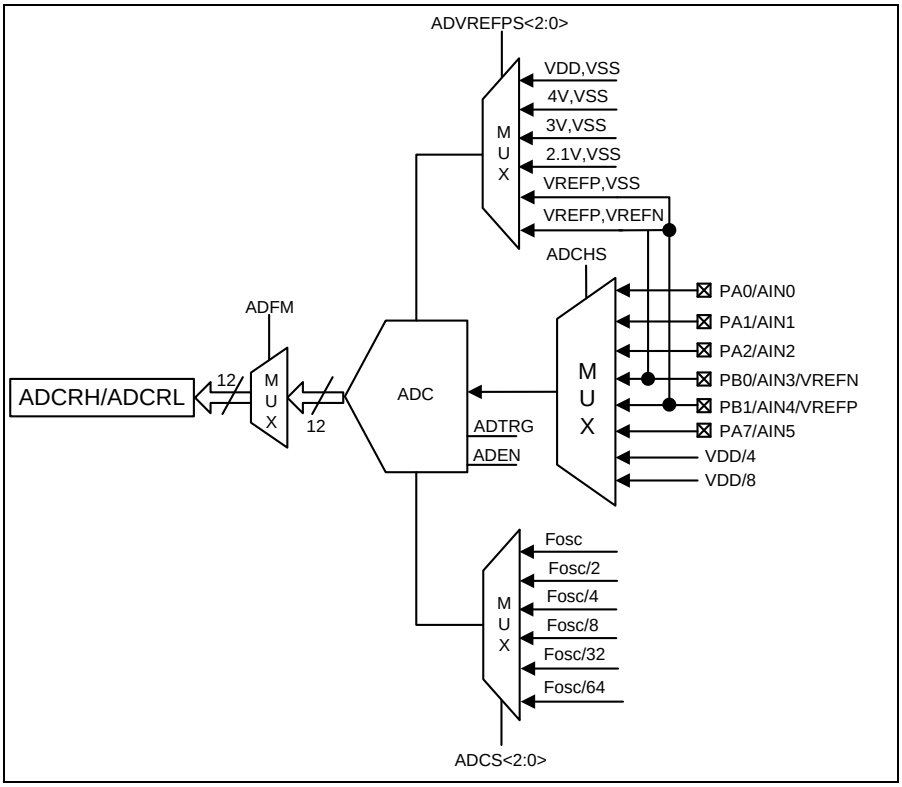


Figure 6-7 ADC Block Diagram

6. 2. 3 ADC Configuration

In order to obtain an accurate conversion result, ADC must be correctly configured.

Clock

7 conversion clocks are available, Fosc ~ Fosc/64 and INTLRC, selected by the ADCCH register.

Reference Voltage

The ADC circuit uses a positive reference voltage and a negative reference voltage, corresponding to the external input pins VPREFP and VREFN, respectively. These two pins are also multiplexed with port B and analog channels. Prior to using the pins as external reference inputs, set them to the proper mode through the ANS register. The positive reference voltage can be selected as VDD, 4V, 3V, 2.1V or the VREFP input, and the negative reference voltage can be selected as VSS or the VREFN input, by ADVREFS <2:0> bits. If the 2.1V is used as the positive reference, select the correct AD 2.1V calibration information by the AD2VCALS bit depending on the used VDD.

Sampling Time

The sampling time is selected by the ADST<3:0> of the ADCCH register, offering 1 ~15 options (Sampling time = 1 ~ 15 x Tadclk).

Multiplexed Port

All analog input channels AINn and reference voltage input pins are multiplexed with PA/PB. All associated pins must be set to analog mode through ANS register before using the ADC.

Analog Input Channel

The ADC supports 6 analog input channels AIN0~AIN5 and 2 power supply detection channels, VDD/4 and VDD/8. The analog channel must be selected before using the ADC by ADCHS <2:0> bit of the ADCCL register.

Data Alignment

Two data alignments are available for conversion results, left-aligned and right-aligned. The ADFM bit in the ADCCH register is used for the alignment selection.

AD Coversion Trigger Event

An AD conversion can be triggered by software or PWM auto-conversion.

When the ADEN bit is enabled, set the conversion trigger bit ADTRG to 1 using software to start a conversion. When both of the ADEN bit and the TRIGEN bit are enabled, the specified the PWM trigger edge will automatically set the ADTRG bit to 1 to start a conversion.

An auto-conversion trigger source is a PWMn1 signal, selected by the TRIGS bit. The trigger edge can either be a PWM rising edge or falling edge, selected by the TRIGPEG bit.

Note that, before using the PWM auto-conversion, poll the status of the ADTRG bit. If the ADTRG bit is 1, the PWM trigger edge will be ignored until the ADTRG bit changes to 0.

After that, when a PWM trigger edge is again detected, an AD conversion will then be automatically triggered.

6. 2. 4 ADC Conversion Steps

The following description list each step of the ADC conversion.

Step 1: Select the ADC conversion clock through the ADCS<2:0> bits of the ADCCH register.

Step 2: Select the ADC reference voltage source through the ADVREFS bits of the ADCCL register.

Step 3: Select the ADC sampling time through the ADST <3:0> bits of the ADCCH register.

Step 4: Set the ADC associated pins to analog mode through ANS register..

Step 5: Select the analog input channel AINx through the ADCHS <2:0> bits of the ADCCL register.

Step 6: Select the data alignment through the ADFM bit in the ADCCH for the conversion result.

Step 7: If interrupts are to be used, interrupt control registers must be correctly configured to activate the ADC interrupt function. In the default interrupt mode, the Global Interrupt Enable bit GIE needs to be set to 1, and ADC interrupt enable bit also needs to be set to1.

Step 8: Enable the ADC circuit by setting the ADEN to 1 in ADCCL.

Step 9: Select a trigger mode, software trigger or PWM trigger. If the software trigger is selected, set the ADTRG bit to 1 to start a AD conversion. If PWM auto-conversion is selected, configure the TRIGS bit to select a trigger source, configure the TRIGPEG to select a trigger edge and then enable the TRIGEN bit. In auto-conversion mode, the specified trigger edge will automatically set the ADTRG bit to 1 to activate the conversion.

Step 10: Poll the ADTRG bit in the ADCCL register to determine whether the conversion is completed.

Step 11: Read the conversion result in ADCRH and ADCRL register

6. 2. 5 ADC Timing

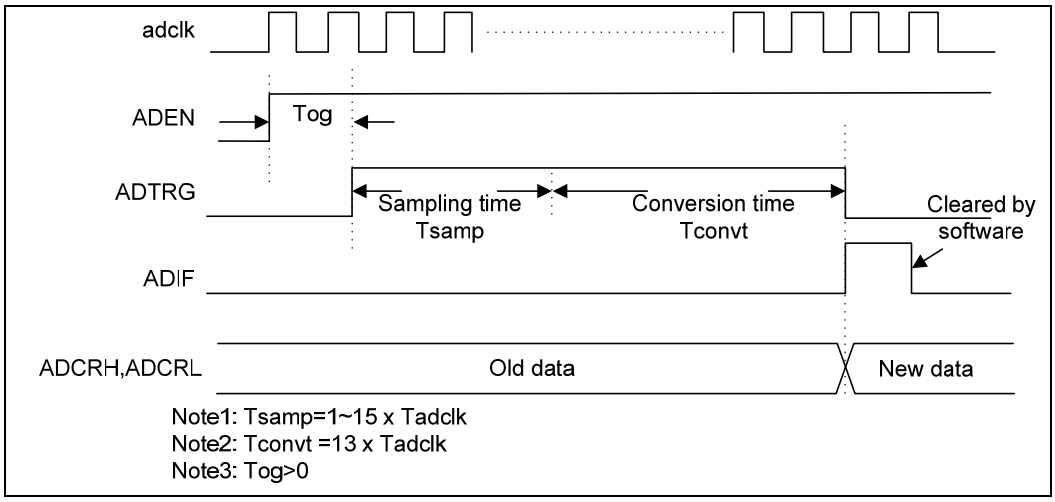


Figure 6-8 ADC Timing Diagram

6. 2. 6 Application Example

Application example: AD conversion on analog channel 0 (AIN0)

```
BCC     ANS,0           ;Set AIN0 pin to analog mode
BCC     ADCCH, ADFM     ; Result in right alignment
MOVI    0X01
MOVA    ADCCL           ; Enable ADC and select channel 0
BSS     ADCCL, ADTRG    ; Trigger AD conversion
AD_WAIT:
JBC     ADCCL, ADTRG    ; Wait for AD conversion to complete
GOTO    AD_WAIT
MOV     ADCRH, 0        ; Read high byte of the result
… …
MOV     ADCRL, 0        ; Read low 4 bits of the result
… …
```

6. 2. 7 Special Function Registers

ADFM	ADCRH: ADC Result High Byte								ADCRL:ADC Result Low Byte							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1	—	—	—	—	ADCR<11:8>				ADCR<7:0>							
0	ADCR<11:4>								ADCR<3:0>				—	—	—	—

ADCR<11:0>: ADC conversion result

ADCCL: ADC Control Register Low Byte								
Bit	7	6	5	4	3	2	1	0
Name	ADVREFS<2:0>			ADCHS<2:0>			ADTRG	ADEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~5 ADVREFS <2:0>: Reference source select bits
000: positive input VDD, negative input VSS
001: positive input 4.0V, negative input VSS
010: positive input 3.0V, negative input VSS
011: positive input 2.1V, negative input VSS
100: positive input external VREFP, negative input VSS
101: positive input external VREFP, negative input VREFN
Others: Reserved

Bit 4~2 ADCHS <2:0>: Analog channel select bits
000: Channel 0(AIN0)
001: Channel 1(AIN1)
010: Channel 2(AIN2)
011: Channel 3(AIN3)
100: Channel 4(AIN4)
101: Channel 5(AIN5)
110: VDD/4
111: VDD/8

Bit 1 ADTRG: ADC trigger bit
0: AD conversion not yet started or complete
1: conversion in progress. Set 1 to start the AD conversion

Bit 0 ADEN:ADC enable bit
0: Disabled
1: Enabled

ADCCH: ADC Control Register High Byte								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	ADFM	ADCS<2:0>			ADST<3:0>			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	1	0	0	0

Bit 7 ADFM: ADC data format select bit
0: Right alignment (ADCRH<7:0>, ADCRL<7:4>)
1: Left alignment (ADCRH<3:0>, ADCRL<7:0>)

Bit 6~4 ADCS <2:0>: AD conversion clock select bits
000:Fosc
001:Fosc/2
010:Fosc/4
011:Fosc/8
100:Fosc/16
101:Fosc/32
110:Fosc/64
111: Reserved

Bit 3~0 ADST <3:0>: AD sampling time select bits
0000: Prohibited
0001~1111: corresponds to 1~15 ADC clock(s) (by default 8)

ADCTR: ADC Trigger Register								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	—	TRIGS	TRIGPEG	TRIGEN	—	—	—	AD2VCALS
R/W	—	R/W	R/W	R/W	—	—	—	R/W
POR	0	0	0	0	0	0	0	0

Bit 7, 3~1 Not in used

Bit 6 TRIGS: Auto-conversion trigger source select bit
0: PWM11
1: PWM21

Bit 5 TRIGPEG: PWM trigger edge select bit
0: PWM rising edge
1: PWM falling edge

Bit 4 TRIGEN: PWM trigger enable bit
0: Disabled
1: Enabled

Bit 0 AD2VCALS: AD positive reference 2.1V calibration select bit
0: AD positive reference 2.1V calibration value at VDD=5V
1: AD positive reference 2.1V calibration value at VDD=3V

6. 3 Low Voltage Detection Module (LVD)

6. 3. 1 Overview

The device features a low voltage detection module LVD, monitoring the power supply VDD. In the case that the power supply is not stable, for instance, with the power supply noise and crosstalk present or under EMS test condition, the power supply will violently fluctuate, and VDD might be lower than the operating voltage if it has not been stabilized. If the detected voltage is lower than the preset threshold value, a warning signal will be prompted. The low voltage detection can also generate interrupts.

6. 3. 2 LVD Operation

The LVD is enabled by setting the LVDEN bit to high, and disabled by clearing the LVDEN bit of the LVDC register. The LVD module compares the VDD with the preset threshold voltage and the comparison result can be polled through LVDLS bit of the LVDC register. The threshold voltage is configured through LVDV<1:0> of the LDVC in the range 2.1V~3.6V. If VDD is lower than the threshold voltage, the LVDLS bit will be set to 1, indicating a low voltage has been detected, the LVD interrupt flag will be set. An LVD interrupt request will be generated if the LVD interrupt enable bit is set.

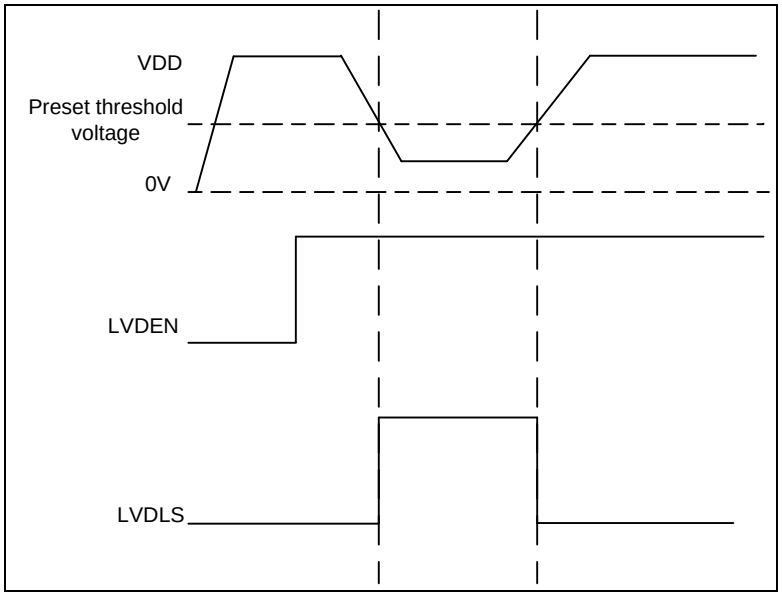


Figure 6-9 LVD Operation Timing Diagram

6. 3. 3 Special Function Registers

LVDC: LVD Control Register								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	LVDLS	—	—	LVDEN	—	—	LVDV<1:0>	
R/W	R	—	—	R/W	—	—	R/W	R/W
POR	0	0	0	1	0	0	0	0

Bit 7 LVDLS: LVD status bit
0: VDD > preset threshold voltage
1: VDD < preset threshold voltage

Bit 6~5,3~2 Not in used

Bit 4 LVDEN: LVD enable bit
0: Disabled
1: Enabled

Bit 2~0 LVDV<1:0>: LVD voltage select bits
00: 2.1V
01: 2.4V
10: 3.0V
11: 3.6V

Chapter7 Interrupts

7. 1 Overview

An interrupt can wake up from the idle mode, as well as allow the system to respond unexpected events during normal operation by suspending the current activities, saving its state, jumping to the entry address of interrupt service routine and executing the corresponding interrupt service routine to deal with the unexpected events. Only the default interrupt mode is available, with up to 12 interrupt sources, 1 software interrupt and 11 hardware interrupts.

7. 2 Block Diagram

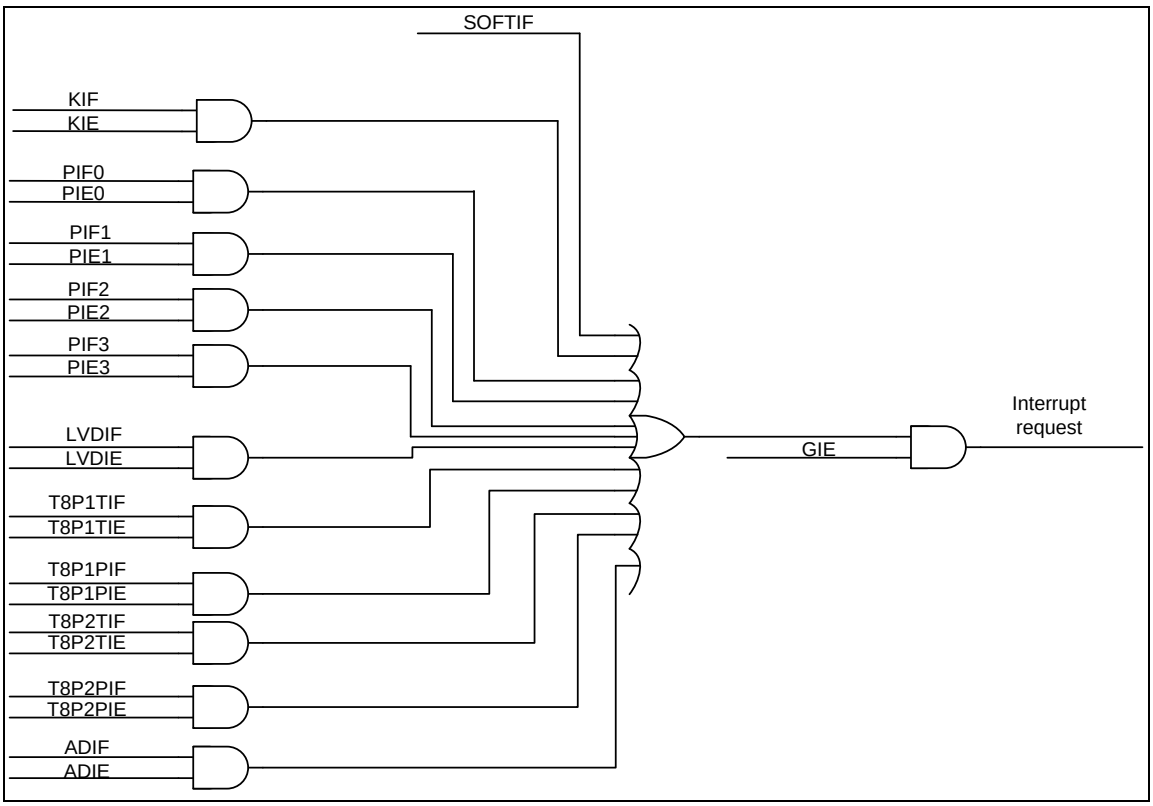


Figure 7-1 Interrupt Logic Diagram

7. 2. 1 Default Interrupt Mode

In default interrupt mode, all interrupt vectors locate at entry address 0004_H. Users determine the interrupt source in order to execute the corresponding interrupt service subroutine by checking the interrupt flag bits and interrupt enable bits through the ISR (interrupt service routine).

No.	Interrupt name	Interrupt flag	Interrupt mask	Interrupt enable	Global interrupt enable	Entry address
1	Software interrupt	SOFTIF	-	-	GIE	004_H
2	KINT0	KIF	KMASK0	KIE	GIE	
	KINT1		KMASK1			
	KINT2		KMASK2			
	KINT3		KMASK3			
	KINT4		KMASK4			
	KIN5		KMSK5			
	KIN6		KMSK6			
	KIN7		KMSK7			
3	PINT0	PIF0	-	PIE0	GIE	
4	PINT1	PIF1	-	PIE1	GIE	
5	PINT2	PIF2	-	PIE2	GIE	
6	PINT3	PIF3	-	PIE3	GIE	
7	LVDINT	LVDIF	-	LVDIE	GIE	
8	T8P1TINT	T8P1TIF	-	T8P1TIE	GIE	
9	T8P1PINT	T8P1PIF	-	T8P1PIE	GIE	
10	T8P2TINT	T8P2TIF	-	T8P2TIE	GIE	
11	T8P2PINT	T8P2PIF	-	T8P2PIE	GIE	
12	ADINT	ADIF	-	ADIE	GIE	

Table 7-1 Default Interrupt Mode Table

7. 3 Context Saving

Push and pop instructions are used to save and restore the current state of some registers, including the A, PSW, IAA and PCRH registers. Save and restore the data of other registers by using instructions. Two continuous push operations can be performed but the third push will overwrite the first pushed value. Similarly, the third pop might restore an unexpected data.

7. 4 Interrupt Operation

Each hardware interrupt source has its own corresponding interrupt enable bit and interrupt flag bit. On initializing a hardware interrupt, there is a need to clear the corresponding interrupt flag first and then enable the interrupt, or else it may enter the interrupt by mistake. After initializing the specific interrupt, enable the global interrupt bit.

If an interrupt condition occurs, the corresponding interrupt flag will be set. The following conditions must exist for the program to jump to the address of the corresponding service routine after the interrupt is set.

1. When the interrupt enable bit is 1, determine whether the second condition is true;

when the interrupt enable bit is 0, even if the interrupt flag bit is 1, the interrupt will never occur and the program will not jump to the address of the corresponding interrupt service routine.

2. If the global interrupt enable bit GIE is cleared, it will mask all interrupt requests. Only when the GIE bit is set, the program will jump to the address of the corresponding interrupt service routine.

7. 4. 1 External Port Interrupt

When a PINTn pin is configured as a digital input, if the input change meets the trigger condition, an external interrupt PINTn will occur and the corresponding interrupt flag PIFn will be set. When the GIE and PIEn are both set, an external interrupt request will be sent to CPU. The system will jump to the entry address of the corresponding interrupt service routine to handle the interrupt.

Note that the interrupt flag bit PIFn and interrupt enable bit PIEn need to be cleared by software. The PEGn bit of the INTC1 register is used to set a trigger edge, including rising edge and falling edge.

7. 4. 2 External Key Interrupt

When a KINn pin is configured as a digital input, if the input level of any unmasked key changes, the interrupt flag bit KIF will be set. When the GIE and the external key interrupt enable bit KIE are both set, an external key interrupt request will be sent to CPU. The system will jump to the entry address of the corresponding interrupt service routine to handle the interrupt.

When an external key interrupt is required, configure the corresponding control register and enable the internal pull-up resister of the associated port.

Before enabling the key interrupt (KMSKn=1, KIE=1), read or write the port register, clearing the interrupt flag to avoid unwanted interrupts.

Clear the interrupt flag bit KIF by the following steps.

1) Read or write the port register and clear the mismatching between the pin level and the latch register;

2) Clear the interrupt flag bit KIF by software.

The interrupt enable bit KIE also needs to be cleared by software.

7. 4. 3 T8Pn (T8P1/T8P2) Timer Interrupt

In both timer and PWM mode, an 8-bit T8Pn counter counts up. When the postscaler counter value matches the postscale ratio, the corresponding interrupt flag T8PnTIF will be set. When the GIE bit and the timer interrupt enable bit T8PnTIE are both set, an interrupt request will be sent to CPU. The system will jump to the entry address of the corresponding interrupt service routine to handle the interrupt. Note that, the interrupt flag T8PnTIF and the interrupt enable bit T8PnTIE both need to be cleared by software.

7. 4. 4 T8Pn (T8P1/T8P2) Period Interrupt

In both timer and PWM mode, an 8-bit T8Pn counter counts up. When the T8Pn counter value matches the T8PnP register value (in PWM mode, the T8Pn counter increments from 0), a period interrupt will occur, and the corresponding interrupt flag T8PnPIF will be set. When the GIE bit and the interrupt enable bit T8PnPIE are both set, an interrupt request will be sent to CPU. The system will jump to the entry address of the corresponding interrupt service routine to handle the interrupt. Note that, the interrupt flag T8PnPIF and the interrupt enable bit T8PnPIE both need to be cleared by software.

7. 4. 5 ADC Interrupt

When a conversion completes, an ADC interrupt will occur, and the ADC interrupt flag ADIF will be set. When the GIE bit and the interrupt enable bit ADIE are both set, an interrupt request will be sent to CPU. The system will jump to the entry address of the corresponding interrupt service routine to handle the interrupt. Note that, the interrupt flag ADIF and the interrupt enable bit ADIE both need to be cleared by software.

7. 4. 6 LVD Interrupt

When VDD is less than the threshold voltage set by the LVDC register, an interrupt will occur on the trigger edge specified by the LVDLS bit, and the interrupt flag LVDIF will be set. When the GIE bit and the interrupt enable bit LVDIE are both set, an interrupt request will be sent to CPU. The system will jump to the entry address of the corresponding interrupt service routine to handle the interrupt. Note that, the interrupt flag LVDIF and the interrupt enable bit LVDIE both need to be cleared by software.

7. 4. 7 Interrupt Operation Considerations

To avoid any unwanted interrupts, users are required to clear the corresponding interrupt flags before enabling the desired interrupts.

Except for read-only interrupt flags which are cleared by hardware, all other interrupt flags are cleared by software.

7. 5 Special Function Registers

INTF0: Interrupt Flag Register 0								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	T8P2PIF	T8P1PIF	ADIF	LVDIF	—	T8P2TIF	T8P1TIF	KIF
R/W	R/W	R/W	R/W	R/W	—	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 T8P2PIF:T8P2 period interrupt flag bit
0: T8P2 counter value did not match the period count.
1:T8P2 counter value matched the period count. (Must be cleared by software)

Bit 6 T8P1PIF:T8P1 period interrupt flag bit
0: T8P1 counter value did not match the period count.
1:T8P1 counter value matched the period count. (Must be cleared by software)

Bit 5 ADIF: ADC interrupt flag bit
0: AD conversion not started or in progress
1: AD conversion completed (must be cleared by software)

Bit 4 LVDIF: LVD interrupt flag bit
0: VDD was not less than the preset threshold voltage
1: VDD was less than the preset threshold voltage (must be cleared by software)

Bit 3 Not in used

Bit 2 T8P2TIF:T8P2 timer interrupt flag bit
0:T8P2 postscaler counter value did not match the postscale ratio.
1:T8P2 postscaler counter value matched the postscale ratio (must be cleared by software)

Bit 1 T8P1TIF:T8P1 timer interrupt flag bit
0:T8P1 postscaler counter value did not match the postscale ratio.
1:T8P1 postscaler counter value matched the postscale ratio (must be cleared by software)

Bit 0 KIF: External key interrupt flag bit
0: None of the key input pins have changed state
1: At least one of the key input pins changed state (must be cleared by software)

INTE0: Interrupt Enable Register 0								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	T8P2PIE	T8P1PIE	ADIE	LVDIE	—	T8P2TIE	T8P1TIE	KIE
R/W	R/W	R/W	R/W	R/W	—	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 T8P2PIE:T8P2 period interrupt enable bit
0: Disabled
1: Enabled

Bit 6 T8P1PIE:T8P1 period interrupt enable bit
0: Disabled

1: Enabled

Bit 5 ADIE: ADC interrupt enable bit
0: Disabled
1: Enabled

Bit 4 LVDIE: LVD interrupt enable bit
0: Disabled
1: Enabled

Bit 3 Not in used

Bit 2 T8P2TIE:T8P2 timer interrupt enable bit
0: Disabled
1: Enabled

Bit 1 T8P1TIE:T8P1 timer interrupt enable bit
0: Disabled
1: Enabled

Bit 0 KIE: External key interrupt enable bit
0: Disabled
1: Enabled

INTF1: Interrupt Flag Register 1

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	PIF3	PIF2	PIF1	PIF0
R/W	—	—	—	—	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~4 Not in used

Bit 3 PIF3:PINT3 interrupt flag bit
0: No interrupt signal was on the PINT3 pin.
1: There was an interrupt signal on the PINT3 pin (must be cleared by software)

Bit 2 PIF2:PINT2 interrupt flag bit
0: No interrupt signal was on the PINT2 pin.
1: There was an interrupt signal on the PINT2 pin (must be cleared by software)

Bit 1 PIF1:PINT1 interrupt flag bit
0: No interrupt signal was on the PINT1 pin.
1: There was an interrupt signal on the PINT1 pin (must be cleared by software)

Bit 0 PIF0:PINT0 interrupt flag bit
0: No interrupt signal was on the PINT0 pin.
1: There was an interrupt signal on the PINT0 pin (must be cleared by software)

INTE1:Interrupt Enable Register 1

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	PIE3	PIE2	PIE1	PIE0
R/W	—	—	—	—	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~4 Not in used

Bit 3 PIE3:PINT3 interrupt enable bit

0: Disabled
1: Enabled

Bit 2 PIE2:PINT2 interrupt enable bit
0: Disabled
1: Enabled

Bit 1 PIE1:PINT1 interrupt enable bit
0: Disabled
1: Enabled

Bit 0 PIE0:PINT0 interrupt enable bit
0: Disabled
1: Enabled

INTC0: Interrupt Control Register 0

Bit	7	6	5	4	3	2	1	0
Name	KMSKn<7:0>							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 KMSKn<7:0>: KINn key input mask bit
0: Masked
1: Not masked

INTC1: Interrupt Control Register 1

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	PEG3	PEG2	PEG1	PEG0
R/W	—	—	—	—	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~4 Not in used

Bit 3 PEG3:PINT3 trigger edge select bit
0:PINT3 falling edge
1:PINT3 rising edge

Bit 2 PEG2:PINT2 rigger edge select bit
0:PINT2 falling edge
1:PINT2 rising edge

Bit 1 PEG1:PINT1 rigger edge select bit
0:PINT1 falling edge
1:PINT1 rising edge

Bit 0 PEG0:PINT0 rigger edge select bit
0:PINT0 falling edge
1:PINT0 rising edge

PINTS: External Port Interrupt Select Register								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	PINT3S<1:0>		PINT2S<1:0>		PINT1S<1:0>		PINT0S<1:0>	
R/W	W	W	W	W	W	W	W	W
POR	0	0	0	0	0	0	0	0

Bit 7~6 PINT3S<1:0>:PINT3 interrupt source select bits
00:PA7
01:PA5
10:PB3
11: Reserved

Bit 5~4 PINT2S<1:0>:PINT2 interrupt source select bits
00:PA6
01:PA4
10:PB2
11: Reserved

Bit 3~2 PINT1S<1:0>:PINT1 interrupt source select bits
00:PA1
01:PA3
10:PB1
11:PB5

Bit 1~0 PINT0S<1:0>:PINT0 interrupt source select bits
00:PA0
01:PA2
10:PB0
11:PB4

Note: This PINTS register is write-only and not readable; therefore it needs to be operated with the MOVA and MOVAR instructions.

INTG: Global Interrupt Register								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GIE	—	—	—	—	—	SOFTIF	—
R/W	R/W	—	—	—	—	—	R/W	—
POR	0	0	0	0	0	0	0	0

Bit 7 GIE: Global interrupt enable bit
0: Disable all interrupts
1: Enable all unmasked interrupts

Bit 6~2,0 Not in used

Bit 1 SOFTIF: Software interrupt flag bit
0: No software interrupt occurred
1: Software interrupt occurred

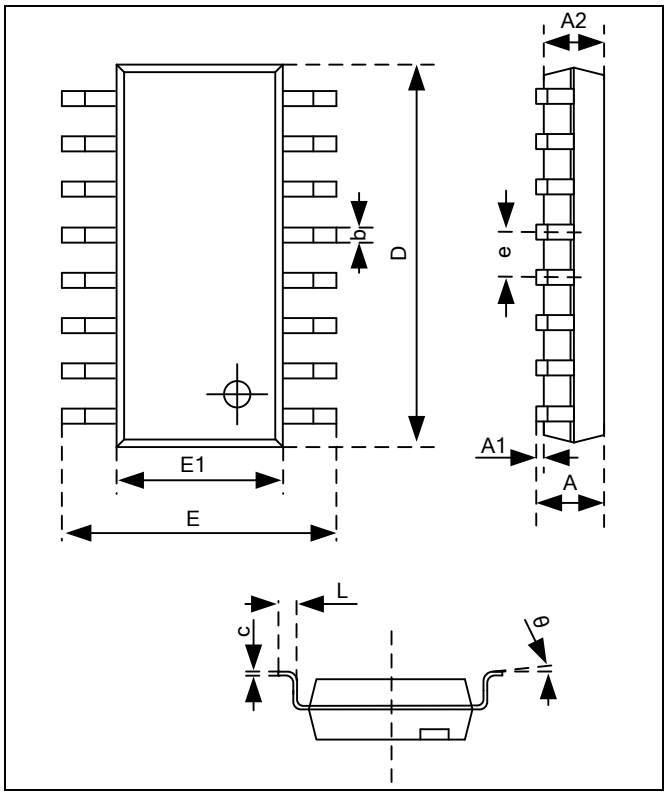
Chapter8 Configuration Word

Register name	Configuration word (CFG_WD)	
Address	$7F2_H$	
OSCS<2:0>	bit2-0	Oscillator select bits 000: LP mode, connect the crystal/resonator to PA4 and PA5 001: Reserved 010: HS mode, connect the crystal oscillator to PA4 and PA5 011: Reserved 100: XT mode: connect the crystal oscillator to PA4 and PA5 101: Reserved 110: INTOSCO mode: PA4 outputs the CLKO and PA5 is an I/O pin. 111: INTOSC mode: PA4 and PA5 are I/O pins
WDTEN	bit3	Hardware watchdog enable bit 0: Disabled 1: Enabled
PWRTEB	bit4	Power up timer enable bit 0: Enabled 1: Disabled
MRSTEN	bit5	MRSTN pin enable bit 0: Digital input 1: Enabled for the external reset
—	bit7-6	Reserved, default to 1
BORVS<1:0>	bit9-8	BOR enable and threshold voltage select bits 00: Disabled 01: Enabled, threshold voltage 2.2V 10: Enabled, threshold voltage 2.7V 11: Reserved
-	bit10	Reserved, default to 1
-	bit15-11	Reserved, default to 0

Note: CLKO is the system clock output divided by 16.

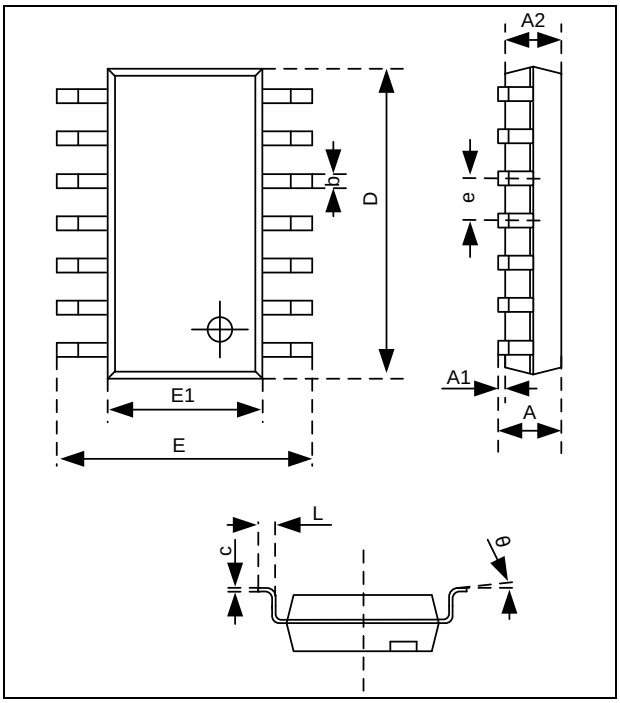
Chapter9 Packaging Information

9. 1 SOP16 Package Drawing



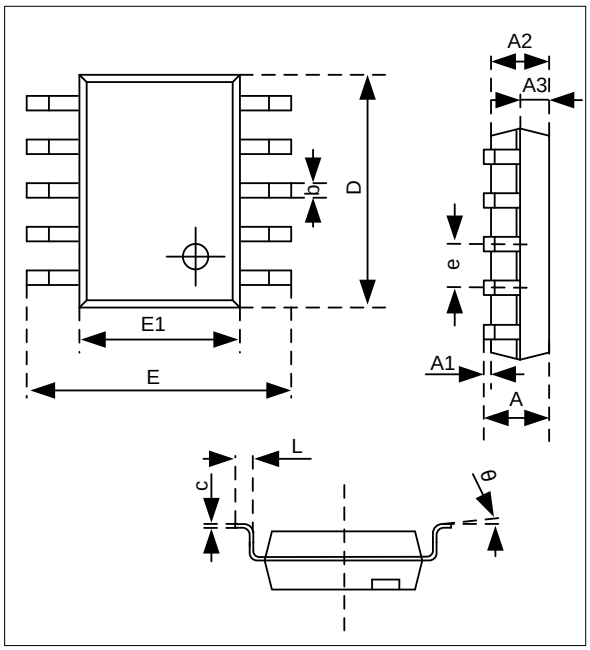
Symbol	（mm）		
	MIN	NOM	MAX
A	—	—	1.77
A1	0.08	0.18	0.28
A2	1.20	1.40	1.60
b	0.39	—	0.48
c	0.21	—	0.26
D	9.70	9.90	10.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27 (BSC)		
L	0.50	0.65	0.80
θ	0°	—	8°

9. 2 SOP14 Package Drawing



Symbol	（mm）		
	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.075	0.175	0.275
A2	1.18	1.38	1.58
b	0.406	—	0.496
c	0.178	—	0.278
D	8.45	8.65	8.85
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	—	1.27	—
L	0.55	0.65	0.75
θ	0°	—	7°

9. 3 MSOP10 Package Drawing



Symbol	（mm）		
	MIN	NOM	MAX
A	—	—	1.10
A1	0.05	—	0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.19	—	0.28
c	0.15	—	0.20
D	2.90	3.00	3.10
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
e	0.50 (BSC)		
L	0.40	—	0.70
θ	0°	—	8°

Appendix1 Instruction Set

Appendix1. 1Overview

The device provides 79 RISC instructions.

Most of the assembly instruction names are in abbreviations of English words to make programming easier. After being complied and linked by the compiler, the program consisting of these instructions will be converted to corresponding instruction codes, which include OP codes and operands. The OP codes will be mapped to the instructions.

When the chip operates with the 4MHz system clock, one machine cycle is 500ns.

Based on the machine cycles required for individual instruction operations, there are two-cycle instructions and single-cycle instructions. JUMP, GOTO, CALL, LCALL, RCALL, RET, RETIA and RETIE are two-cycle instructions; JBC, JBS, JDEC and JINC are two-cycle instructions only when the jump conditions are true, otherwise they are single-cycle instructions. All other instructions are single-cycle instructions.

Appendix1. 2Register Instructions

No.	Instructions		Affected status bits	Machine cycle	Operations
1	SECTION	I<7:0>	-	1	Not supported
2	PAGE	I<8:0>	-	1	Not supported
3	ISTEP	I<7:0>	-	1	IAA+i->IAA(-128≤i≤127)
4	MOVI	I<7:0>	-	1	I<7:0>->(A)
5	MOV	R<7:0>,F	Z,N	1	(R)->(Dest.)
6	MOVA	R<7:0>	-	1	(A)->(R)
7	MOVAR	R<10:0>	-	1	(A)->(R)
8	MOVRA	R<10:0>	-	1	(R)->(A)

Appendix1. 3Program Instructions

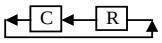
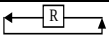
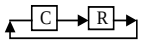
No.	Instructions		Affected status bits	Machine cycle	Operations
9	JUMP	I<7:0>	-	2	PC+1+i<7:0>->PC (-128≤i≤127)
10	AJMP	I<19:0>	-	2	I<9:0>->PC<9:0> I<9:8>->PCRH<1:0>
11	GOTO	I<10:0>	-	2	I<9:0>->PC<9:0>,

No.	Instructions		Affected status bits	Machine cycle	Operations
12	CALL	I<10:0>	-	2	PC+1->TOS,I<9:0>->PC<9:0>
13	LCALL	I<19:0>	-	2	PC+1->TOS,I<9:0>->PC<9:0> I<9:8>->PCRH<1:0>
14	RCALL	R<7:0>	-	2	PC+1→TOS, (R)→PC<7:0>, PCRH<1:0>→PC<9:8>,
15	JBC	R<7:0>, B<2:0>	-	2 or 1	If R<B> = 0, skip the next instruction
16	JBS	R<7:0>, B<2:0>	-	2 or 1	If R<B> = 1, skip the next instruction
17	JCAIE	I<7:0>	-	2 or 1	If (A) = I, skip the next instruction
18	JCAIG	I<7:0>	-	2 or 1	If (A) > I, skip the next instruction
19	JCAIL	I<7:0>	-	2 or 1	If (A) < I, skip the next instruction
20	JCRAE	R<7:0>	-	2 or 1	If (R) = (A) , skip the next instruction
21	JCRAG	R<7:0>	-	2 or 1	If (R) > (A) , skip the next instruction
22	JCRAL	R<7:0>	-	2 or 1	If (R) < (A) , skip the next instruction
23	JCCRE	R<7:0>, B<2:0>	-	2 or 1	If C = R(B) , skip the next instruction
24	JCCRG	R<7:0>, B<2:0>	-	2 or 1	If C > R(B) , skip the next instruction
25	JCCRL	R<7:0>, B<2:0>	-	2 or 1	If C < R(B) , skip the next instruction
26	JDEC	R<7:0>, F	-	2 or 1	(R-1)-> (Dest.), skip the next instruction when the value in dest. register is 0
27	JINC	R<7:0>, F	-	2 or 1	(R+1)-> (Dest.), skip the next instruction when the value in dest. register is 0
28	NOP	-	-	1	No operation
29	POP	-	-	1	AS->A, PSWS->PSW, PCRHS->PCRH
30	PUSH	-	-	1	A->AS, PSW->PSWS, PCRH->PCRHS
31	RET	-	-	2	TOS->PC

No.	Instructions		Affected status bits	Machine cycle	Operations
32	RETIA	I<7:0>	-	2	I->(A),TOS->PC
33	RETIE	-	-	2	TOS->PC,1->GIE
34	RST	-	All status bits are affected.	1	Software reset instruction
35	CWDT	-	N_TO, N_PD	1	00_H->WDT, 0->WDT Prescaler, 1-> N_TO, 1-> N_PD
36	IDLE	-	N_TO, N_PD	1	00_H->WDT, 0->WDT Prescaler, 1-> N_TO, 0-> N_PD

Appendix1. 4Arithmetic/Logical Operation Instructions

No.	Instructions		Affected status bits	Machine cycle	Operations
37	ADD	R<7:0>,F	C, DC, Z,OV,N	1	(R)+(A)->(Dest.)
38	ADDC	R<7:0>,F	C, DC, Z,OV,N	1	(R)+(A)+C->(Dest.)
39	ADDCI	I<7:0>	C, DC, Z,OV,N	1	I+(A)+C->(A)
40	ADDI	I<7:0>	C, DC, Z,OV,N	1	I+(A)->(A)
41	AND	R<7:0>,F	Z,N	1	(A).AND.(R)->(Dest.)
42	ANDI	I<7:0>	Z,N	1	I.AND.(A)->(A)
43	BCC	R<7:0>,B<2:0>	-	1	0->R<B>
44	BSS	R<7:0>,B<2:0>	-	1	1->R<B>
45	BTT	R<7:0>,B<2:0>	-	1	(~R<B>)->R<B>
46	CLR	R<7:0>	Z	1	(R)=0
47	SETR	R<7:0>	-	1	FF_H->(R)
48	NEG	R<7:0>	C, DC, Z,OV,N	1	~(R)+1-> (R)
49	COM	R<7:0>,F	Z,N	1	(~R)->(Dest.)
50	DAR	R<7:0>,F	C	1	Decimalize (R) -> (Dest.)
51	DAA	-	C	1	Decimalize (A) ->(A)
52	DEC	R<7:0>,F	C, DC, Z,OV,N	1	(R-1)->(Dest.)

No.	Instructions		Affected status bits	Machine cycle	Operations
53	INC	R<7:0>,F	C, DC, Z,OV,N	1	(R+1)->(Dest.)
54	IOR	R<7:0>,F	Z,N	1	(A).OR.(R)->(Dest.)
55	IORI	I<7:0>	Z,N	1	I.OR.(A)->(A)
56	RLB	R<7:0>,F,B<2:0>	C,Z,N	1	 C<< R<7:0>
57	RLBNC	R<7:0>,F,B<2:0>	Z,N	1	 R<7> << R<7:0>
58	RRB	R<7:0>,F,B<2:0>	C,Z,N	1	 C>> R<7:0>
59	RRBNC	R<7:0>,F,B<2:0>	Z,N	1	 R<7:0> >> R<0>
60	SUB	R<7:0>,F	C, DC, Z,OV,N	1	(R)-(A)->(Dest.)
61	SUBC	R<7:0>,F	C,DC, Z,OV,N	1	(R)-(A)- (~C)->(Dest.)
62	SUBCI	I<7:0>	C,DC, Z,OV,N	1	I-(A)- (~C)->(A)
63	SUBI	I<7:0>	C,DC, Z,OV,N	1	I-(A)->(A)
64	SSUB	R<7:0>,F	C,DC, Z,OV,N	1	(A)-(R)->(Dest.)
65	SSUBC	R<7:0>,F	C,DC, Z,OV,N	1	(A)-(R)- (~C)->(Dest.)
66	SSUBCI	I<7:0>	C,DC, Z,OV,N	1	(A)-I- (~C)->(A)
67	SSUBI	I<7:0>	C,DC, Z,OV,N	1	(A)-I->(A)
68	SWAP	R<7:0>,F	-	1	R<3:0>->(Dest.)<7:4>, R<7:4>->(Dest.)<3:0>
69	TBR	-	-	2	Pmem(FRA)->ROMD
70	TBR#1	-	-	2	Pmem(FRA)-> ROMD, FRA+1->FRA
71	TBR_1	-	-	2	Pmem(FRA)-> ROMD, FRA-1->FRA
72	TBR1#	-	-	2	FRA+1->FRA, Pmem(FRA)-> ROMD
73	TBW	-	-	2	Not supported
74	TBW#1	-	-	2	Not supported
75	TBW_1	-	-	2	Not supported

No.	Instructions		Affected status bits	Machine cycle	Operations
76	TBW1#	-	-	2	Not supported
77	XOR	R<7:0>, F	Z,N	1	(A).XOR.(R)->(Dest.)
78	XORI	I<7:0>	Z,N	1	I.XOR.(A)->(A)

Instruction Set Notes

1. i－Immediate value, F－Flag bit,　A－Register A, R－Register R, B－the Bth bit in Register R
2. C－carry/ borrow, DC－half carry/half borrow, Z－Zero flag, OV－Overflow flag, N－Negative flag
3. TOS－Top of Stack
4. If F = 0, the destination register is Register A; if F = 1, the destination register is Register R.
5. Another NOP instruction in the 79 RISC is not described in the above table.
6. For this chip, the length of PC is 11 bits and there is no PCRU register present.

Appendix2 Summary of Special Function Registers

Address	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	POR value
$FF80_H$	IAD	IAD<7:0>								0000 0000
$FF81_H$	IAAL	IAA<7:0>								0000 0000
$FF82_H$	IAAH	IAA<15:8>								0000 0000
$FF83_H$	—	—								—
$FF84_H$	PSW	—	UF	OF	N	OV	Z	DC	C	x00x xxxx
$FF85_H$	AREG	AREG<7:0>								xxxx xxxx
$FF86_H$	IAPC	IAPEN	—	—	—	—	—	IAPGO	—	0000 0000
$FF87_H$	FRAL	FRA<7:0>								xxxx xxxx
$FF88_H$	FRAH	FRA<15:8>								xxxx xxxx
$FF89_H$	ROMDL	ROMD<7:0>								xxxx xxxx
$FF8A_H$	ROMDH	ROMD<15:8>								xxxx xxxx
$FF8B_H$	PCRL	PCR<7:0>								0000 0000
$FF8C_H$	PCRH	—	—	—	—	—	PCR<10:8>			0000 0000
$FF8D_H$	-	—								—
$FF8E_H$	PA	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	xxxx xxxx
$FF8F_H$	PAT	PAT7	PAT6	PAT5	PAT4	PAT3	PAT2	PAT1	PAT0	1111 1111
$FF90_H$	PB	—	—	PB5	PB4	PB3	PB2	PB1	PB0	00xx xxxx
$FF91_H$	PBT	—	—	PBT5	PBT4	PBT3	PBT2	PBT1	PBT0	0011 1111
$FF92_H$	—	—								—
$FF93_H$	—	—								—
$FF94_H$	N_PAD	N_PAD7	N_PAD6	N_PAD5	N_PAD4	—	N_PAD2	N_PAD1	N_PAD0	1111 1111
$FF95_H$	N_PBD	—	—	PLCS	N_PBD4	N_PBD3	N_PBD2	N_PBD1	N_PBD0	0011 1111
$FF96_H$	N_PAU	N_PAU7	N_PAU6	N_PAU5	N_PAU4	N_PAU3	N_PAU2	N_PAU1	N_PAU0	1111 0111
$FF97_H$	N_PBU	—	—	N_PBU5	N_PBU4	N_PBU3	N_PBU2	N_PBU1	N_PBU0	0011 1111

Address	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	POR value
$FF98_H$	—	—								—
$FF99_H$	—	—								—
$FF9A_H$	—	—								—
$FF9B_H$	PINTS	PINT3S<1:0>		PINT2S<1:0>		PINT1S<1:0>		PINT0S<1:0>		0000 0000
$FF9C_H$	ANS	PWM20NS	PWM10NS	ANPA7	ANPB1	ANPB0	ANPA2	ANPA1	ANPA0	0000 0000
$FF9D_H$	INTF0	T8P2PIF	T8P1PIF	ADIF	LVDIF	—	T8P2TIF	T8P1TIF	KIF	0000 0000
$FF9E_H$	INTE0	T8P2PIE	T8P1PIE	ADIE	LVDIE	—	T8P2TIE	T8P1TIE	KIE	0000 0000
$FF9F_H$	INTC0	KMSK7	KMSK6	KMSK5	KMSK4	KMSK3	KMSK2	KMSK1	KMSK0	0000 0000
$FFA0_H$	INTG	GIE	—	—	—	—	—	SOFTIF	—	0000 0000
$FFA1_H$	LVDC	LVDLS	—	—	LVDEN	—	—	LVDV<1:0>		0001 0000
$FFA2_H$	INTF1	—	—	—	—	PIF3	PIF2	PIF1	PIF0	0000 0000
$FFA3_H$	INTE1	—	—	—	—	PIE3	PIE2	PIE1	PIE0	0000 0000
$FFA4_H$	INTC1	—	—	—	—	PEG3	PEG2	PEG1	PEG0	0000 0000
$FFA5_H$	OSCCAL	OSCCAL<7:0>								1010 1001
$FFA6_H$	WDTCAL	WDTCAL<7:0>								1000 0100
$FFA7_H$	PWRC	LPM	VRST<1:0>		N_RSTI	N_TO	N_PD	N_POR	N_BOR	0101 110x
$FFA8_H$	OSCC	CLKSS	FOSCS<2:0>			—	WDTOSCF	HSOSCF	LPOSCF	0110 010x
$FFA9_H$	WKDC	WKDC <7:0>								1111 1111
$FFAA_H$	OSCP	OSCP<7:0>								1111 1111
$FFAB_H$	WDTC	WDTCKS	—	—	WDTPRE	WDTPRS<3:0>				0001 0111
$FFAC_H$	PWEN	—	SW_WDT	SW_HS	SW_LP	—	—	RCEN	—	0100 0011
$FFAD_H$	—	—								—
$FFAE_H$	—	—								—
$FFAF_H$	—	—								—
$FFB0_H$	WDTP	WDTP<7:0>								1111 1111
$FFB1_H$	—	—								—

Address	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	POR value
$FFB2_H$	T8P1	T8P1<7:0>								0000 0000
$FFB3_H$	T8P1C	T8P1M	T8P1POS<3:0>				T8P1E	T8P1PRS<1:0>		0000 0000
$FFB4_H$	T8P1P	T8P1P<7:0>								1111 1111
$FFB5_H$	T8P1R	T8P1R<7:0>								0000 0000
$FFB6_H$	T8P1PMC	—	—	—	—	—	—	T8P1RS	T8P1PMS	0000 0000
$FFB7_H$	T8P1OC	T8P1TRN	T8P1REX	T8P1RE<1:0>		T8P1NEN<1:0>		T8P1PEN<1:0>		0000 0000
$FFB8_H$	T8P2	T8P2<7:0>								0000 0000
$FFB9_H$	T8P2C	T8P2M	T8P2POS<3:0>				T8P2E	T8P2PRS<1:0>		0000 0000
$FFBA_H$	T8P2P	T8P2PL<7:0>								1111 1111
$FFBB_H$	T8P2R	T8P2RL<7:0>								0000 0000
$FFBC_H$	T8P2PMC	—	—	—	—	—	—	T8P2RS	T8P2PMS	0000 0000
$FFBD_H$	T8P2OC	T8P2TRN	T8P2REX	T8P2RE<1:0>		T8P2NEN<1:0>		T8P2PEN<1:0>		0000 0000
$FFBE_H$	T8P1PDT	T8P1PDT<7:0>								0000 0000
$FFBF_H$	T8P2PDT	T8P2PDT<7:0>								0000 0000
$FFC0_H$	T8P1PEX	—	—	—	—	T8P1POSEX<3:0>				0000 0000
$FFC1_H$	T8P2PEX	—	—	—	—	T8P2POSEX<3:0>				0000 0000
$FFC2_H$	—	—								—
$FFC3_H$	—	—								—
$FFC4_H$	—	—								—
$FFC5_H$	—	—								—
$FFC6_H$	ADCCL	ADVREFS<2:0>			ADCHS<2:0>			ADTRG	ADEN	0000 0000
$FFC7_H$	ADCCH	ADFM	ADCS<2:0>			ADST<3:0>				0000 1000
$FFC8_H$	ADCRL	ADCRL<7:0>								xxxx xxxx
$FFC9_H$	ADCRH	ADCRH<7:0>								xxxx xxxx
$FFCA_H$	ADCTR	—	TRIGS	TRIGPEG	TRIGEN	—	—	—	AD2VCALS	0000 0000
$FFCB_H$	—	—								—

Address	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	POR value
$FFCC_H$	—	—								—
$FFCD_H$	—	—								—
$FFCE_H$	—	—								—
$FFCF_H$	CALPROT	—	—	—	—	—	—	—	CALPROT0	0000 0001
$FFD0_H$ ~$FFFF_H$	—	—								—

Appendix3 Electrical Characteristics

Appendix3. 1Parameter Characteristics

◆ Maximum Absolute Ratings

Parameter	Symbol	Condition	Range	Unit
Power supply	VDD	-	-0.3 ~ 7.5	V
Input voltage	V_{IN}	-	-0.3 ~ VDD + 0.3	V
Output voltage	V_{OUT}	-	-0.3 ~ VDD + 0.3	V
Storage temp	T_{STG}	-	-55 ~ 125	℃
Operating temp	T_{OPR}	VDD：2.1 ~ 5.5V	-40 ~ 85	℃

◆ Power Consumption Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating condition
Power supply	VDD	2.1	-	5.5	V	F_{OSC}≤2MHz;-40℃~85℃
		3.0	-	5.5	V	F_{OSC}≤20MHz;-40℃~85℃
Static current	I_{DD}	-	200	-	μA	25℃, VDD = 5V, internal clock mode, all I/Os input low, MRSTN = 0, OSC1 = 0 and OSC2 = 0
Current in idle 0	I_{PD1}	-	2	-	μA	25℃, VDD = 5V, BOR and WDT enabled
		-	3	-	μA	25℃, VDD = 5V, BOR, WDT and LVD enabled
Current in idle 1 (high-speed clock mode)	I_{PD2}	-	400	-	μA	25℃, VDD = 5V, BOR, WDT and LVD enabled
Current in idle 1 (low-speed clock mode)	I_{PD3}	-	25	-	μA	25℃, VDD = 5V, BOR and WDT enabled
Operating current (high-speed clock mode)	I_{OP1}	-	2	-	mA	25℃, VDD = 5V, normal operating mode, internal 16MHz RC clock, fixed I/O output, no load and ADC disabled
Operating current (high-speed clock mode)	I_{OP2}	-	610	-	uA	25℃, VDD = 5V, normal operating mode, internal 2MHz RC clock (internal 16MHz RC clock divided by 8), fixed I/O output, no load and ADC disabled

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating condition
Operating current (low-speed clock mode)	I_{OP3}	-	20	-	uA	25℃, VDD = 5V, normal operating mode, internal 32KHz RC clock, BOR and LVD enabled, fixed I/O output, no load and ADC disabled
Max. input current on VDD pin	I_{MAXVDD}	-	-	55	mA	25℃, VDD = 5V
Max. output current on VSS pin	I_{MAXVSS}	-	-	120	mA	25℃, VDD = 5V
Sink current on normal drive I/O port	I_{OL2}	-	8	-	mA	25℃,VDD = 5V V_{OL} = 0.6V
Source current on normal drive I/O port	I_{OH2}	-	8	-	mA	25℃,VDD = 5V V_{OH} = 4.4V
Sink current on high drive I/O port	I_{OL2}	-	30	-	mA	25℃,VDD = 5V V_{OL} = 0.6V
Source current on high drive I/O port	I_{OH2}	-	16	-	mA	25℃,VDD = 5V V_{OH} = 4.4V

◆ Input Port Parameters

Operating temperature range:-40℃ ~ 85℃						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Test Condition**
PA and PB input high voltage (with Schmidt input characteristics)	V_{IH}	0.8VDD	-	VDD	V	2.1V≤VDD≤5.5V
MRSTN pin input high voltage (with Schmidt input characteristics		0.8VDD	-	VDD	V	
PA and PB input low voltage	V_{IL}	VSS	-	0.18VDD	V	
MRSTN pin input low		VSS	-	0.20VDD	V	

Operating temperature range:-40℃ ~ 85℃						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Test Condition**
voltage						
PA and PB input leakage current	I_{IL}	-	-	±1	μA	2.1V≤VDD≤5.5V VSS≤Vpin≤VDD (the ports are in high-resistance state)
MRSTN pin leakage current		-	-	5	μA	VSS≤Vpin≤VDD
PA and PB input weak pull-up current	I_{WPU1}	-	50	-	μA	25℃,VDD=5.0V Vpin = VSS
PA and PB input weak pull-down current	I_{WPD1}	-	50	-	μA	25℃,VDD=5.0V Vpin = VDD
MRSTN pin input weak pull-up current	I_{WPU2}	-	50	-	μA	25℃,VDD=5.0V Vpin = VSS

◆ Output Port Characteristics

Operating temperature range:-40℃ ~ 85℃						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Test Condition**
Output high voltage	V_{OH}	VDD-0.7	-	-	V	2.1V≤VDD≤5.5V I_{OH} = 2mA
Output low voltage	V_{OL}	-	-	0.6	V	2.1V≤VDD≤5.5V I_{OL} = 3 mA

◆ System Clock Parameters

Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Test Condition**
System clock frequency	F_{OSC}	-	-	2M	Hz	2.1V≤VDD≤5.5V
		-	-	8M	Hz	2.7V≤VDD≤5.5V
		-	-	20M	Hz	3.0V≤VDD≤5.5V
System clock period	T_{OSC1}	500	-	-	ns	2.1V≤VDD≤5.5V
		125	-	-	ns	2.7V≤VDD≤5.5V
		50	-	-	ns	3.0V≤VDD≤5.5V
External clock low time and high time	T_{OSL},T_{OSH}	15	-	-	ns	-
External clock rising time and falling time	T_{OSR},T_{OSF}	-	-	15	ns	-
WDT overflow time	T_{WDT}	2.4 (9.6KHz)	8 (32KHz)	13.6 (54KHz)	ms	VDD=5V, -40℃ ~ 85℃

◆ Internal 16MHz RC Clock Calibration Parameter

Calibration Condition	Operating Condition	Min.	Typ.	Max.	Units
VDD=5V, 25℃	25℃, VDD = 5V	15.68	16	16.32	MHz
	-40℃ ~ 85℃, VDD = 2.1V ~ 5.5V	15.52	16	16.48	MHz

◆ ADC Parameters

Parameters	Symbol	Description	Min.	Typ.	Max.	Units
Resolution	RR	25℃, VDD=5V, internal reference VDD, f_{ADCCLK}=1MHz, sampling time = 8x ADCCLK	-	11	-	bit
Differential Non linearity	DNL		-	±1	-	LSB
Integral Non linearity	INL		-	±2	-	LSB
Offset voltage	Voffset	25℃, VDD=5V, f_{ADCCLK}=1MHz, sampling time = 8x ADCCLK	-	±2	-	mV
Reference voltage	Vref1	25℃, VDD=5V, external reference VREFP	2*1	-	VDD*1	V
	Vref2	25℃, VDD=5V, internal reference VDD	-	VDD*1	-	V
	Vref3	25℃,VDD=5V, internal reference 4.0V	3.92*1	4.0*1	4.08*1	V
	Vref4	25℃,VDD=5V, internal reference 3.0V	2.94*1	3.0*1	3.06*1	V
	Vref5	25℃,VDD=5V, internal reference 2.1V	2.05*1	2.1*1	2.15*1	V
Supply voltage	Vpow	internal reference VDD or external reference VREFP	2.5*1	-	-	V
		internal reference 2.1V	3*1	-	-	V
		internal reference 3.0V	3.5*1	-	-	V
		internal reference 4.0V	4.5*1	-	-	V
Analog input voltage	VIN	-	0	-	Vref1-5	V
Input capacitor	CIN	-	-	40	-	Pf
Input resistor (recommended)	RIN	-	-	10	-	KΩ

Note*1: All are theoretical values.

◆ ADC Conversion Time Parameters

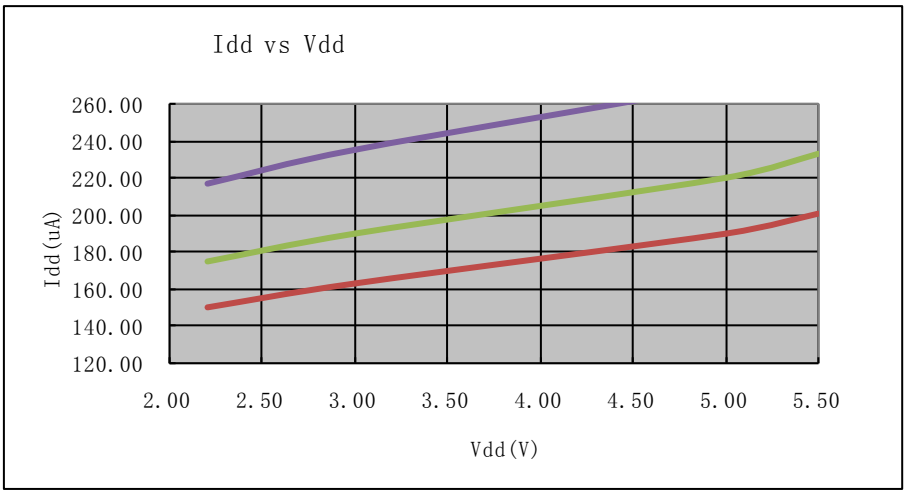
A/D Clock Source	Operating Frequency			
	16M	8M	4M	1M
Fosc	Not Recommended *2	Not Recommended *2	Not Recommended *2	T_{ADCCLK} = 1us
Fosc/2	Not Recommended *2	Not Recommended *2	T_{ADCCLK} = 0.5us	T_{ADCCLK} = 2us
Fosc/4	Not Recommended *2	T_{ADCCLK} = 0.5us	T_{ADCCLK} = 1us	T_{ADCCLK} = 4us
Fosc/8	T_{ADCCLK} = 0.5us	T_{ADCCLK} = 1us	T_{ADCCLK} = 2us	T_{ADCCLK} = 8us
Fosc/16	T_{ADCCLK} = 1us	T_{ADCCLK} = 2us	T_{ADCCLK} = 4us	T_{ADCCLK} = 16us
Fosc/32	T_{ADCCLK} = 2us	T_{ADCCLK} = 4us	T_{ADCCLK} = 8us	T_{ADCCLK} = 32us
Fosc/64	T_{ADCCLK} = 4us	T_{ADCCLK} = 8us	T_{ADCCLK} = 16us	T_{ADCCLK} = 64us

Note*2: Tad values do not meet the resolution requirement, so not recommended.

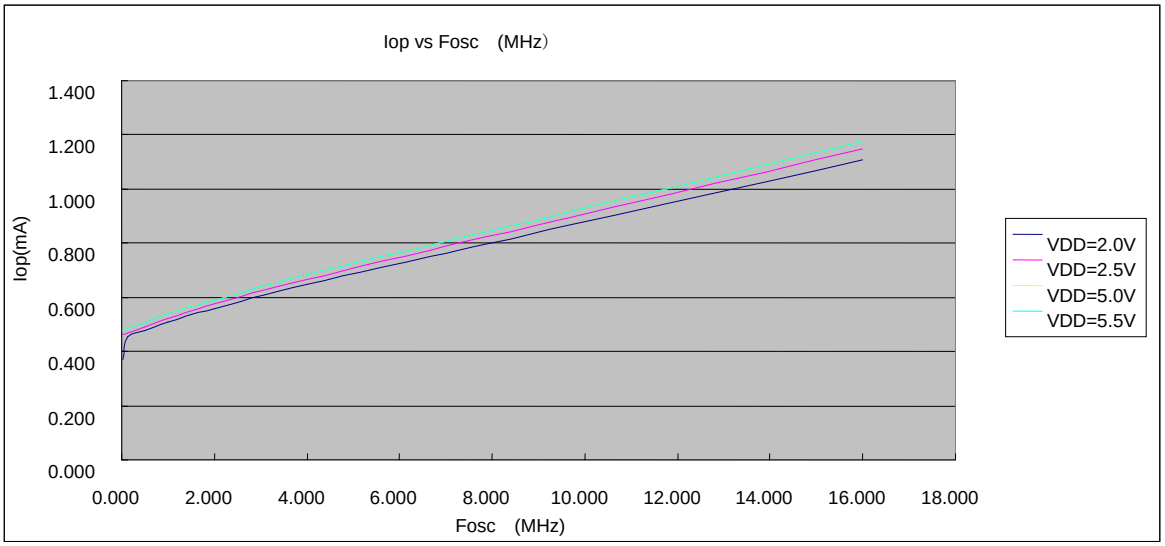
Appendix3. 2Characteristics Graphs

All the graphs provided are a statistical summary based on a limited number of samples and are provided for design reference only. Some data in part of the graphs are beyond specification and the device is guaranteed to operate normally only within the specified range.

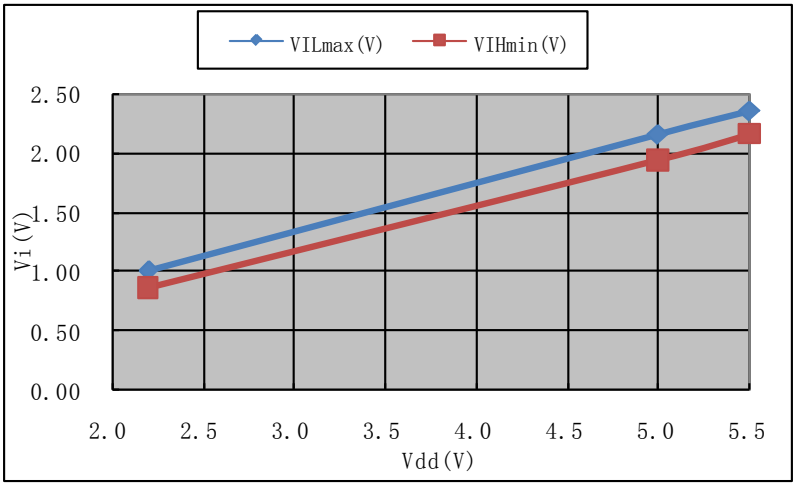
- Idd vs. VDD VDD @25℃



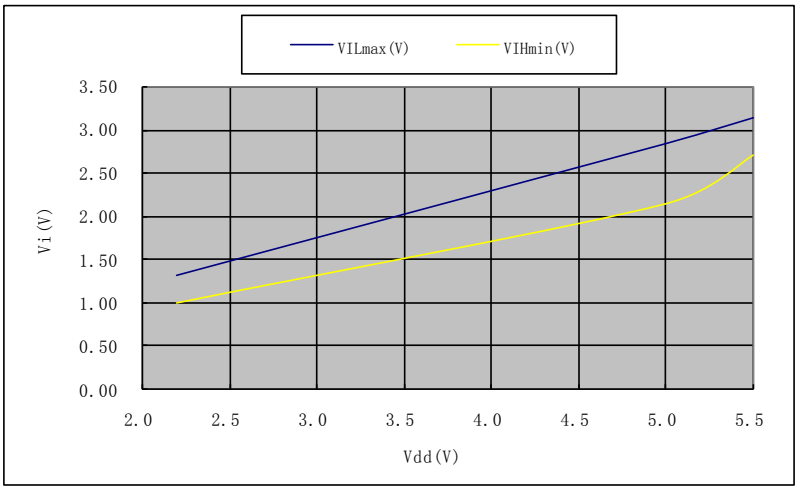
- Iop vs. Fosc (Fosc is the divided frequencies of internal 16MHz, @25℃)



◆ Vi vs. VDD on MRSTN pin @25℃

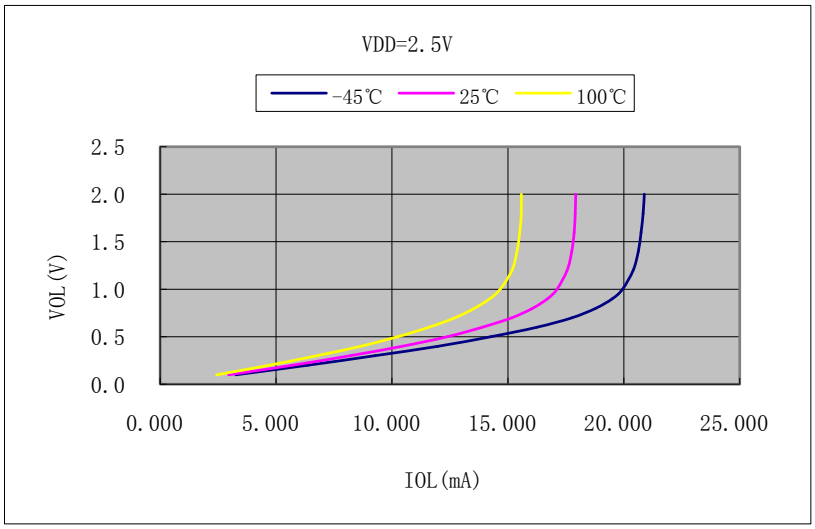


◆ Vi vs. VDD on PB0 pin

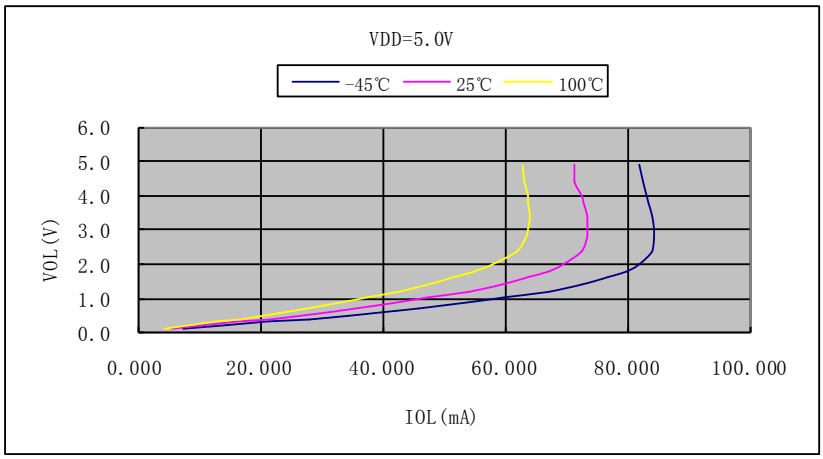


◆ I/O Ports Output Characteristics

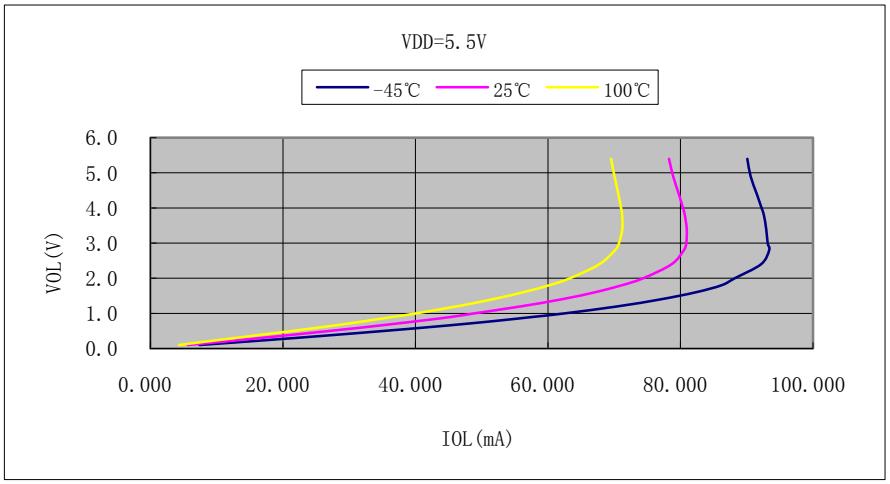
A: V_{OL} vs I_{OL}@VDD=2.5V



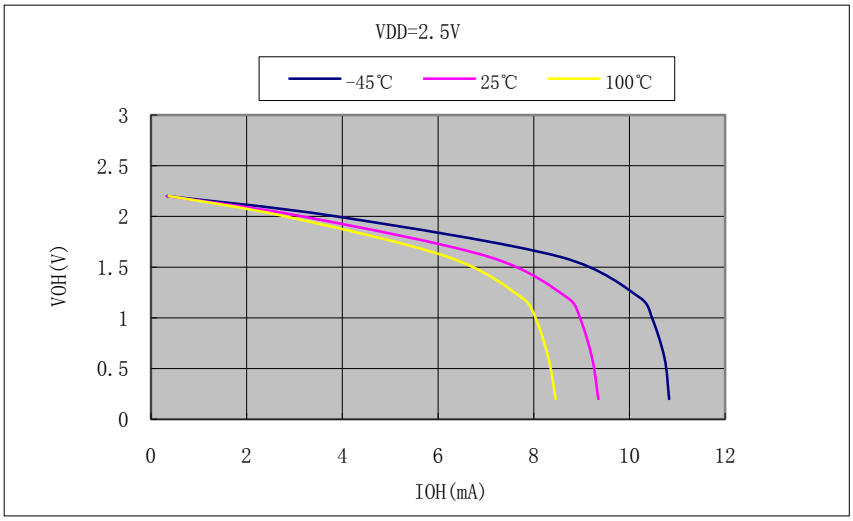
B: V_{OL} vs I_{OL}@VDD=5.0V



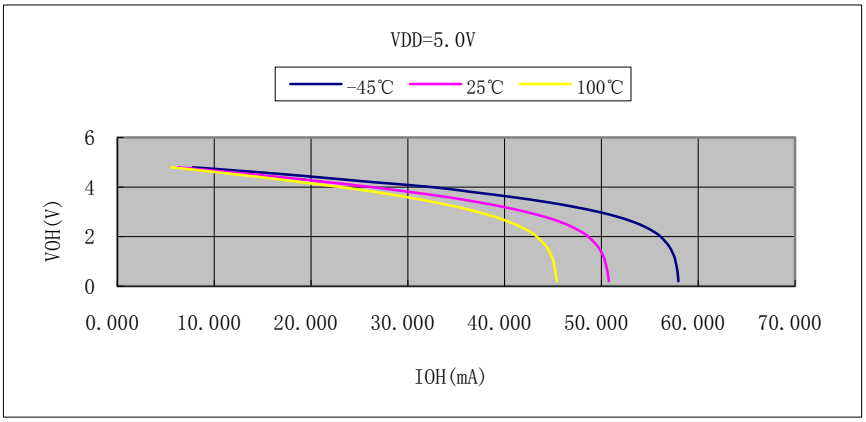
C: V_{OL} vs I_{OL}@VDD=5.5V



D: V_{OH} vs I_{OH}@VDD=2.5V



E: V_{OH} vs I_{OH}@VDD=5V



F: V_{OH} vs I_{OH}@V_{DD}=5.5V