E-102
Hardware Reference Manual

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Theory of Operation

The purpose of this document is to familiarize you with the E-102 hardware.

The E-102 features a Xilinx Zynq Z-7020 System-on-a-Chip. It is to designed to be a flexible solution in multiple applications. It can run as an embedded module with a large amount of user I/O, in a standalone application, or as a USB peripheral device.

Specifications

XC7Z020-CLG484C Programmable SoC (Engineering Silicon)

- 85K Logic Cells
- Dual core ARM Cortex-A9 MPCores up to 667 MHz (-1 speed grade)
- Commercial Temperature grade (0°C to +85°C)

DDR3 DRAM

- 512 MB total density
- 32 bit data bus
- Up to 533 MHz DDR
- 3.97 GB/s total DDR3 bandwidth

USB OTG

- Supports either host or peripheral operation through USB Micro-AB receptacle
- Access to onboard ARM processors through Zynq MIO

USB UART

- Supports UART connection through USB Micro-B receptacle
- Access to onboard ARM processors through Zynq MIO

HDMI Output

- Output up to 1080P 24-bit color video through HDMI-Micro (Type-D) receptacle

MicroSD Card

- Boot from MicroSD or MicroSDHC card through Zynq MIO
- A 4GB Class 4 MicroSD card is included

33 Zynq MIO GPIO

- Accessed through Samtec QSH-030-01-L-D-A
  - Mating Part: QTH-030-02-L-D-A
- 1.8V operation

150 Zynq SelectIO GPIO

- Accessed through Samtec QSH-090-01-L-D-A
  - Mating Part: QTH-090-02-L-D-A
- 3 separate GPIO banks with 2 separate programmable voltage rails
  - 3 pin Voltage ID programming available through hardware or from FPGA

- GPIO Voltage rails available to mating card for up to 1A current draw

DONE, INIT, and GPIO status LEDs

- See “Status LED Description” section for more details

Mechanical and Environmental

- Board Dimensions: 50mm x 80mm
- Commercial Temperature rating

System Monitoring

- Die temperature monitoring
- VCCINT and VCCAUX Voltage monitoring

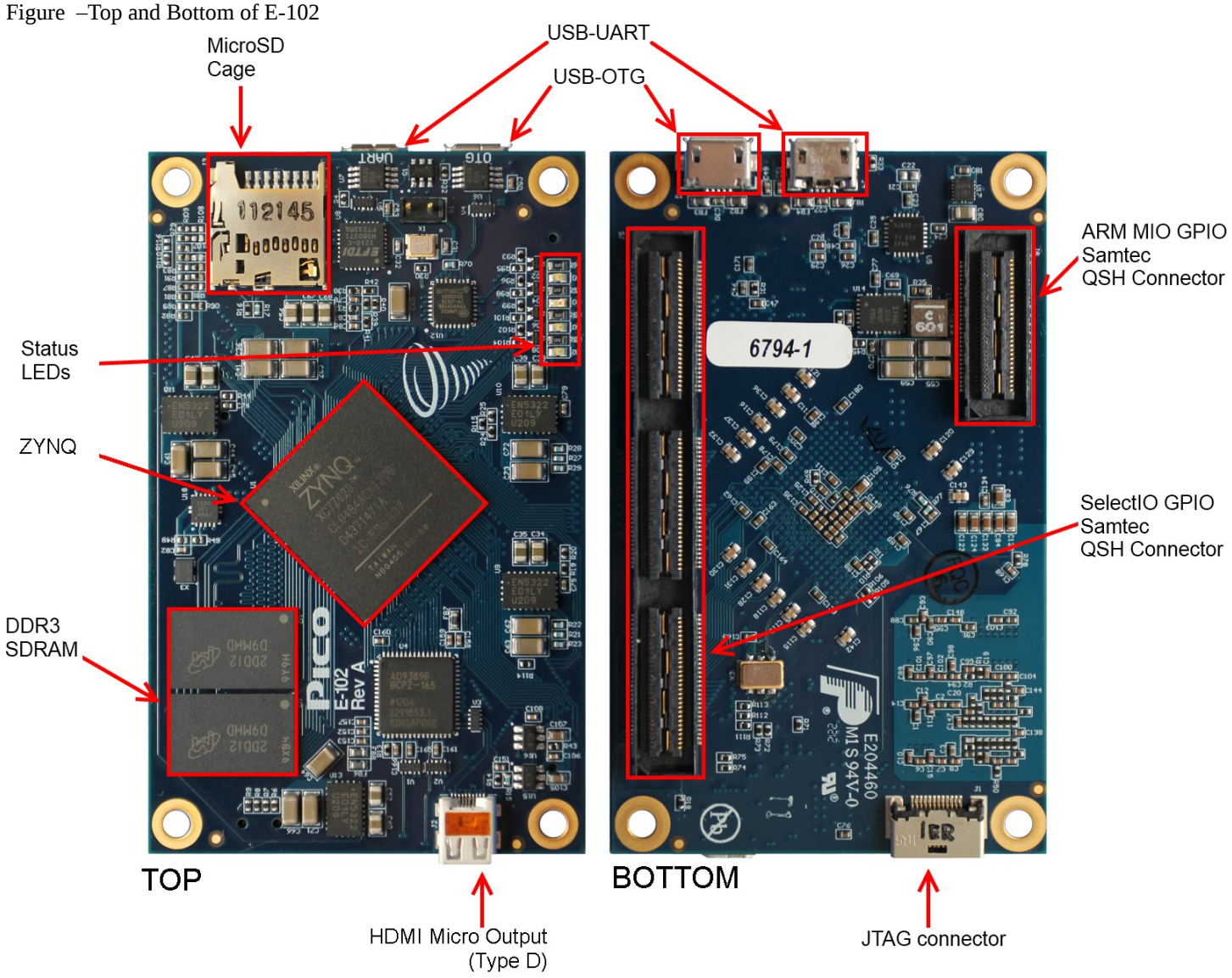
Included with E-102

- 4GB Class 4 MicroSD card
- MicroSD to full size SD adapter
- USB A Male to Micro-B Male Cable
- JTAG Cable Adapter

Please use anti-static handling precautions when handling the board.

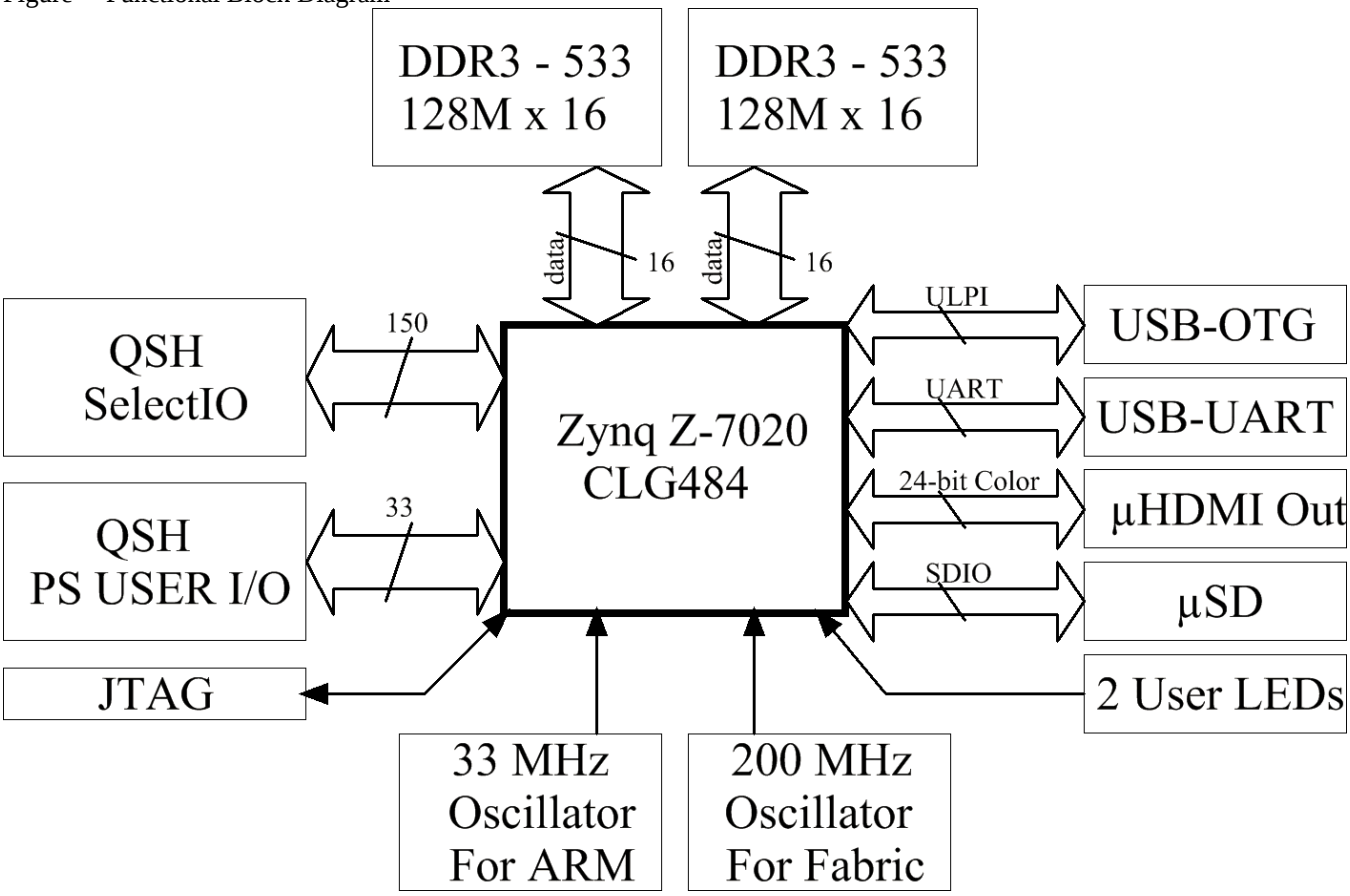
Board Overview

Figure –Top and Bottom of E-102



E-102 Block Diagram

Figure – Functional Block Diagram



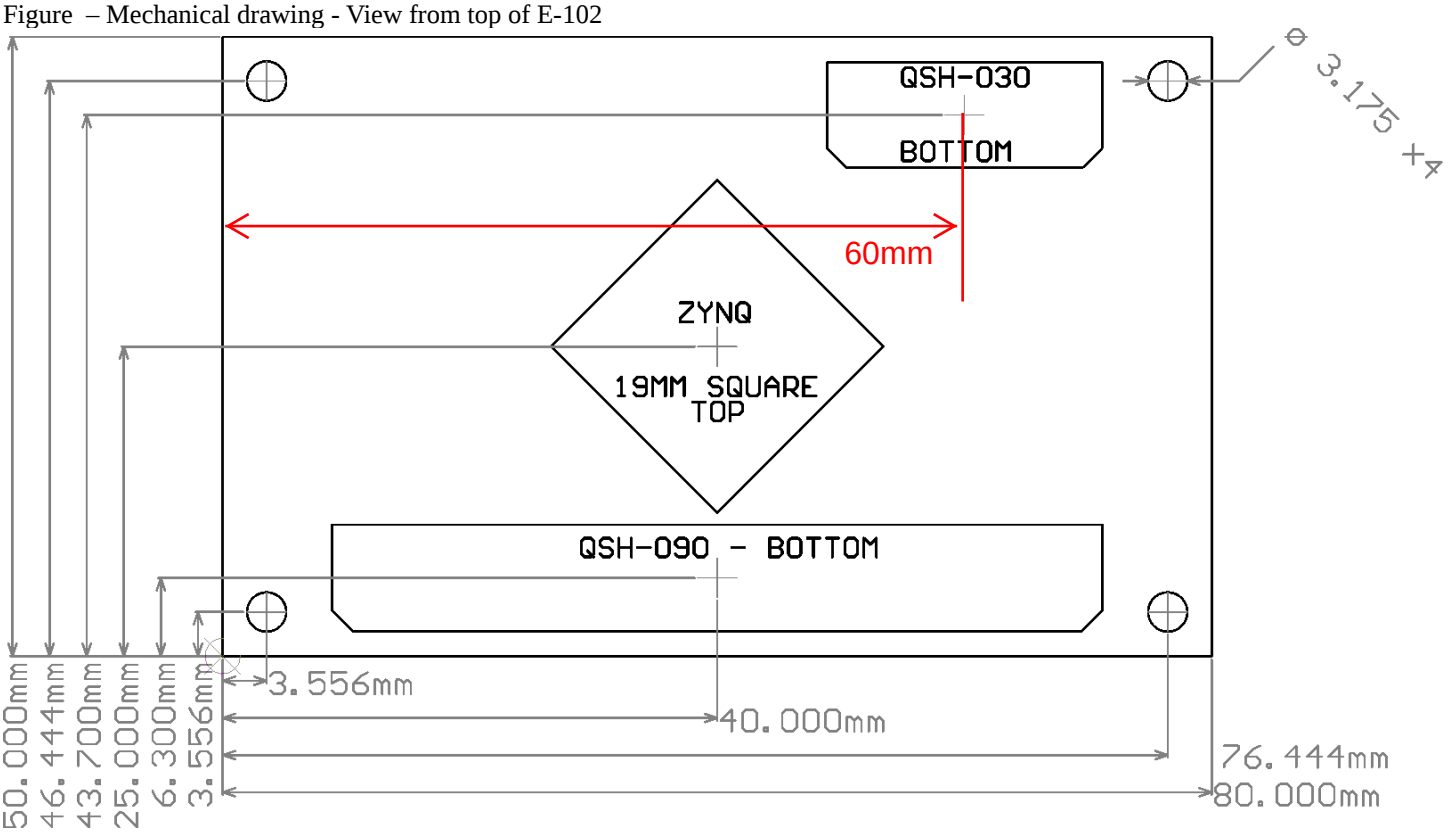
Mechanical

The E-102 is 50mm x 80mm

It has 1 mounting hole in each of the 4 corners that will fit either a standard #4 screw or a metric M3 screw.

It can mate to a carrier board using Samtec Q-Series I/O connectors (see 33 Zynq MIO GPIO and "150 Zynq SelectIO GPIO" for mating parts)

Figure – Mechanical drawing - View from top of E-102



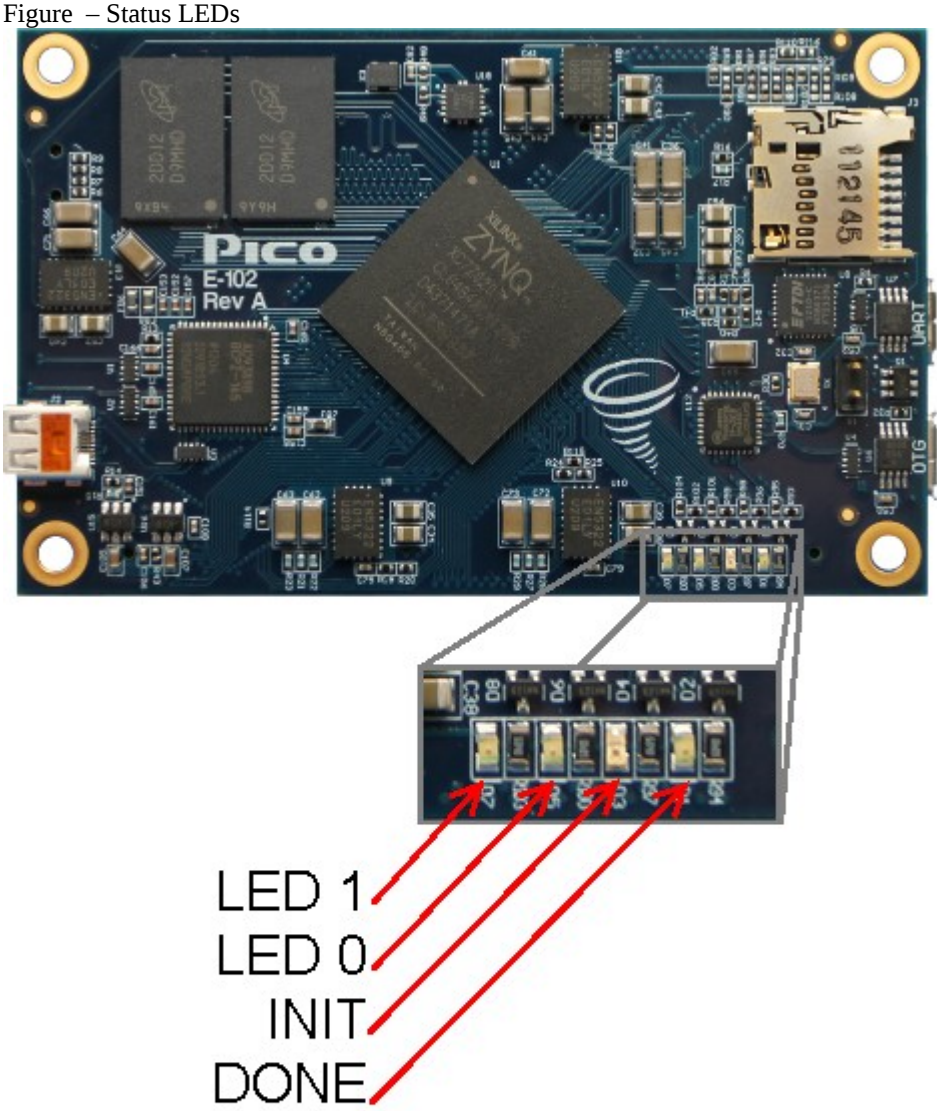
Configuration

The Zynq boots through the MicroSD slot. See Firmware and Software docs for more details.

Status LED Description

The E-102 utilizes LEDs in order to provide status feedback. The DONE and INIT pins drive the 2 right-most LEDs in the Figure below. There are also 2 LEDs that are driven by pins on the FPGA and can be used to indicate statuses chosen by the user.

Figure – Status LEDs



STATUS	COLOR
DONE	GREEN
INIT	YELLOW
LED0	GREEN
LED1	GREEN

Clock Circuitry

The Zynq on the E-102 has 2 separate clock inputs.

PS_CLK

- PS_CLK is driven by a 33.33 MHz oscillator.
- The Zynq uses this clock to generate all of the appropriate clocks for the ARM and Memory.
- This clock can also be used to generate a logic clock.

SYS_CLK

- SYS_CLK is driven by a 200 MHz low-jitter differential oscillator.
- This clock drives a Multi-Region-Clock-Capable input in the FPGA's SelectIO.
- SYS_CLK_P and SYS_CLK_N are on FPGA balls Y6 and Y5 respectively.
-

GPIO Header Pin Locations

Figure - GPIO connector, view from top, through board

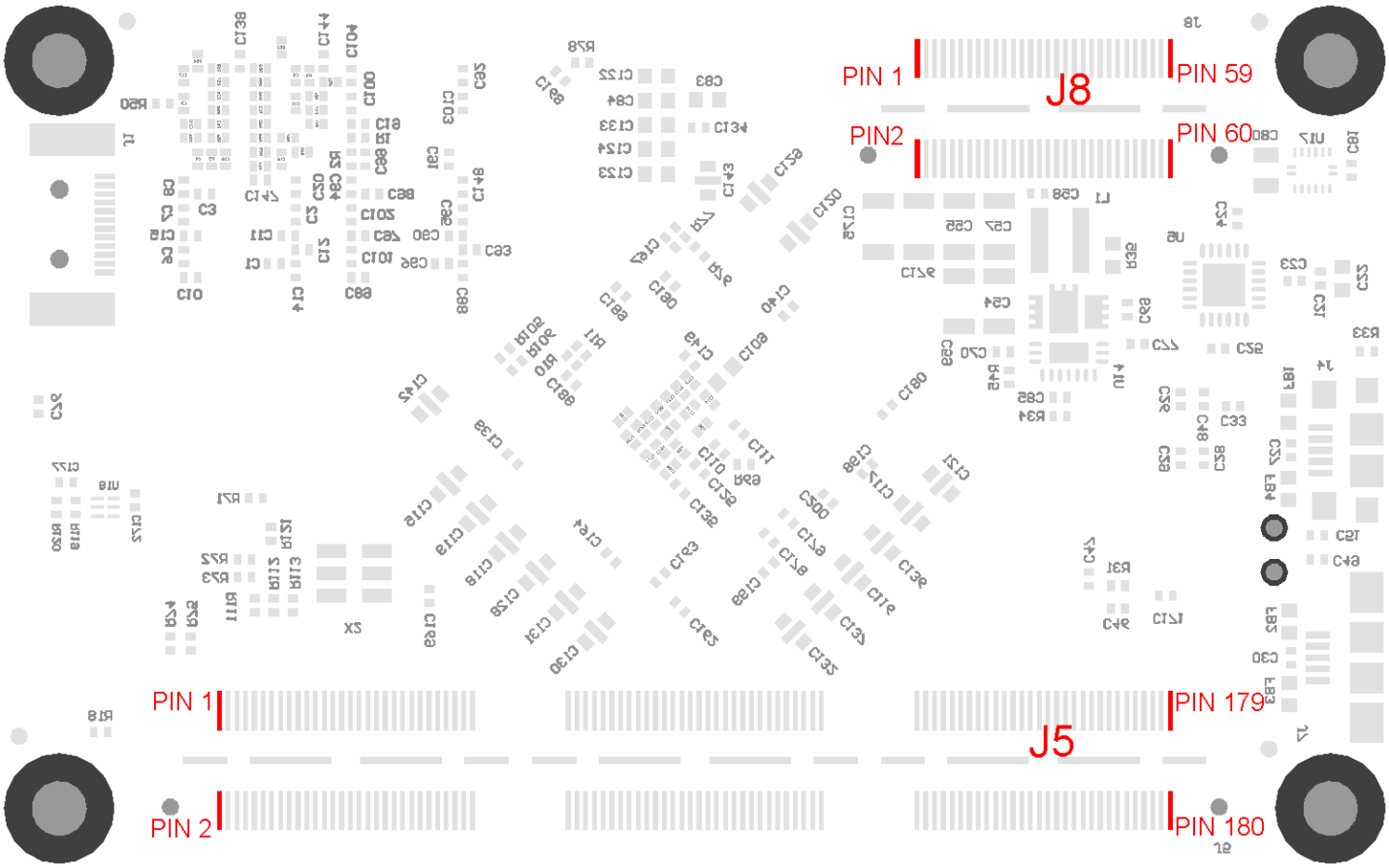


Table - J8 pinout

Net Name	FPGA Ball	J8 pin	Logic Level	Pin Type	Notes
GND	------	0	------	POWER	GND Blade on Q-Series Connector
1.8V	------	1	------	POWER	1.8V Power Output
5V	------	2	------	POWER	Main Power Input OR Output
1.8V	------	3	------	POWER	1.8V Power Output
5V	------	4	------	POWER	Main Power Input OR Output
1.8V	------	5	------	POWER	1.8V Power Output
5V	------	6	------	POWER	Main Power Input OR Output
PS_MIO9_500	C4	7	1.8V	INPUT/OUTPUT	
PS_MIO13_500	A6	8	1.8V	INPUT/OUTPUT	
PS_MIO7_500	D5	9	1.8V	INPUT/OUTPUT	Pulled high with 20K resistor on E-102. Pin is polled at powerup for Boot-up settings
PS_POR_B_500	B5	10	1.8V	INPUT	Held low until 1.5V DDR3 Rail is stable
PS_MIO16_501	D6	11	1.8V	INPUT/OUTPUT	
PS_MIO6_500	A4	12	1.8V	INPUT/OUTPUT	Pulled low with 20K resistor on E-102. Pin is polled at powerup for Boot-up settings
PS_MIO27_501	D7	13	1.8V	INPUT/OUTPUT	
PS_MIO5_500	A3	14	1.8V	INPUT/OUTPUT	Pulled high with 20K resistor on E-102. Pin is polled at powerup for Boot-up settings
PS_MIO3_500	F6	15	1.8V	INPUT/OUTPUT	Pulled low with 20K resistor on E-102. Pin is polled at powerup for Boot-up settings
PS_MIO14_500	B6	16	1.8V	INPUT/OUTPUT	
PS_MIO17_501	E9	17	1.8V	INPUT/OUTPUT	
PS_MIO24_501	B7	18	1.8V	INPUT/OUTPUT	
PS_SRST_B_501	C9	19	1.8V	INPUT	Pulled high with 10K resisitor on E-102
PS_MIO20_501	A8	20	1.8V	INPUT/OUTPUT	
PS_MIO19_501	E10	21	1.8V	INPUT/OUTPUT	
PS_MIO47_501	B10	22	1.8V	INPUT/OUTPUT	
PS_MIO11_500	B4	23	1.8V	INPUT/OUTPUT	
PS_MIO23_501	E11	24	1.8V	INPUT/OUTPUT	
PS_MIO8_500	E5	25	1.8V	INPUT/OUTPUT	Pulled high with 20K resistor on E-102. Pin is polled at powerup for Boot-up settings
PS_MIO51_501	C10	26	1.8V	INPUT/OUTPUT	

PS_MIO12_500	C5	27	1.8V	INPUT/OUTPUT	
PS_MIO18_501	A7	28	1.8V	INPUT/OUTPUT	
PS_MIO15_500	E6	29	1.8V	INPUT/OUTPUT	
PS_MIO26_501	A13	30	1.8V	INPUT/OUTPUT	
PS_MIO10_500	G7	31	1.8V	INPUT/OUTPUT	
PS_MIO22_501	A14	32	1.8V	INPUT/OUTPUT	
PS_MIO52_501	D10	33	1.8V	INPUT/OUTPUT	
PS_MIO50_501	D13	34	1.8V	INPUT/OUTPUT	
PS_MIO53_501	C12	35	1.8V	INPUT/OUTPUT	
PS_MIO46_501	D12	36	1.8V	INPUT/OUTPUT	
PS_MIO4_500	E4	37	1.8V	INPUT/OUTPUT	Pulled high with 20K resistor on E-102. Pin is polled at powerup for Boot-up settings
PS_MIO21_501	F11	38	1.8V	INPUT/OUTPUT	
PS_MIO2_500	A2	39	1.8V	INPUT/OUTPUT	Pulled low with 20K resistor on E-102. Pin is polled at powerup for Boot-up settings
PS_MIO25_501	F12	40	1.8V	INPUT/OUTPUT	
PS_MIO1_500	A1	41	1.8V	INPUT/OUTPUT	
------	------	42	------	NC	
------	------	43	------	NC	
------	------	44	------	NC	
------	------	45	------	NC	
------	------	46	------	NC	
------	------	47	------	NC	
------	------	48	------	NC	
------	------	49	------	NC	
------	------	50	------	NC	
------	------	51	------	NC	
------	------	52	------	NC	
------	------	53	------	NC	
------	------	54	------	NC	
------	------	55	------	NC	
------	------	56	------	NC	
------	------	57	------	NC	
------	------	58	------	NC	
------	------	59	------	NC	
------	------	60	------	NC	

Table - J5 pinout

Net Name	FPGA Ball	J5 pin	Logic Level	Pin Type	Notes
GND	------	0	------	POWER	GND Blade on Q-Series Connector
GPIO_001	Y16	1	VGPIO0	INPUT/OUTPUT	
GPIO_002	W21	2	VGPIO0	INPUT/OUTPUT	
GPIO_003	W17	3	VGPIO0	INPUT/OUTPUT	
GPIO_004	W22	4	VGPIO0	INPUT/OUTPUT	
GPIO_005	AA18	5	VGPIO0	INPUT/OUTPUT	
GPIO_006	AA19	6	VGPIO0	INPUT/OUTPUT	
GPIO_007	Y18	7	VGPIO0	INPUT/OUTPUT	
GPIO_008	AB17	8	VGPIO0	INPUT/OUTPUT	
GPIO_009	Y19	9	VGPIO0	INPUT/OUTPUT	
GPIO_010	AB14	10	VGPIO0	INPUT/OUTPUT	
GPIO_011	Y20	11	VGPIO0	INPUT/OUTPUT	
GPIO_012	AB15	12	VGPIO0	INPUT/OUTPUT	
GPIO_013	Y21	13	VGPIO0	INPUT/OUTPUT	
GPIO_014	AA14	14	VGPIO0	INPUT/OUTPUT	
GPIO_015	AA21	15	VGPIO0	INPUT/OUTPUT	
GPIO_016	AA17	16	VGPIO0	INPUT/OUTPUT	
GPIO_017	AA16	17	VGPIO0	INPUT/OUTPUT	
GPIO_018	AA13	18	VGPIO0	INPUT/OUTPUT	
GPIO_019	V15	19	VGPIO0	INPUT/OUTPUT	
GPIO_020	AB16	20	VGPIO0	INPUT/OUTPUT	
GPIO_021	W15	21	VGPIO0	INPUT/OUTPUT	
GPIO_022	V13	22	VGPIO0	INPUT/OUTPUT	
GPIO_023	Y14	23	VGPIO0	INPUT/OUTPUT	
GPIO_024	U17	24	VGPIO0	INPUT/OUTPUT	
GPIO_025	V14	25	VGPIO0	INPUT/OUTPUT	
GPIO_026	U14	26	VGPIO0	INPUT/OUTPUT	
GPIO_027	Y13	27	VGPIO0	INPUT/OUTPUT	

GPIO_028	U15	28	VGPIO0	INPUT/OUTPUT	
GPIO_029	W13	29	VGPIO0	INPUT/OUTPUT	
GPIO_030	U16	30	VGPIO0	INPUT/OUTPUT	
GPIO_031	Y15	31	VGPIO0	INPUT/OUTPUT	
GPIO_032	W16	32	VGPIO0	INPUT/OUTPUT	
GPIO_033	U20	33	VGPIO0	INPUT/OUTPUT	
GPIO_034	V17	34	VGPIO0	INPUT/OUTPUT	
GPIO_035	U19	35	VGPIO0	INPUT/OUTPUT	
GPIO_036	T22	36	VGPIO0	INPUT/OUTPUT	
GPIO_037	V18	37	VGPIO0	INPUT/OUTPUT	
GPIO_038	U22	38	VGPIO0	INPUT/OUTPUT	
GPIO_039	V19	39	VGPIO0	INPUT/OUTPUT	
GPIO_040	V22	40	VGPIO0	INPUT/OUTPUT	
GPIO_041	W18	41	VGPIO0	INPUT/OUTPUT	
GPIO_042	AB22	42	VGPIO0	INPUT/OUTPUT	
GPIO_043	V20	43	VGPIO0	INPUT/OUTPUT	
GPIO_044	AB21	44	VGPIO0	INPUT/OUTPUT	
GPIO_045	W20	45	VGPIO0	INPUT/OUTPUT	
GPIO_046	AB20	46	VGPIO0	INPUT/OUTPUT	
GPIO_047	U21	47	VGPIO0	INPUT/OUTPUT	
GPIO_048	AB19	48	VGPIO0	INPUT/OUTPUT	
GPIO_049	T21	49	VGPIO0	INPUT/OUTPUT	
GPIO_050	AA22	50	VGPIO0	INPUT/OUTPUT	
------	------	51	------	NC	
------	------	52	------	NC	
------	------	53	------	NC	
USER_VGPIO_EN	Y11	54	1.8V	INPUT	Enable for VGPIO0 and VGPIO1. Pulled low WITH 1.62K resistor on E-102 to diable these regulators by default. Can be controlled in hardware from carrier board or in firmware from FPGA
VGPIO0	------	55	------	POWER	Voltage ouput for VGPIO0 - Disabled by default
VGPIO0_VS2	V8	56	1.8V	INPUT	Voltage Selection for VGPIO0. Pulled low WITH 1K resistor on E-102 for default 3.3V operation. Can be controlled in hardware from carrier board or in firmware from FPGA

VGPIO0	------	57	------	POWER	Voltage ouput for VGPIO0 - Disabled by default
VGPIO0_VS1	V7	58	1.8V	INPUT	Voltage Selection for VGPIO0. Pulled low WITH 1K resistor on E-102 for default 3.3V operation. Can be controlled in hardware from carrier board or in firmware from FPGA
VGPIO0	------	59	------	POWER	Voltage ouput for VGPIO0 - Disabled by default
VGPIO0_VS0	U6	60	1.8V	INPUT	Voltage Selection for VGPIO0. Pulled low WITH 1K resistor on E-102 for default 3.3V operation. Can be controlled in hardware from carrier board or in firmware from FPGA
------	------	61	------	NC	
5V	------	62	------	POWER	Main Power Input OR Output
------	------	63	------	NC	
5V	------	64	------	POWER	Main Power Input OR Output
GPIO_051	R16	65	VGPIO1	INPUT/OUTPUT	
GPIO_052	P15	66	VGPIO1	INPUT/OUTPUT	
GPIO_053	P16	67	VGPIO1	INPUT/OUTPUT	
GPIO_054	E19	68	VGPIO1	INPUT/OUTPUT	
GPIO_055	T16	69	VGPIO1	INPUT/OUTPUT	
GPIO_056	F19	70	VGPIO1	INPUT/OUTPUT	
GPIO_057	P17	71	VGPIO1	INPUT/OUTPUT	
GPIO_058	G20	72	VGPIO1	INPUT/OUTPUT	
GPIO_059	R18	73	VGPIO1	INPUT/OUTPUT	
GPIO_060	T19	74	VGPIO1	INPUT/OUTPUT	
GPIO_061	T17	75	VGPIO1	INPUT/OUTPUT	
GPIO_062	H19	76	VGPIO1	INPUT/OUTPUT	
GPIO_063	P20	77	VGPIO1	INPUT/OUTPUT	
GPIO_064	R20	78	VGPIO1	INPUT/OUTPUT	
GPIO_065	T18	79	VGPIO1	INPUT/OUTPUT	
GPIO_066	R21	80	VGPIO1	INPUT/OUTPUT	
GPIO_067	P18	81	VGPIO1	INPUT/OUTPUT	
GPIO_068	P22	82	VGPIO1	INPUT/OUTPUT	
GPIO_069	R19	83	VGPIO1	INPUT/OUTPUT	
GPIO_070	P21	84	VGPIO1	INPUT/OUTPUT	
GPIO_071	N17	85	VGPIO1	INPUT/OUTPUT	
GPIO_072	N22	86	VGPIO1	INPUT/OUTPUT	

GPIO_073	M17	87	VGPIO1	INPUT/OUTPUT	
GPIO_074	N20	88	VGPIO1	INPUT/OUTPUT	
GPIO_075	R15	89	VGPIO1	INPUT/OUTPUT	
GPIO_076	M22	90	VGPIO1	INPUT/OUTPUT	
GPIO_077	N19	91	VGPIO1	INPUT/OUTPUT	
GPIO_078	E20	92	VGPIO1	INPUT/OUTPUT	
GPIO_079	M19	93	VGPIO1	INPUT/OUTPUT	
GPIO_080	D20	94	VGPIO1	INPUT/OUTPUT	
GPIO_081	M20	95	VGPIO1	INPUT/OUTPUT	
GPIO_082	D18	96	VGPIO1	INPUT/OUTPUT	
GPIO_083	L19	97	VGPIO1	INPUT/OUTPUT	
GPIO_084	C19	98	VGPIO1	INPUT/OUTPUT	
GPIO_085	K19	99	VGPIO1	INPUT/OUTPUT	
GPIO_086	B20	100	VGPIO1	INPUT/OUTPUT	
GPIO_087	J18	101	VGPIO1	INPUT/OUTPUT	
GPIO_088	D17	102	VGPIO1	INPUT/OUTPUT	
GPIO_089	J20	103	VGPIO1	INPUT/OUTPUT	
GPIO_090	C17	104	VGPIO1	INPUT/OUTPUT	
GPIO_091	K20	105	VGPIO1	INPUT/OUTPUT	
GPIO_092	D16	106	VGPIO1	INPUT/OUTPUT	
GPIO_093	K21	107	VGPIO1	INPUT/OUTPUT	
GPIO_094	N15	108	VGPIO1	INPUT/OUTPUT	
GPIO_095	L21	109	VGPIO1	INPUT/OUTPUT	
GPIO_096	N18	110	VGPIO1	INPUT/OUTPUT	
GPIO_097	L22	111	VGPIO1	INPUT/OUTPUT	
GPIO_098	M16	112	VGPIO1	INPUT/OUTPUT	
GPIO_099	M21	113	VGPIO1	INPUT/OUTPUT	
GPIO_100	L18	114	VGPIO1	INPUT/OUTPUT	
VGPIO1	------	115	------	POWER	Voltage ouput for VGPIO1 - Disabled by default

VGPIO1_VS2	U12	116	1.8V	INPUT	Voltage Selection for VGPIO1. Pulled low WITH 1K resistor on E-102 for default 3.3V operation. Can be controlled in hardware from carrier board or in firmware from FPGA
VGPIO1	------	117	------	POWER	Voltage ouput for VGPIO1 - Disabled by default
VGPIO1_VS1	V12	118	1.8V	INPUT	Voltage Selection for VGPIO1. Pulled low WITH 1K resistor on E-102 for default 3.3V operation. Can be controlled in hardware from carrier board or in firmware from FPGA
VGPIO1	------	119	------	POWER	Voltage ouput for VGPIO1 - Disabled by default
VGPIO1_VS0	W12	120	1.8V	INPUT	Voltage Selection for VGPIO1. Pulled low WITH 1K resistor on E-102 for default 3.3V operation. Can be controlled in hardware from carrier board or in firmware from FPGA
------	------	121	------	NC	
5V	------	122	------	POWER	Main Power Input OR Output
------	------	123	------	NC	
5V	------	124	------	POWER	Main Power Input OR Output
------	------	125	------	NC	
------	------	126	------	NC	
------	------	127	------	NC	
------	------	128	------	NC	
------	------	129	------	NC	
------	------	130	------	NC	
GPIO_101	G22	131	VGPIO1	INPUT/OUTPUT	
GPIO_102	K18	132	VGPIO1	INPUT/OUTPUT	
GPIO_103	H20	133	VGPIO1	INPUT/OUTPUT	
GPIO_104	J17	134	VGPIO1	INPUT/OUTPUT	
GPIO_105	H22	135	VGPIO1	INPUT/OUTPUT	
GPIO_106	H18	136	VGPIO1	INPUT/OUTPUT	
GPIO_107	J21	137	VGPIO1	INPUT/OUTPUT	
GPIO_108	H17	138	VGPIO1	INPUT/OUTPUT	
GPIO_109	J22	139	VGPIO1	INPUT/OUTPUT	
GPIO_110	G19	140	VGPIO1	INPUT/OUTPUT	
GPIO_111	E21	141	VGPIO1	INPUT/OUTPUT	
GPIO_112	F18	142	VGPIO1	INPUT/OUTPUT	
GPIO_113	F21	143	VGPIO1	INPUT/OUTPUT	
GPIO_114	E18	144	VGPIO1	INPUT/OUTPUT	
GPIO_115	F22	145	VGPIO1	INPUT/OUTPUT	
GPIO_116	E16	146	VGPIO1	INPUT/OUTPUT	
GPIO_117	G21	147	VGPIO1	INPUT/OUTPUT	

GPIO_118	D15	148	VGPIO1	INPUT/OUTPUT	
GPIO_119	D22	149	VGPIO1	INPUT/OUTPUT	
GPIO_120	C15	150	VGPIO1	INPUT/OUTPUT	
GPIO_121	B22	151	VGPIO1	INPUT/OUTPUT	
GPIO_122	B15	152	VGPIO1	INPUT/OUTPUT	
GPIO_123	C20	153	VGPIO1	INPUT/OUTPUT	
GPIO_124	E15	154	VGPIO1	INPUT/OUTPUT	
GPIO_125	C22	155	VGPIO1	INPUT/OUTPUT	
GPIO_126	M15	156	VGPIO1	INPUT/OUTPUT	
GPIO_127	D21	157	VGPIO1	INPUT/OUTPUT	
GPIO_128	L17	158	VGPIO1	INPUT/OUTPUT	
GPIO_129	B21	159	VGPIO1	INPUT/OUTPUT	
GPIO_130	L16	160	VGPIO1	INPUT/OUTPUT	
GPIO_131	A19	161	VGPIO1	INPUT/OUTPUT	
GPIO_132	K16	162	VGPIO1	INPUT/OUTPUT	Pulled low on E-102 with 10K resistor for proper PUDC operation
GPIO_133	B19	163	VGPIO1	INPUT/OUTPUT	
GPIO_134	J16	164	VGPIO1	INPUT/OUTPUT	
GPIO_135	A21	165	VGPIO1	INPUT/OUTPUT	
GPIO_136	G17	166	VGPIO1	INPUT/OUTPUT	
GPIO_137	A22	167	VGPIO1	INPUT/OUTPUT	
GPIO_138	F17	168	VGPIO1	INPUT/OUTPUT	
GPIO_139	A18	169	VGPIO1	INPUT/OUTPUT	
GPIO_140	F16	170	VGPIO1	INPUT/OUTPUT	
GPIO_141	C18	171	VGPIO1	INPUT/OUTPUT	
GPIO_142	K15	172	VGPIO1	INPUT/OUTPUT	
GPIO_143	A17	173	VGPIO1	INPUT/OUTPUT	
GPIO_144	J15	174	VGPIO1	INPUT/OUTPUT	
GPIO_145	B17	175	VGPIO1	INPUT/OUTPUT	
GPIO_146	H15	176	VGPIO1	INPUT/OUTPUT	

GPIO_147	A16	177	VGPIO1	INPUT/OUTPUT	
GPIO_148	G15	178	VGPIO1	INPUT/OUTPUT	
GPIO_149	B16	179	VGPIO1	INPUT/OUTPUT	
GPIO_150	G16	180	VGPIO1	INPUT/OUTPUT	

Power

The E-102 can be powered AND supply power through multiple channels:

GPIO connectors (J5 & J8)

- The 5V rail connects directly to 4 pins on J5 and 3 pins on J8.
- Power can be sourced from either the E-102 OR from a carrier board using these pins.
- If power is sourced through these connectors, proper precautions (power OR-ing and current backflow protection) should be taken to ensure no damage is done to the power supply.

USB-OTG Receptacle (J7)

- There is Power OR-ing circuitry in place to prevent over-currenting and current backflow to the source through this connector.
- When the E-102 is operating as a USB peripheral, power can be sourced to the E-102 through this connector.
- When the E-102 is operating as a USB Host, power can be sourced from the E-102 to the downstream peripheral device. In order to support doing this, a jumper needs to be placed across the 2 pins on S1 (this bypasses the power OR-ing circuitry).
    - Total current available for powering peripheral devices is limited by the method used to source this current (whether the card is powered through the J5 & J8, or J4).

USB-UART Receptacle (J4)

- There is Power OR-ing circuitry in place to prevent over-currenting and current backflow to the source through this connector.

When power is supplied to the E-102 through either the USB-OTG or the USB-UART receptacles, power consumption should be limited to the USB specified 2.5W. Sourcing power through both the USB-OTG and the USB-UART receptacles will allow for up to a 5W power budget. When power is sourced through the GPIO connectors, power consumption is limited by the power supplies onboard. Refer to "Table - Power Specifications" for more detailed information about power consumption.

Table - Power Specifications

	Minimum	Nominal	Maximum
DC Input Voltage J5, J8, J7, J4	**4.75V**	**5.0V**	**5.25V**
PS Power	**TBD**	**TBD**	**TBD**
PL Power	**TBD**	**TBD**	**TBD**

Errata

Board Revision History

Table - Board Revision History

Version	Release Date	Description
Rev A	Jul-12	Prototype Release – ES Silicon
Rev B	Oct-12	First Production Release – ES Silicon

Document Revision History

Table - Document Revision History

Date	Version	Changes
Nov-12	1.00	Initial Release

Legal Notices

Pico Computing products are not authorized for use in life-critical applications, or where device failure could cause injury or disruption of service.