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Letter

Ultralow-power instant-on photon-pair counting and photon-entanglement analysis

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Abstract
The latest breakthroughs in quantum technologies, such as satellite quantum communications, present new challenges, imposing stringent restrictions on weight, size, and power consumption of quantum information systems. Here, we show that nonlinear and quantum optics provides powerful resources to confront these challenges by offering attractive solutions for photon-pair counting and quantum-entanglement detection. We demonstrate a low-cost, readily miniaturizable photon-pair counting module, which consumes less than 100 μAh during a sub-10 ms power-on/off measurement cycle, thus providing a meaningful performance as a promising component for satellite quantum technologies.

Keywords: nonlinear optics, optical parametrical processes, quantum optics

(Some figures may appear in colour only in the online journal)

Satellite quantum information relays [1–3] are of considerable interest for long distance quantum key distribution [4] and space-based secure communications [5]. The exosphere, however, presents a challenging environment for quantum communications due to prohibitive restrictions on the weight, size, and power requirements of satellite components needed for creating quantum relays. Recent advances in radiation tolerant detectors [6–8] and quantum photonics [9–11] have facilitated compact space-based single-photon detectors [12] for use in satellite quantum information systems, but further improvements to size, weight, and power requirements of the processing and analysis back-end of these detectors is possible with the advent of fast booting, low power field-programmable gate array (FPGA) processing solutions.

The FPGA has already been instrumental in the development of high count rate, precision multichannel Geiger mode detectors for a wide variety of event counting applications, including quantum key distribution and photon entanglement studies using single and entangled photon emitters [13–16], multiphoton microscopy [17], positron emission tomography [18], and random number generation [19, 20]. However, FPGA elements used in these counting solutions have also suffered from power requirements in excess of several hundred milliwatts, and possess boot-up/configuration times in excess of 100 ms [21, 22], making them unsuitable for use in a portable measurement instrument.

With the advent of low power, instant-on FPGA replacements [23] for traditional complex programmable logic

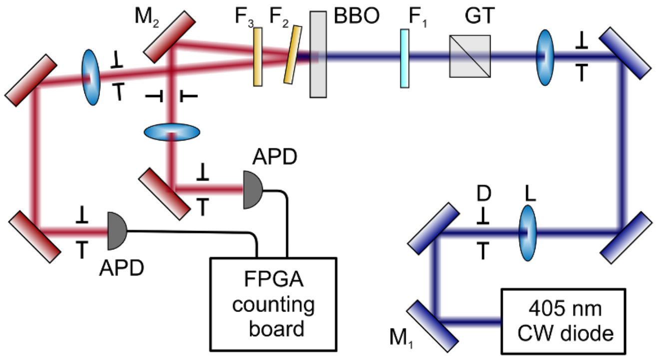

Figure 1. Experimental setup for testing FPGA platform compact low power photon counting module, consisting of a 405 nm continuous wave (CW) diode laser collimated by telescope lenses (L) through a set of diaphragms (D) and a Glan–Taylor polarizer (GT) and then focused onto a type II beta barium borate (BBO) crystal and recollimated (F1, F2, F3). The entangled signal and idler SPDC components were separated by a semicircular mirror (M) and coupled into a pair of avalanche photodiodes (APDs) whose output was analyzed by an FPGA counting board.

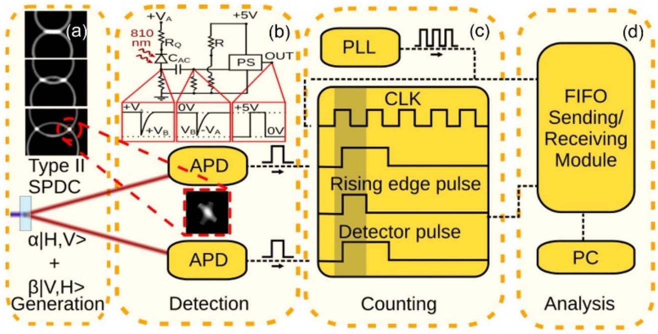

Figure 2. (a) Signal/idler rings from SPDC source with overlap separation tuned by angle adjustment between pump beam and SPDC crystal axis. (b) Spatially isolated overlap region coupled into APDs, with associated APD circuit diagram. (c) Timing diagram of photon counting and coincidence detection circuit within FPGA fabric. (d) Data I/O block of FPGA.

devices, a compact, ultra-low power satellite deployable photon counting module is now practical. The aforementioned FPGAs are capable of maximum power envelopes of under 2 watts at full performance load and a power-on time of under 10 ms, drawing just 100 μAh per on/off power cycle. The small chip package and the inclusion of a low-power avalanche photodiode (APD) module [9, 24] enables the creation of a compact, ultralow power photon counting module amenable to use in satellite quantum communication uplinks.

This compact photon counting module was realized by incorporating a hermetically sealed SAP500 APD into a transistor–transistor logic pulse-shaping circuit connected to a multichannel MAX 10 FPGA photon counting board and tested by the measuring second order coherence from a source of entangled photon pairs.

The experimental setup for testing the instant-on photon counting module utilizes a 500 mW 405 nm diode laser and a spontaneous parametric down-conversion (SPDC) crystal as a source for production of 810 nm polarization entangled photons (figure 1). The resulting SPDC signal was filtered using an 810 nm bandpass filter.

The SPDC output from the crystal was imaged onto a Trius SX674 CCD astronomical camera in order to verify the presence of the characteristic emission cones and their corresponding intersections where polarization entangled photons exist. An actively controlled thermoelectric cooler element was used to hold the laser source at a fixed, specified temperature that corresponded to emission at 405 nm. The SPDC source then provided emission centered on the 810 nm band pass region of the filter, ensuring symmetric signal-idler rings and therefore identical photons (figure 2(a)). The angle between the SPDC crystal and the input 405 nm laser was tuned in order to achieve the desired separation between points of overlap between the signal and idler rings so that each overlap region could be individually addressed and analyzed. Polarization entangled photons in the region of intersection between the signal and idler cones were separated from the remainder of the SPDC signal with a pair of diaphragms (figure 2(b) (inset)).

The photon detectors were created from a Laser Components SAP500 APD with 40% peak quantum efficiency and an optimal dark count rate of 1000 cps at a set temperature of 273 K from the TEC. The SAP500 APD was affixed cooled with an attached TEC, and the pair were enclosed in a hermetically sealed custom-machined aluminum housing possessing an antireflection-coated window for signal coupling to the diode. The diode was then connected to a custom built avalanche pulse shaping circuit (figure 2(b)).

The operating principle of the APD circuit (figure 2(b)) involves reverse biasing the APD into the metastable voltage breakdown region of the diode. In this state, the diode is extremely sensitive to any electromagnetic perturbations, and when a single photon is absorbed by the depletion region of the pn-junction, the photoelectron generated is accelerated in the large bias electric field, and impacts a nearby region in the lattice, ionizing multiple lattice electrons. These electrons are also accelerated by the field and impact further areas of the p–n junction, triggering a cascade of current in the form of a negative voltage avalanche with a gain often on the order of 10^6 charge carriers, signaling the absorption of a single photon. This avalanche manifests as a 5 ns long drop in voltage, which is arrested when the current increases to the point that the avalanche voltage, V_A, falls below the APD breakdown voltage. The use of a quench resistor limits the avalanche current to safe levels, preventing thermal overload of the APD, and forms an RC circuit with the intrinsic cathode-anode capacitance of the APD. The RC time of this circuit determines the refresh time of the avalanche process, and thus defines the maximum count rate of 1 Mcps for the herald detector.

An AC decoupling capacitor removes the V_{BD} bias from the avalanche signal, and this signal is passed into a pulse shaping circuit (figure 2(b)) consisting of an LT1719 constant level discriminator (CLD) referenced to 20 mV and a 74HC74 positive-edge-triggered flip–flop. The output of the CLD swings high to its +5 V rail when it receives a voltage higher than the reference voltage, and swings low to the 0 V rail when the voltage is below the reference. This creates a short lived

5 V signal with a ringing edge, which is converted to a single 5 V square pulse by the flip-flop, indicating the absorption of a photon by the circuit. The overall current draw of this circuit is less than 2 mA at full load. In order to detect the generation of a pair of entangled photons, simultaneous measurements on two photon detection channels must be possible. Normally two high temporal resolution photon counting boards would be used, however these devices are expensive, large, and have a large power envelope. Thus a single counting board with multiple channels is desired.

In recent years, multichannel coincidence counting devices have garnered significant interest for use in the field of quantum information [25–27]. One technology used to achieve multi-channel coincidence counting is the FPGA counting board. An FPGA is a circuit designed to the term field-programmable, in that the firmware can be modified without modifying any physical properties of the device. Doing this requires the use of a hardware description language (HDL), of which Verilog and very-high-speed integrated-circuit hardware description language are the most popular variants. FPGAs contain a matrix of programmable logic blocks and programmable interconnects. By configuring the interconnects, simple logic element like AND, OR, and NOT gates can be formed for use in more complex logic operations. The FPGA has several advantages including low cost, high speed, high signal processing rate, high reconfigurability, and massively parallel data processing. Recent FPGA solutions have demonstrated vast improvements in overall power usage and footprint.

The FPGA based counting board is comprised of an Intel MAX 10 FPGA evaluation board, with a phase-locked loop generating periodic pulses at a rate of 50 MHz. This FPGA based counting board possesses a 10-fold better time resolution than a standard commercial multichannel card (5 MHz), thereby reducing the probability of detecting accidental coincidence while maintaining capacity for multiple detection channels. The detected photon pulse is input to the edge detection module of the counting board and stored for one clock cycle, whereupon it is output to the first-in-first-out (FIFO) communication module. For one output clock (CLK) period, the edge detection module transfers the counts detected in each channel to the FIFO data sending module (figures 2(c) and (d)). After the FIFO sending module receives the count data, it transfers the count data to a FT232H high-speed FIFO to USB 2.0 to module connected to a PC where the data is analyzed.

The FPGA counting board was first tested to ascertain the minimum off/on power cycling period between first application of V_{CC} to when the configuration pin goes high. This was accomplished by monitoring the V_{CC} output of the main regulator, the nSTATUS pin that indicates that the measurement program has begun being loaded onto the FPGA, and the CONF DONE pin indicating whether or not the measurement program has finished loading and that the FPGA is ready for measurements. The total power-on initialization time from the beginning of the V_{CC} voltage ramp to when the CONF DONE pin goes high was found to be approximately 6 ms (figure 3(a)), indicating that a 4 ms measurement window can be included in a power off/on measurement cycle of 10 ms.

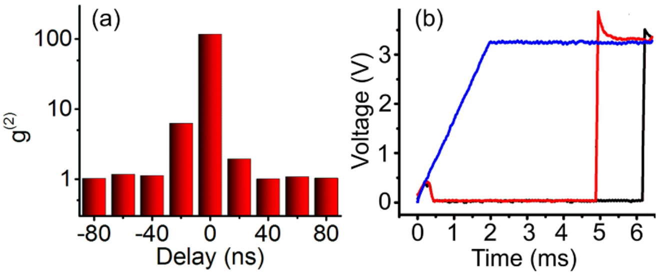

Figure 3. (a) Power on initialization time from beginning of V_{CC} ramp (blue trace) until CONF DONE pin goes high (black trace). nSTATUS pin indicates beginning of program load sequence (red trace) (b) $g^{(2)}(\tau)$ measurement taken for photon count rates at 10^3 cps (red bars).

The SPDC source was then tested to ascertain a maximum $g^{(2)}(\tau)$ and number of photon coincidences measured during the 4 ms measurement window by coupling the cone intersections into a pair of photon detectors. Maximum count rates of 10^5 were measured by the photon counters, and the coincidence rate was found to be approximately 10% of the count rate, indicating that approximately 10^2 coincidence counts can be detected within the 10 ms off/on cycle of the detector. $g^{(2)}(\tau)$ was plotted as a function of delay, and a stable value of 100 was found for photon count rates and coincidence rates of 10^3 cps and 10^2 respectively (figure 3(b)). Peak $g^{(2)}(\tau)$ values of over 1000 were also measured.

To summarize, a low power compact photon counting module drawing less than 100 μAh per power on/off cycle and capable of a less than 10 ms power on/off measurement cycle was demonstrated and tested using a source of entangled photons, exhibiting a maximum second order degree of coherence on the order of 1000. These efforts have laid the groundwork for future developments of low-power, portable instant-on FPGA-based multichannel photon counting modules. As one envisaged application, the approach developed in this study can help improve the performance of quantum-correlation and plasmonic structured illumination microscopy. Research in this direction is currently in progress [28, 29]. Other applications may include NOON-state generation [30, 31] and, more generally, quantum-entanglement engineering beyond the class of biphotonic states. Finally, the methods demonstrated in this paper can facilitate the development of a photonic toolbox for a rapid detection of virus infections [32–34].

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