XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC17VXX, XC17SXXA Family

Description

The XC17VXX(17V08 and 17V16 are described in another specification) and XC17SXXA Configuration PROMs provide easy-to-use, cost-effective configuration memory for Xilinx Field Programmable Gate Arrays.

These devices use a simple serial-access to configure one or more LCA devices. The user can select the polarity of the reset function by programming a special bit. These devices are fully compatible and can be cascaded with other members of the XC1700 family.

Pin Assignments:

Function	(PD8/VO8)	*(PC20/SO20)	VQ44	PLCC44
Vpp	7	18	35	41
Vcc	8	20	38	44
Gnd	5	11	18	24
CLK	2	3	43	5
$\overline{CE}$	4	10	15	21
Reset/$\overline{OE}$	3	8	13	19
$\overline{CEO}$	6	13	21	27
D0	1	1	40	2

*** Note: The pin definition of the PC20 package is different from the PC20 package for the older PROM devices (eg. XC1701L-PC20)**

Programming Overview

The XC17VXX and XC17SXX devices are one-time programmable (OTP) devices, organized as follows:

XC17V04

4,194,304 X 1 bit

XC17V02

2,097,152 X 1 bit

XC17V01 **

1,679,360 X 1 bit

XC17S200A

1,679,360 X 1 bit

XC17S50A, XC17S100A, and XC17S150A

1,048,576 X 1 bit

XC17S15A and XC17S30A

524,288 X 1 bit

XC17S300A

2,097,152 X 1 bit

**** Note: The density of the XC17V01 is different from the older devices in this density (i.e. XC1701L)**

The XC17VXX and XC17SXXA PROM are internally organized in rows, each row containing multiple 64 bit words. Additional non-data rows are used to read the Manufacturer's/Device ID and set the Reset Polarity and cannot be used to store configuration data. The device programmer should prompt the user for the desired Reset Polarity. Figure 1 shows the flow of how the PROMs are programmed. See Figure 2 for the programming cycle overview and Figure 4 for the details of the programming cycle.

Enter Programming Mode

The programming mode is entered by holding $\overline{CE}$ and $\overline{OE}$ High with V_{PP} at V_{PP1} for two rising clock edges, then lowering V_{PP} to V_{PPNOM} for one more rising clock edge (See Figure 3). Once in the programming mode, the following functions are available.

Read Manufacturer's/Device ID

All of the PROMs contain a Manufacturer's and Device identification code. Prior to attempting to program or verify the device, the device programmer should read this code and verify that it is the correct code for the device selected by the user. If not, display message **"Manufacturer or Device ID Error."**

To read the Manufacturer's/Device identification code, first enter the programming mode. While holding $\overline{CE}$ High, $\overline{OE}$ Low, apply the following clock signals to the clock pin to access the ID row.

ID Row clock count

65632 for XC17V02 and XC17V04

65632 for XC17S300A

26256 for XC17V01

26256 for XC17S15A / 30A / 50A / 100A / 150A / 200A

Then bring $\overline{OE}$ High and $\overline{CE}$ Low*. The first bit of the identification word is present when $\overline{CE}$ goes Low and does not require a clock. Apply 15 additional clock signals to the CLK pin to read the complete device ID from the DØ pin.

The Manufacturer's/Device ID

Consisting of 2 bytes of data. The first byte contains the JEDEC assigned Manufacturer's ID code for Xilinx (C9). The first four bits of the second byte define the density of the PROM, while the last four bits of the second byte contain specific programming algorithm information, currently:

2 for XC17V01, XC17V02 and XC17V04

3 for XC17S15A, 17S50A and 17S200A

4 for XC17S30A, XC17S100A and XC17S300A

5 for XC17S150A

The data is read out MSB first.

The density codes are defined as follows:

9 for XC17S15A and XC17S30A

D for XC17S50A, XC17S100A, and XC17S150A

1 for XC17V01, XC17S200A

3 for XC17V02, XC17S300A

B for XC17V04

Loading and Programming a Data Word

The data word is shifted into the SPROM on DØ, one bit at a time, on the rising edge of the clock, while $\overline{CE}$ and $\overline{OE}$ are High. The data word counter is temporarily held in internal latches until the address is advanced to the next address, and is programmed into the memory as an entire word upon strobing the device with V_{PP} at V_{PP1} for 100µs.

The contents of the data word must now be verified at V_{PP2}. The data word is verified on DØ while lowering $\overline{CE}$ and capturing the data while clocking the device 63 times. The first bit of the word (LSB) is present when $\overline{CE}$ goes low. After all 64 bits were read, bring $\overline{CE}$ high and compare the data to the original file data. If the data does not compare, power the device down and issue message: "Device Failed to Program". See Figure 1. If the word compares, increment the word counter as described below.

Increment the Address (Word) Counter

After successfully programming a data word, the address counter must be incremented. This is done on the rising edge of the clock while $\overline{CE}$ is High and $\overline{OE}$ is Low.

Setting RESET Polarity

The polarity of the Reset/$\overline{OE}$ pin may be made active by writing zeros into a dedicated location (See Figure 5). This special mode bit is located outside of the user array. In order to program this bit, you need to follow the following sequence. 1) Enter the programming mode 2) lower Reset/$\overline{OE}$ while holding hold the Data pin Low 3) strobe the clock to advance the address pointer (see table below), 4) raise the Reset/$\overline{OE}$ pin 5) load the data latches with all zeros (see Load a Data Word above), and 6) strobe $V_{PP\ at}$ V_{PP1} for T_{PGM}. This special bit has to be verified (sensed) at V_{PP2} while in programming mode.

Clocks required to advance to Reset Polarity Row

65536	for	XC17S300A, XC17V02 and XC17V04
26240	for	XC17V01 and XC17S200A
16384	for	XC17S15A / 30A / 50A / 100A / /150A

Note: The Reset Polarity is actually only the MSB of the data word. Be careful not to have $\overline{CE}$ and $\overline{OE}$ Low at the same time, as this causes the device to exit programming mode.

Sensing the RESET bit

To sense or verify the polarity of the reset bit 1) enter the programming mode 2) lower Reset/$\overline{OE}$ while holding the Data pin high 3) strobe the clock to advance the address pointer to the Reset bit (see previous table) 4) set Reset/$\overline{OE}$ High 5) set $\overline{CE}$ Low and 6) sense the $\overline{CEO}$ pin. If $\overline{CEO}$ is High, the user bit is programmed and in the active low state. If $\overline{CEO}$ is Low, the user bit is unprogrammed (default) and in the active high state.

Exit Programming Mode

To exit the programming mode, remove power from the device, or lower both $\overline{CE}$ and $\overline{OE}$, per Figure 6.

Stand Alone Read Of Data Bits (Normal Mode)

The verify operation should be performed after programming. Power up the device and read the data bits out bit-by-bit in normal serial mode (see Figure 7). A margin voltage (difference between V_{PP} and V_{CC}) is applied to the device to ensure charge retention on each programmed bit. Set V_{CC} to V_{CCVFY} and V_{PP} to V_{PPVFY}. When in normal mode, the Reset/$\overline{OE}$ signal should be driven active high if the reset polarity bit was unprogrammed (logic "1"). It should be driven active low if the reset polarity bit was programmed (logic "0").

At the end of the read operation the programmer must confirm that the $\overline{CEO}$ pin has gone low one clock after the last bit is read out.

If the data fails to verify, display message **"Failed Margin Verify"**. If the data verifies, display the message **"Device Passed"**.

Name	I/O	Description
Data0	I/O	The rising edge of the clock shifts a data word in or out of the SPROM one bit at a time.
CLK	I	Clock input. Used to increment the internal address/word counter for reading and programming.
RESET/$\overline{OE}$	I	The rising edge of CLK shifts a data word into the PROM when $\overline{CE}$ and $\overline{OE}$ are high; it shifts a data word out of the PROM when $\overline{CE}$ is Low and $\overline{OE}$ is high. The address/word counter is incremented on the rising edge of CLK while $\overline{CE}$ is held High and $\overline{OE}$ is held Low. Note: Any modified polarity of the RESET/$\overline{OE}$ pin is **ignored** in the programming mode.
$\overline{CE}$	I	The rising edge of CLK shifts a data word into the PROM when $\overline{CE}$ and $\overline{OE}$ are High; it shifts a data word out of the PROM when $\overline{CE}$ is Low and $\overline{OE}$ is High. The address/word counter is incremented on the rising edge of CLK while $\overline{CE}$ is held High and $\overline{OE}$ is held Low.
GND		Ground pin
$\overline{CEO}$	O	The polarity of the RESET/$\overline{OE}$ can be read by sensing the $\overline{CEO}$ pin. Note: The polarity of the RESET/$\overline{OE}$ pin is ignored while in the programming mode. In final verification, this pin must be monitored to go Low one clock cycle after the last data bit has been read.
Vcc		Vcc power supply pin
V_{PP}		Programming Voltage Supply. Programming mode is entered by holding $\overline{CE}$ and $\overline{OE}$ High and V_{PP} at V_{PP1} for two rising clock edges and then lowering V_{PP} to V_{PPNOM} for one more rising clock edge. A word is programmed by strobing the device with V_{PP} for the duration T_{PGM}. V_{PP} must be held at VCC for normal operation.
V_{CC}		V_{CC} power supply input.

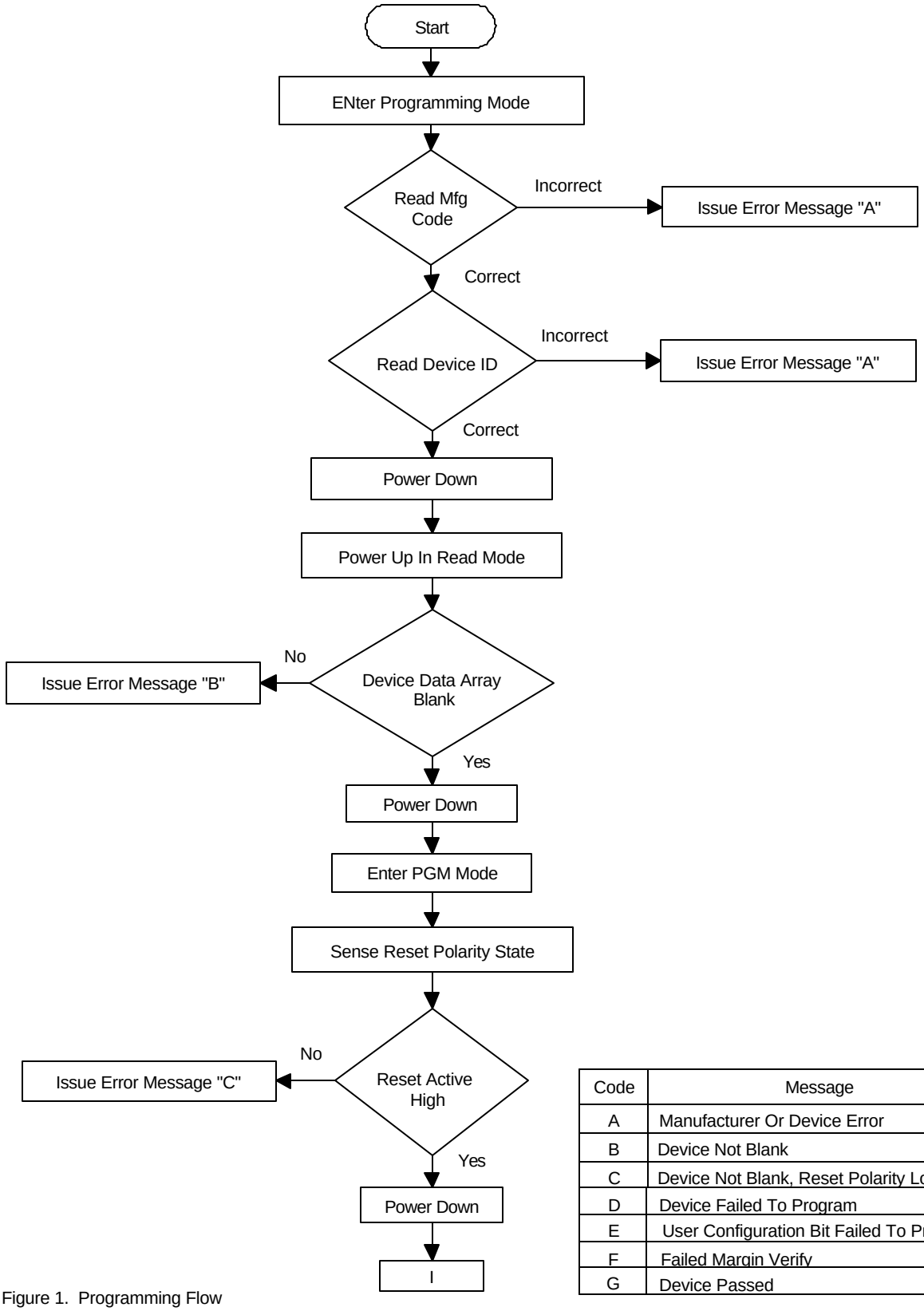
DC Programming Specifications

Symbol	Description	Min	Recommended	Max	Units
V_{CCP*}	Supply voltage during programming		3.3		V
V_{IL}	Low-level input voltage	0.0	0.0	0.5	V
V_{IH}	High-level input voltage	2.4	V_{CC}	V_{CC}	V
V_{OL}	Low-level output voltage			0.4	V
V_{OH}	High-level output voltage	2.5			V
V_{PP1**}	Programming voltage	11.5	11.75	12.0	V
V_{PP2***}	Margin verify voltage during programming		3.7		V
I_{PPP}	Supply current on programming pin			100	mA
V_{CCNOM}/V_{PPNOM}	Nominal Voltage		3.3		V
V_{CCVFY}	Supply voltage during stand alone margin verify		3.3		V
V_{PPVFY}	Margin voltage during stand alone margin verify		3.7		V

* Noise and voltage deviation allowed: 3.3V ± 50 mV.
** No overshoot is permitted on signal. V_{PP} must not be allowed to exceed V_{PP1} max.
*** Noise and voltage deviation allowed: 3.7V ± 250 mV.

AC Programming Specifications

Symbol		Description	Min	Rec.	Max	Units
1	T_{RPP}	10% to 90% rise time of V_{PP}		5		µs
2	T_{FPP}	90% to 10% fall time V_{PP}		5		µs
3	T_{PGM}	V_{PP} programming pulse width	90	100	110	µs
4	T_{SVC}	V_{PP} setup to CLK for entering programming	100			ns
5	T_{HVC}	V_{PP} hold from CLK for entering programming	300			ns
6	T_{SDP}	Data setup to CLK for programming	50			ns
7	T_{HDP}	Data hold from CLK for programming	0			ns
8	T_{SCC}	$\overline{CE}$ setup from programming/verifying	100			ns
9	T_{ON}	Reset Pulse Width		5		ms
10	T_{SCV}	$\overline{CE}$ hold from CLK for programming/verifying	100			ns
11	T_{HCV}	$\overline{CE}$ hold from V_{PP} for programming	50			ns
12	T_{SIC}	$\overline{OE}$ setup to CLK for incrementing address	100			ns
13	T_{HIC}	$\overline{OE}$ hold from CLK for incrementing address	0			ns
14	T_{CAC}	CLK to data valid			20	ns
15	T_{OH}	Data hold from CLK	0			ns
16	T_{CEV}	$\overline{CE}$ low to data valid during program-verify			250	ns
17	T_{CE}	$\overline{CE}$ low to data valid during read			20	ns
18	T_{PRST}	Reset polarity programming pulse width		100		us
19	T_{WKU}	Chip wake up time		100		ms



Code	Message
A	Manufacturer Or Device Error
B	Device Not Blank
C	Device Not Blank, Reset Polarity Low
D	Device Failed To Program
E	User Configuration Bit Failed To Program
F	Failed Margin Verify
G	Device Passed

Figure 1. Programming Flow

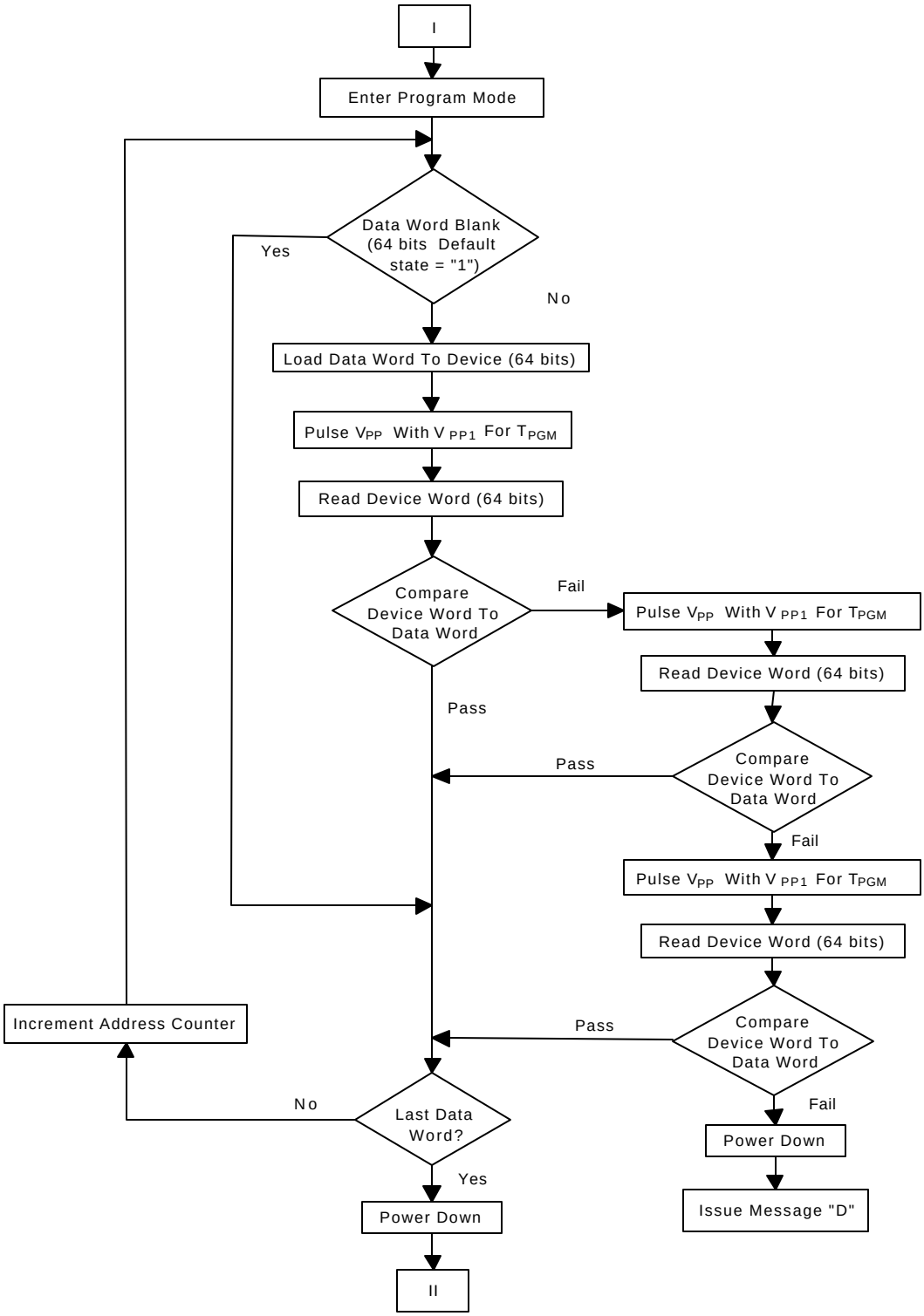


Figure 1. Programming Flow (Continued)

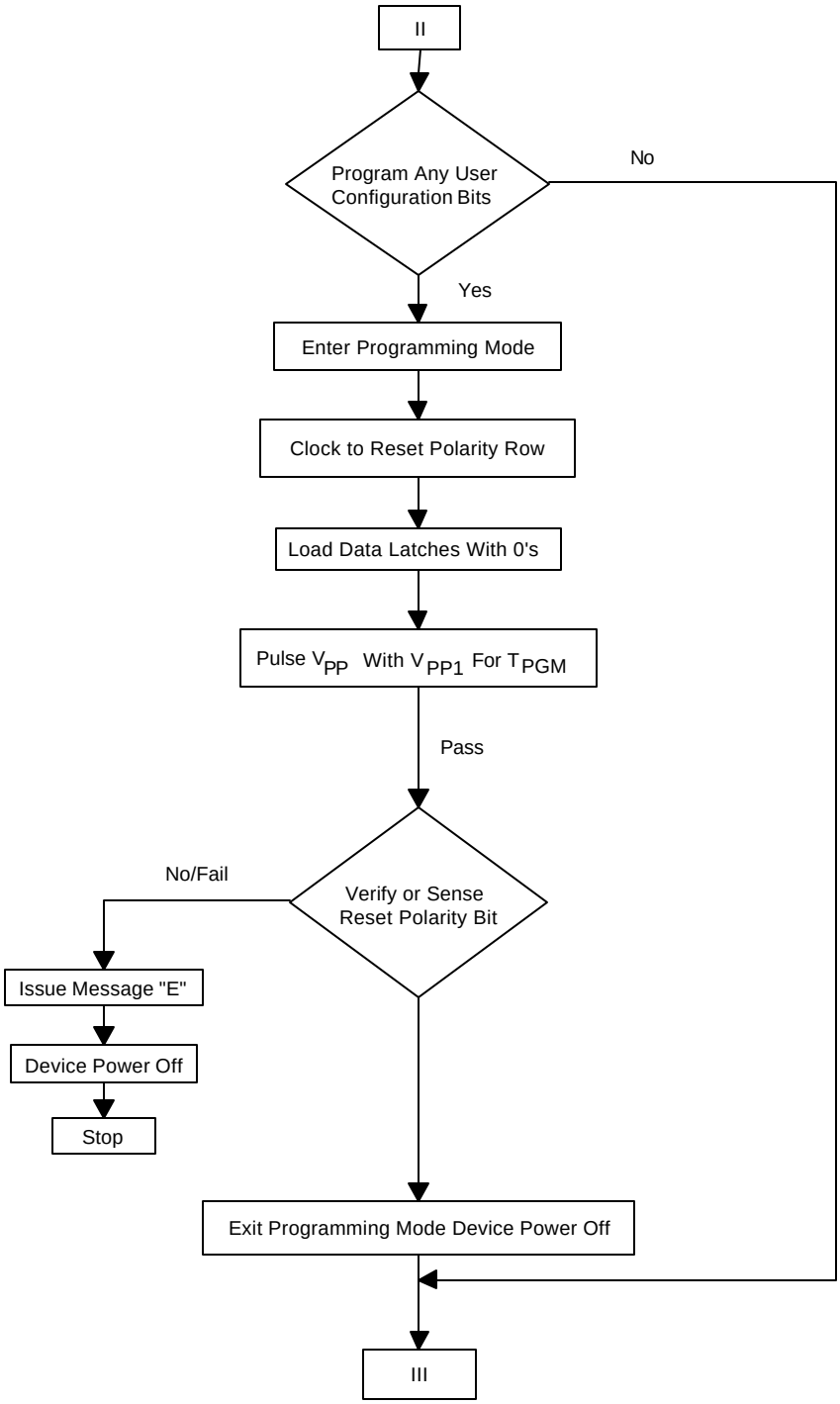


Figure 1. Programming Flow (Continued)

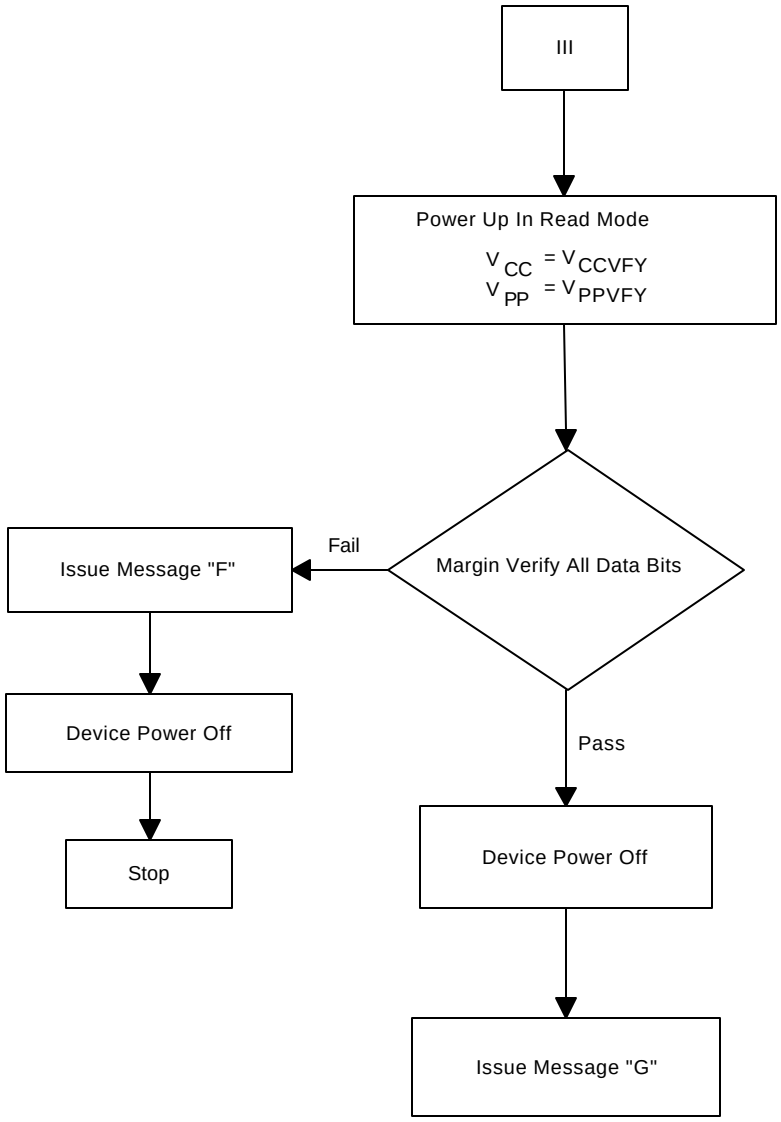


Figure 1. Programming Flow (Continued)

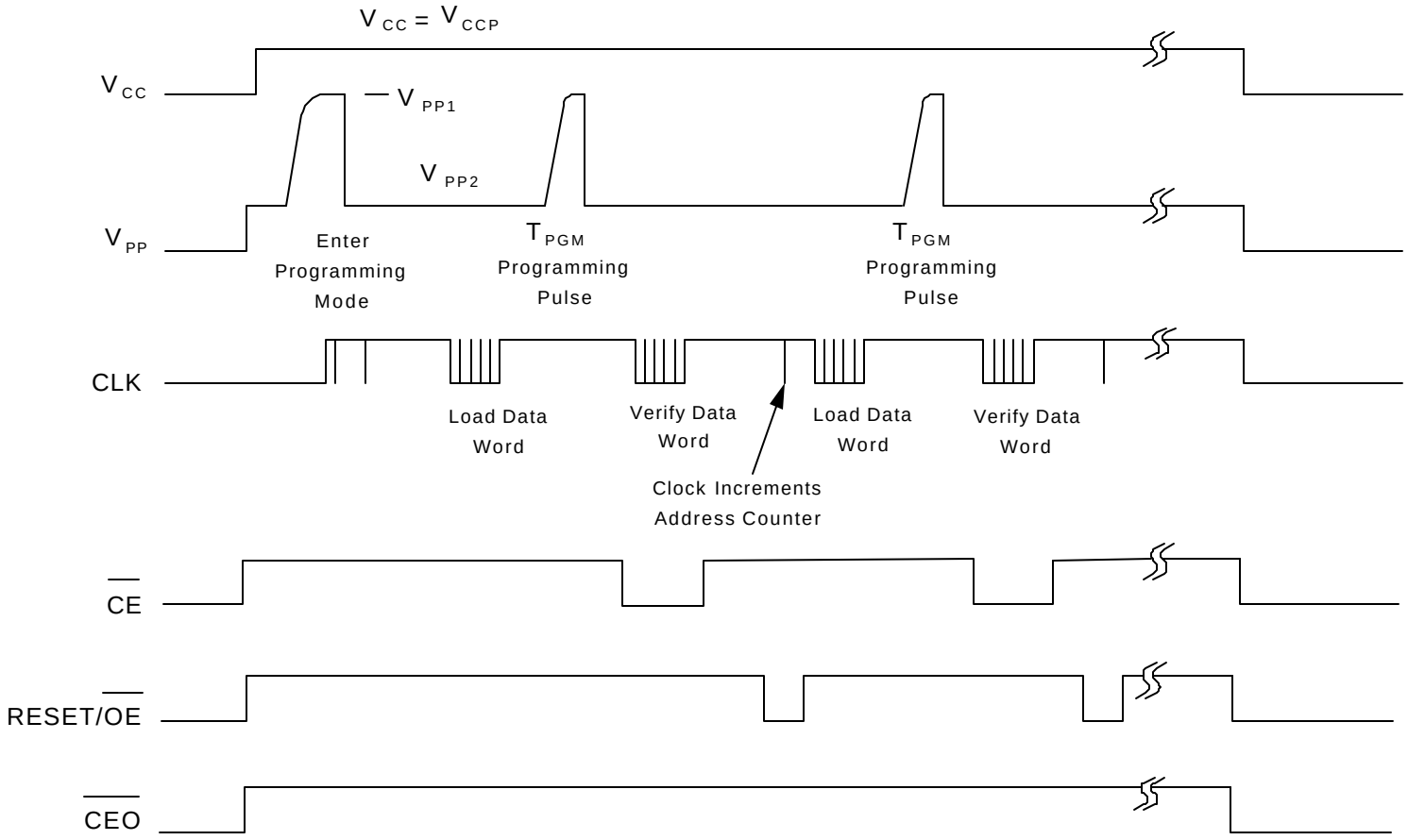
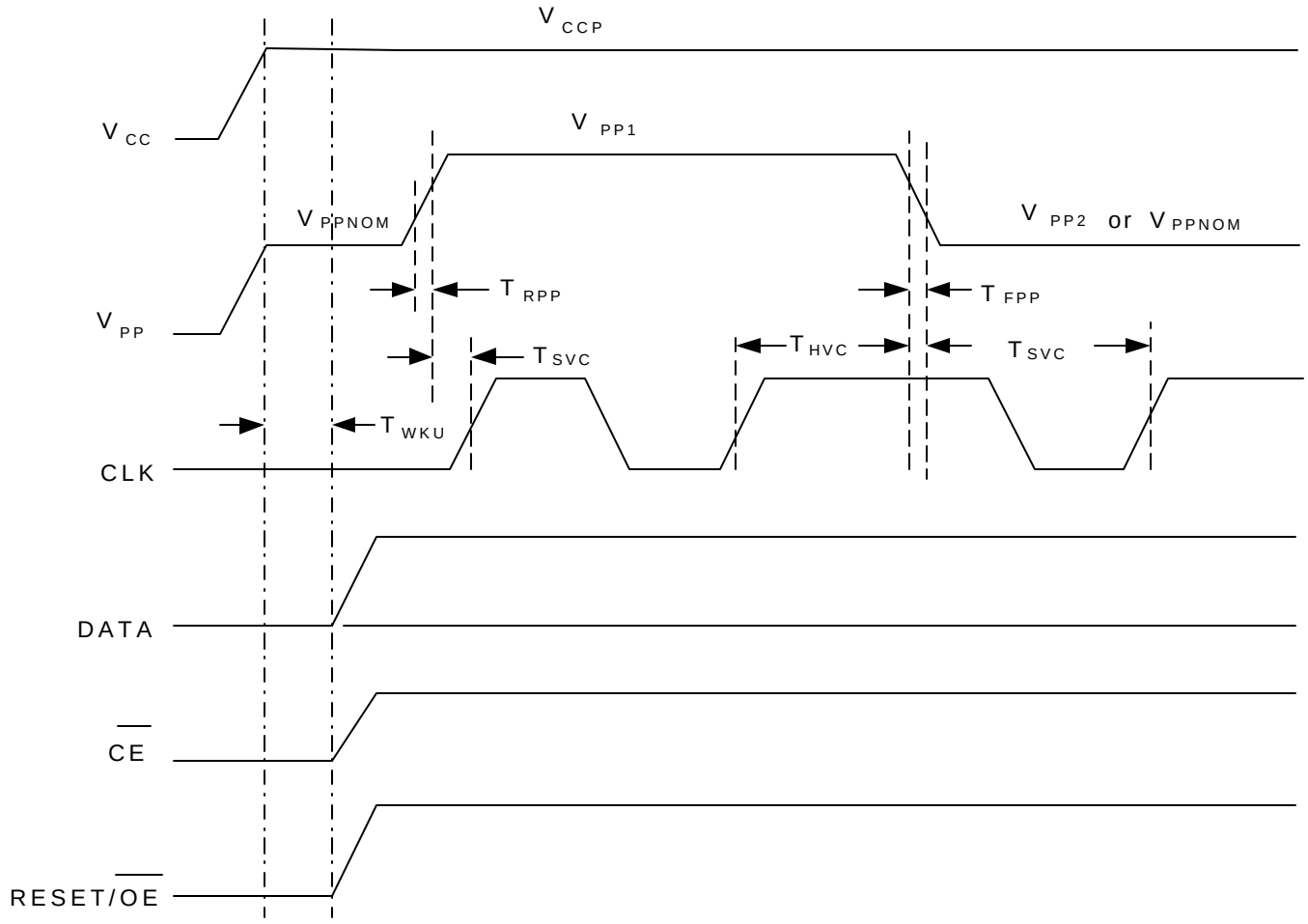


Figure 2. Programming Cycle Overview



If your programming hardware does not allow V_{PP} and V_{CC} to power up simultaneously, then power up V_{PP} followed by V_{CC}.

Figure 3. Enter Programming Mode

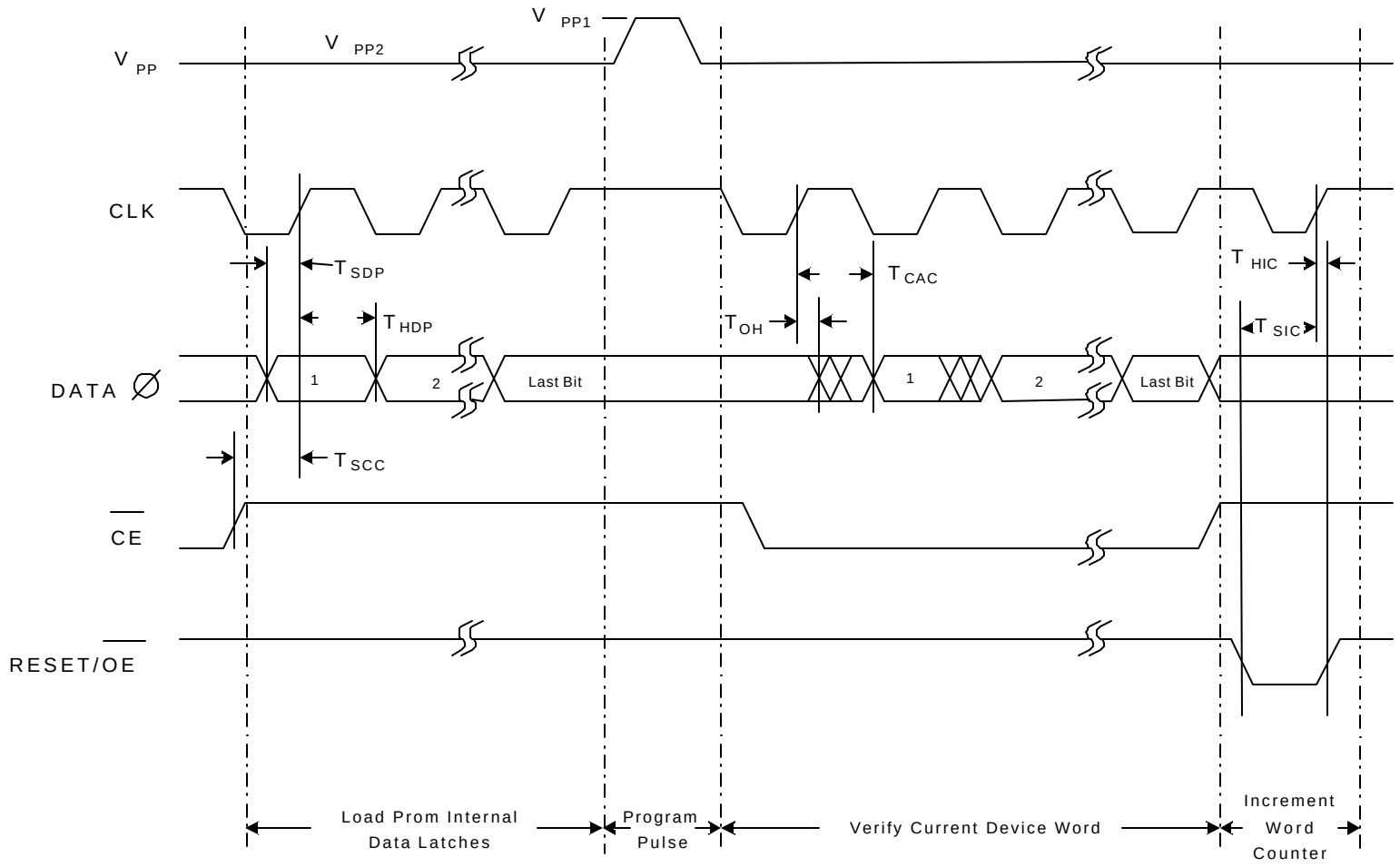
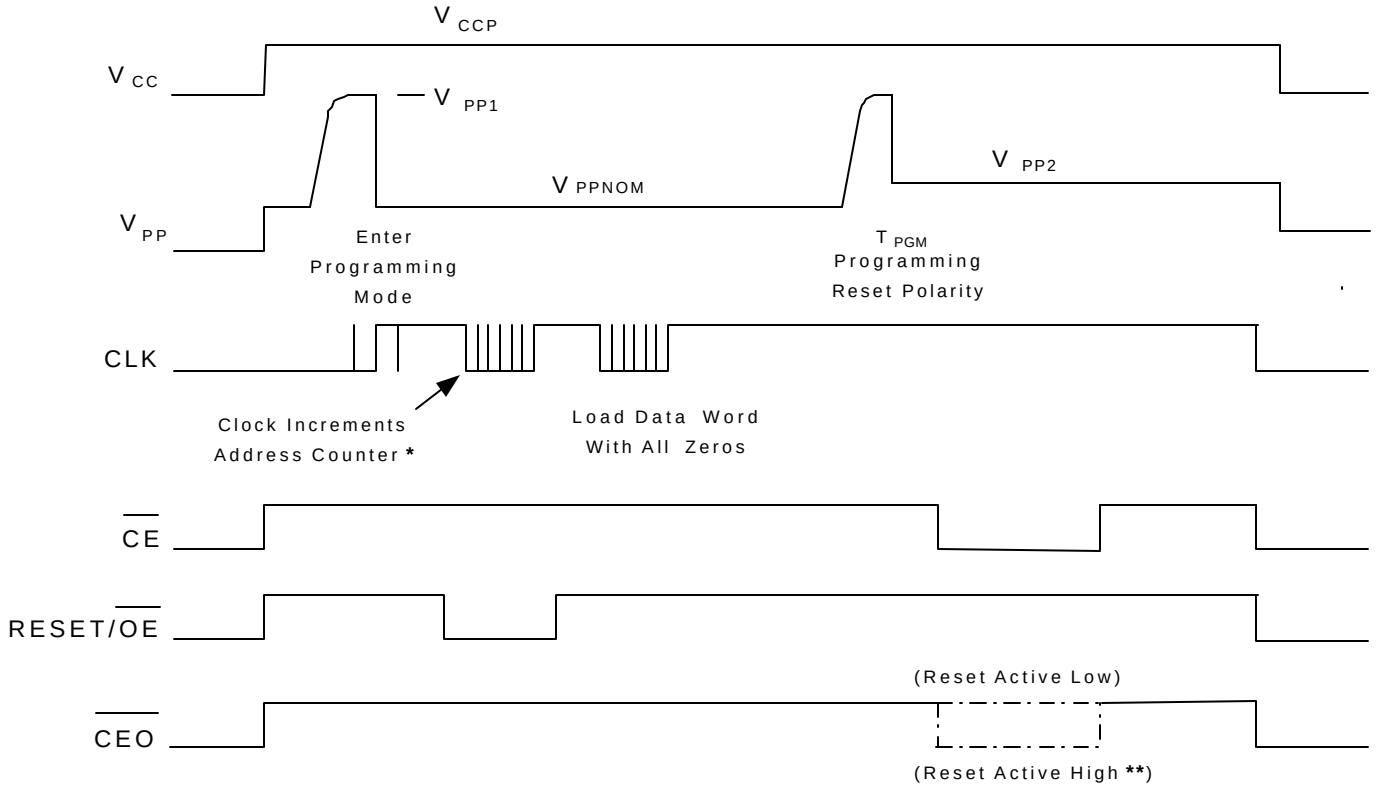


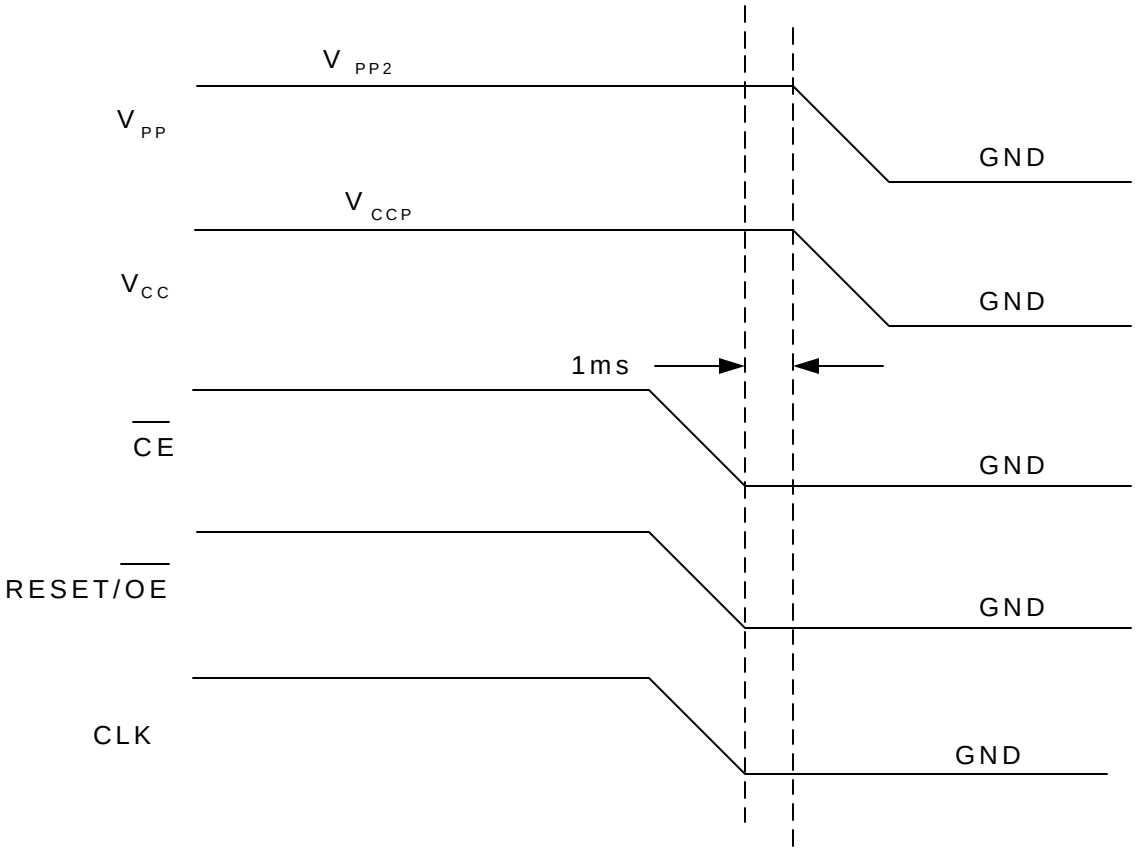
Figure 4. Details Of The Programming Cycle



* Number of Clocks for the Device Reset Polarity Location.

** Operation failed to program the Reset Polarity to the Actice Low state.

Figure 5. Programming User Bit Polarity



If your programming hardware does not allow V_{CC} and V_{PP} to power down simultaneously, then power down V_{CC} followed by V_{PP}.

Figure 6. Exit Programming Mode

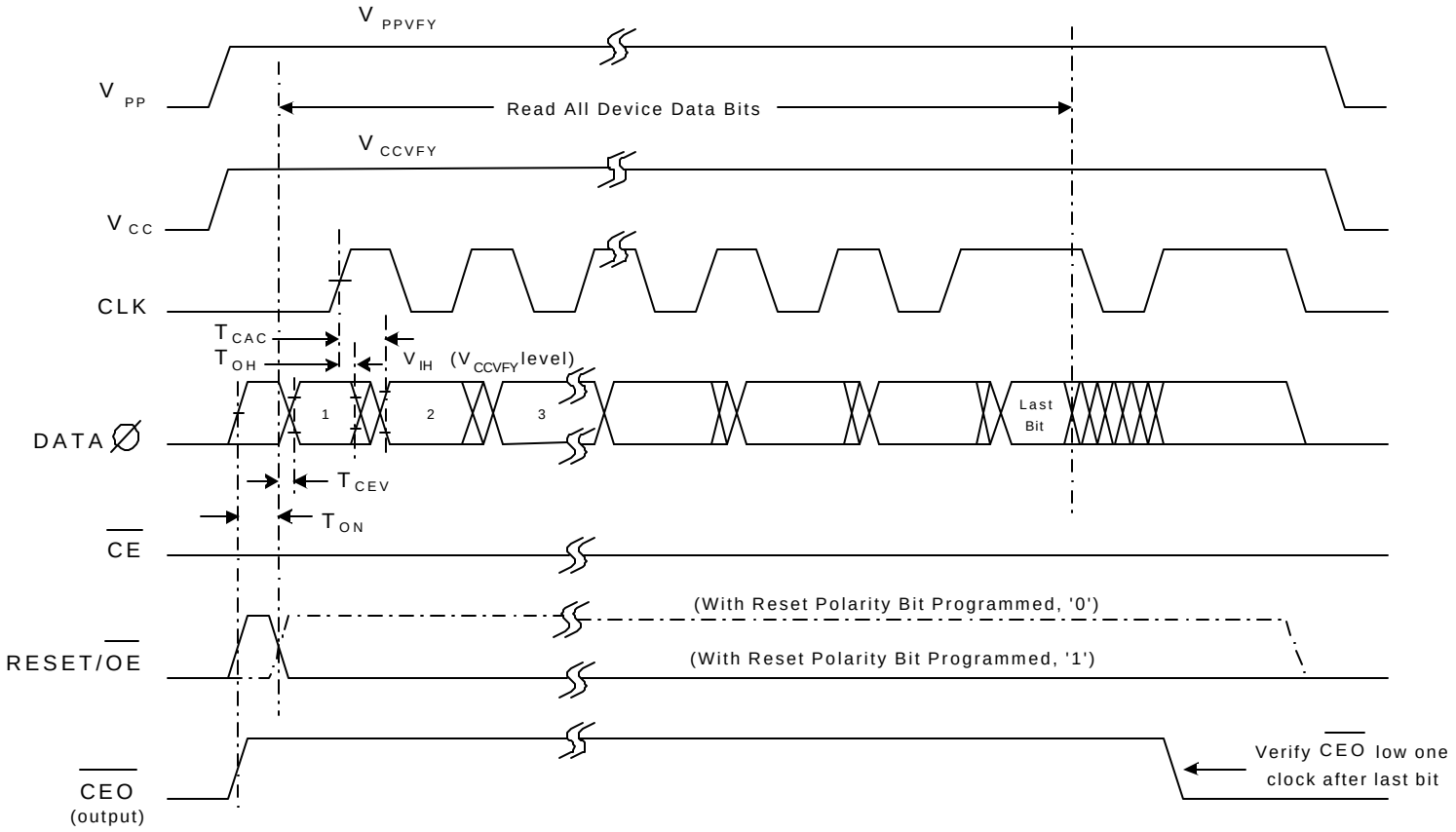


Figure 7. Details Of The Verify Cycle