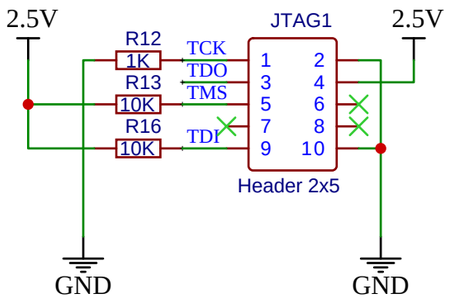
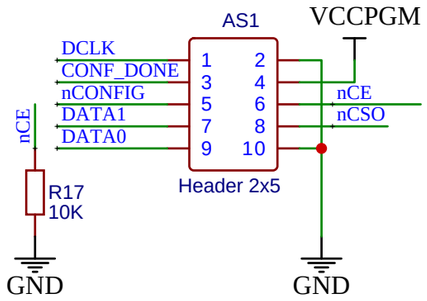
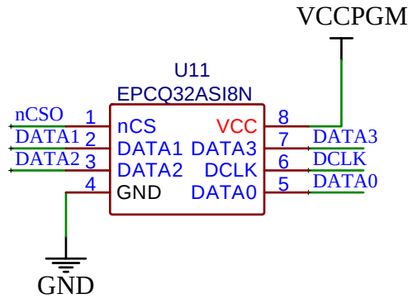


JTAG HEADER

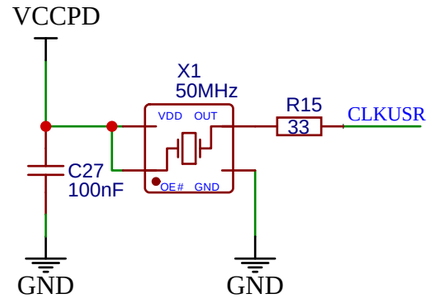


AS HEADER

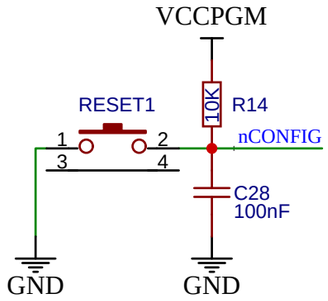


CONFIG EEPROM

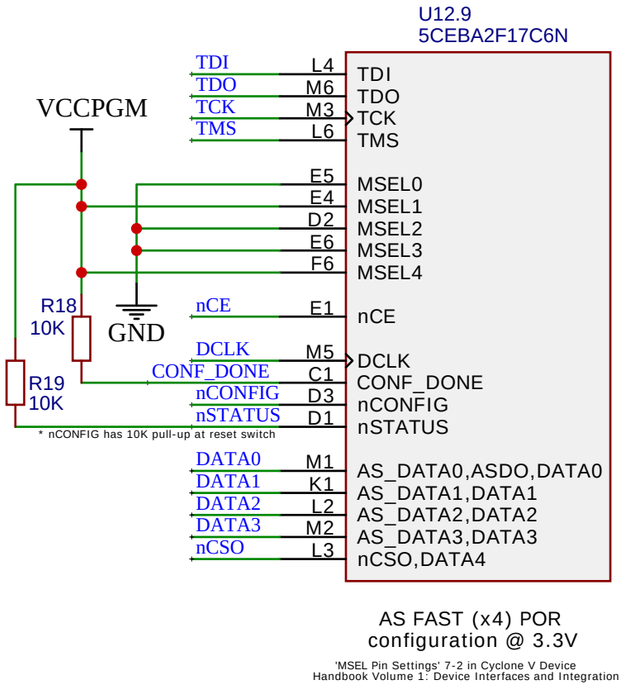
* Minimum 32Mbit EEPROM required for 21Mbit image



50 MHz CLOCK



FPGA RESET



AS FAST (x4) POR
configuration @ 3.3V

'MSEL Pin Settings' 7-2 in Cyclone V Device Handbook Volume 1: Device Interfaces and Integration

TITLE: Configuration & AS/JTAG		REV: 1.0
EasyEDA	Company: 10103	Sheet: 1/1
	Date: 2020-06-25 Drawn By: nockieboy	