

CYCLONE V GPU SCHEMATICS

REVISIONS

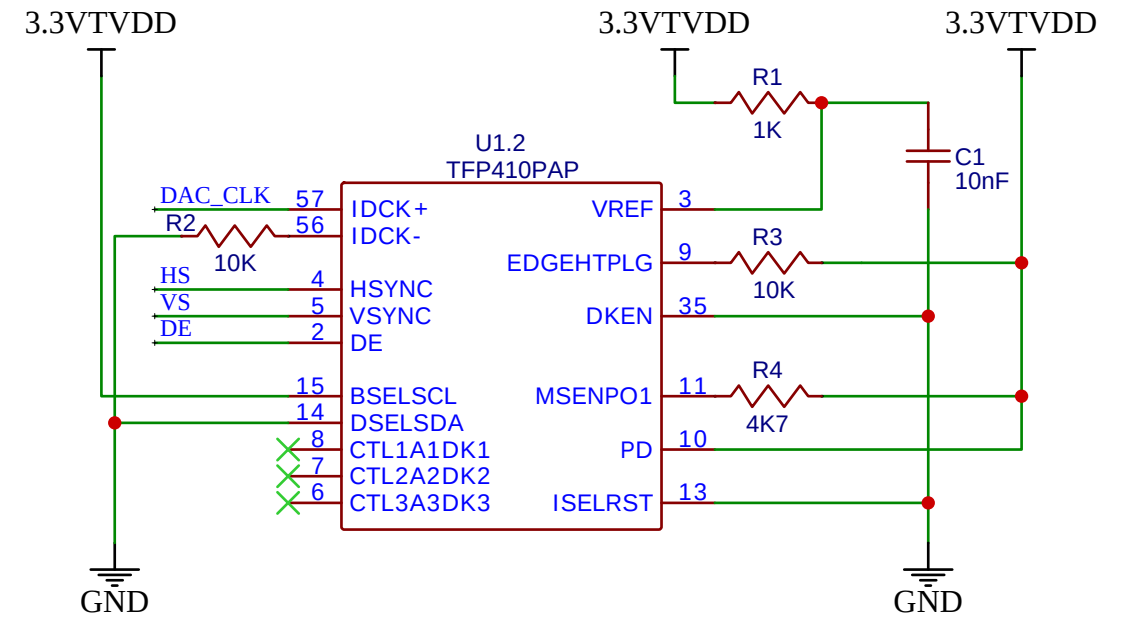
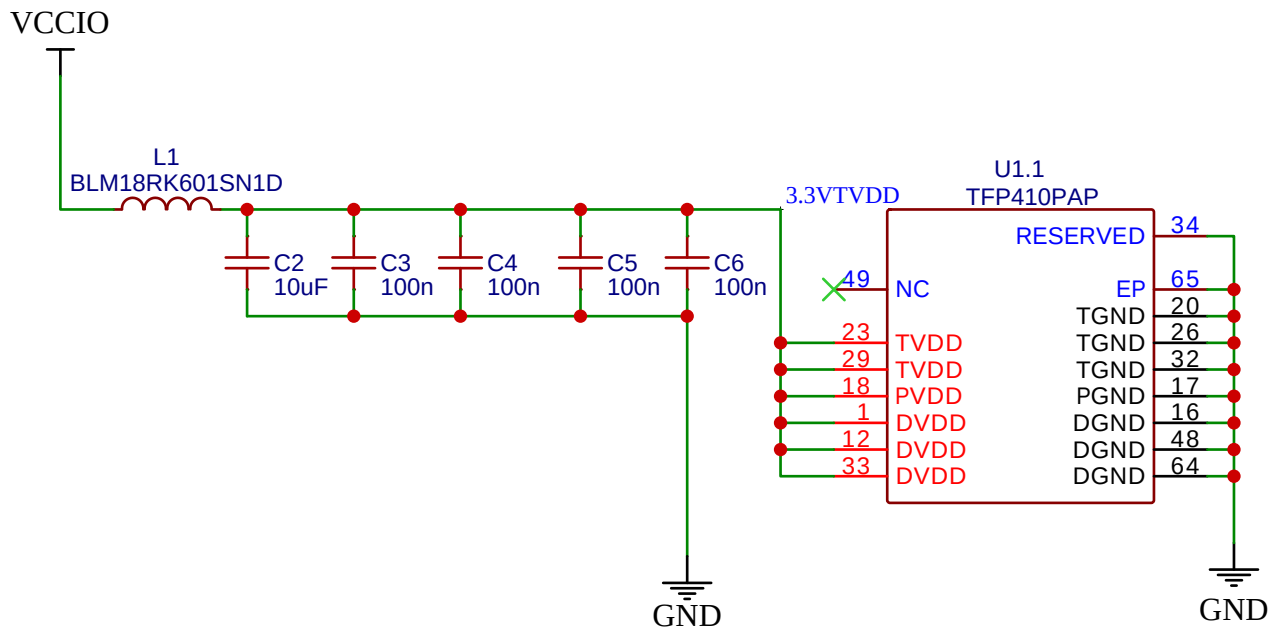
1.0 - Initial draft
1.1 - Replaced MAX5101 DAC with PCM5101A. Replaced wire-wound chokes with fixed inductors.
1.2 - Added decoupling and supply isolation for TFP410.
1.3 - Removed decoupling and supply isolation for TFP410. Added external memory.
1.4 - 10u caps and 100k pull-downs added to audio DAC output. Fixed micro-SD pullups. Corrected DDR-RAM clock pins. Variable-voltage added to U19.
1.5 - Trimpot orientation fixed. VCCA fixed to 3.3VA. Protection diodes added to PS2 port. Links added for AS x1/x4 config. VCCPGM replaced with VCCIO. TFP410 powered from VCCIO.

PAGE CONTENT

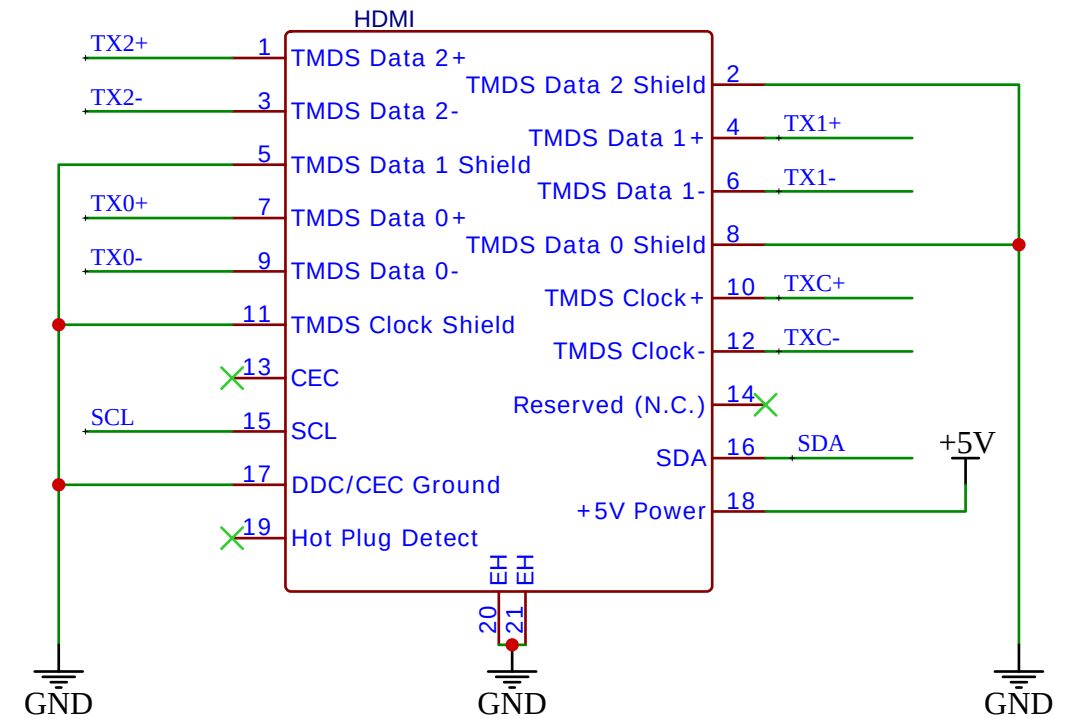
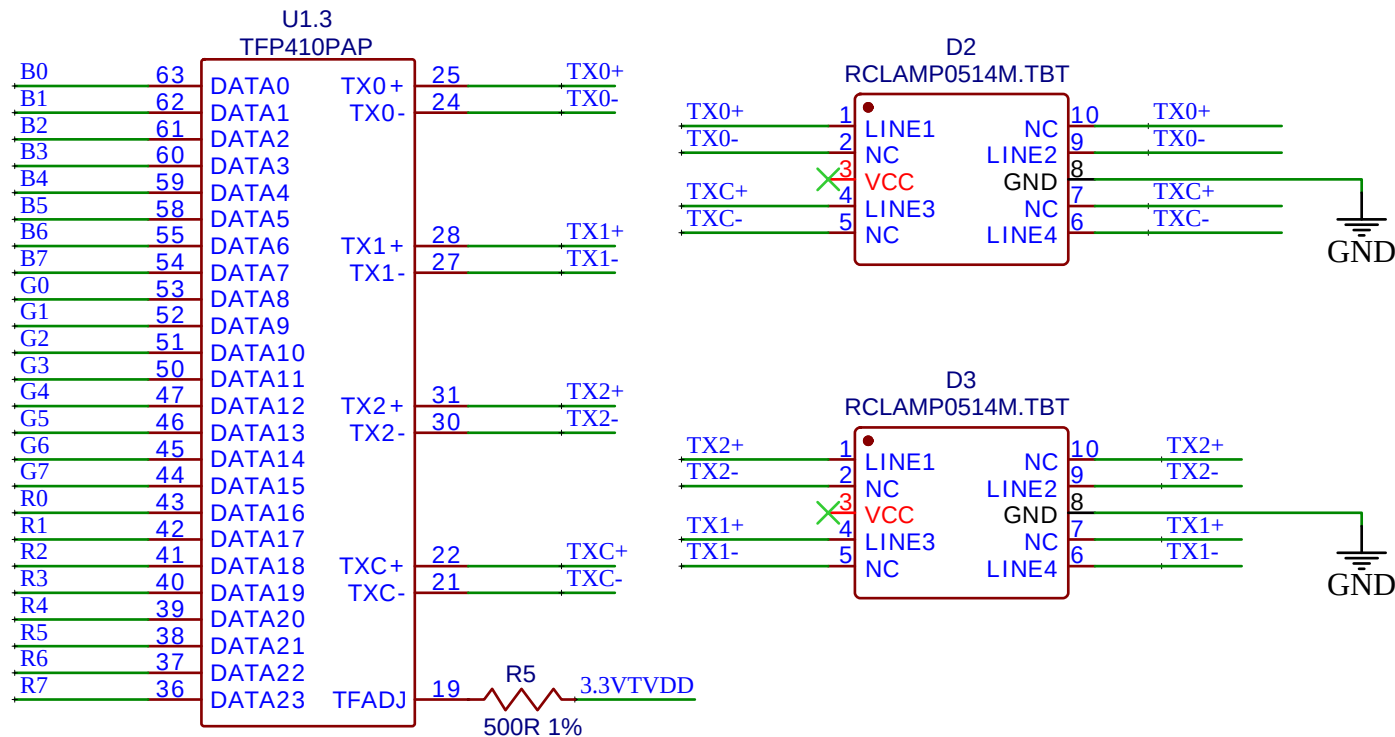
1.	INDEX
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TITLE: Cyclone V GPU		REV: 1.5
	Company: 10103	Sheet: 1/1
	Date: 2020-10-20 Drawn By: nockieboy	

24-bit DVI VIDEO OUTPUT

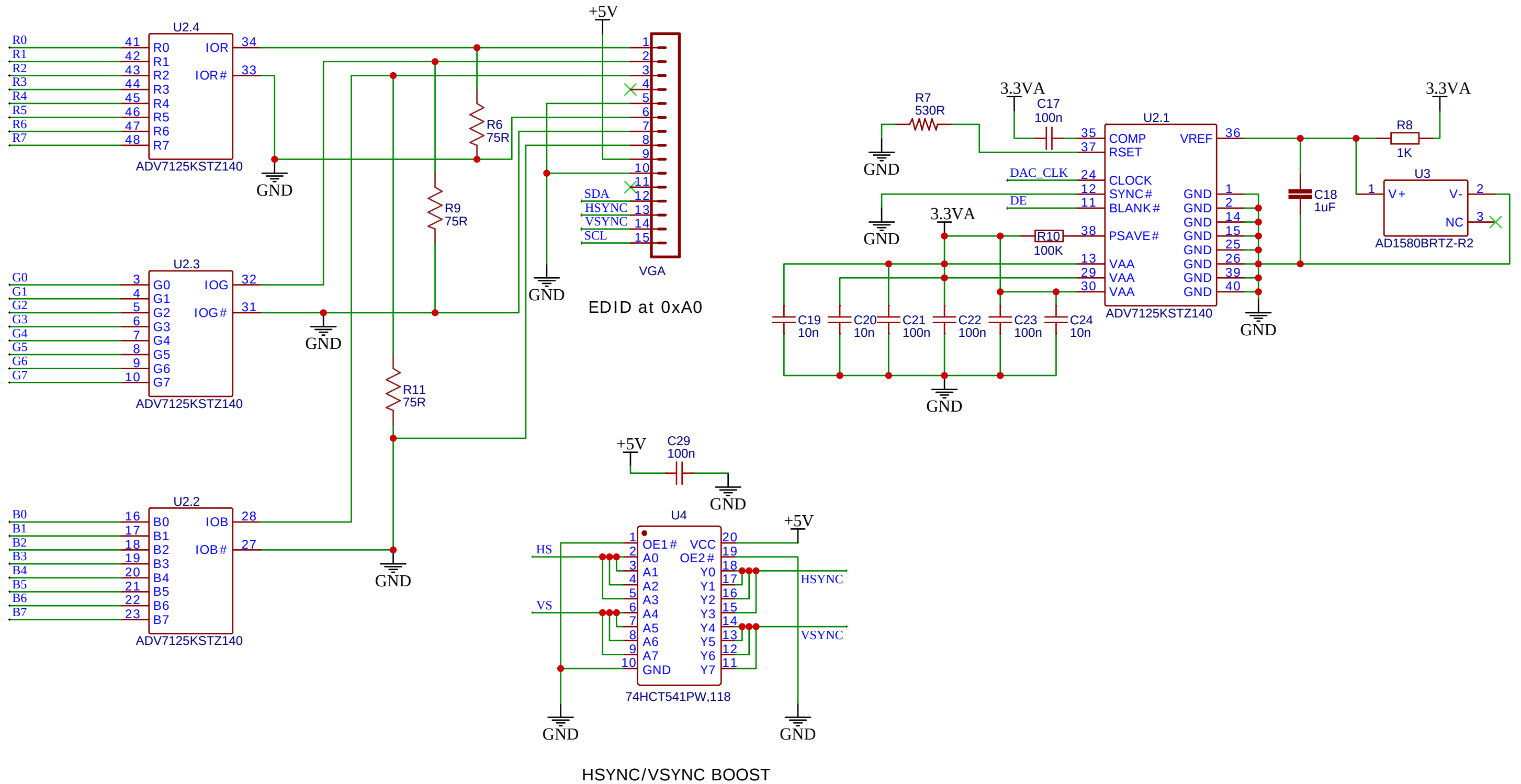


Width	Latch Mode	Edge	Clock Mode
24-bit	Single-edge	Rising	Single-ended



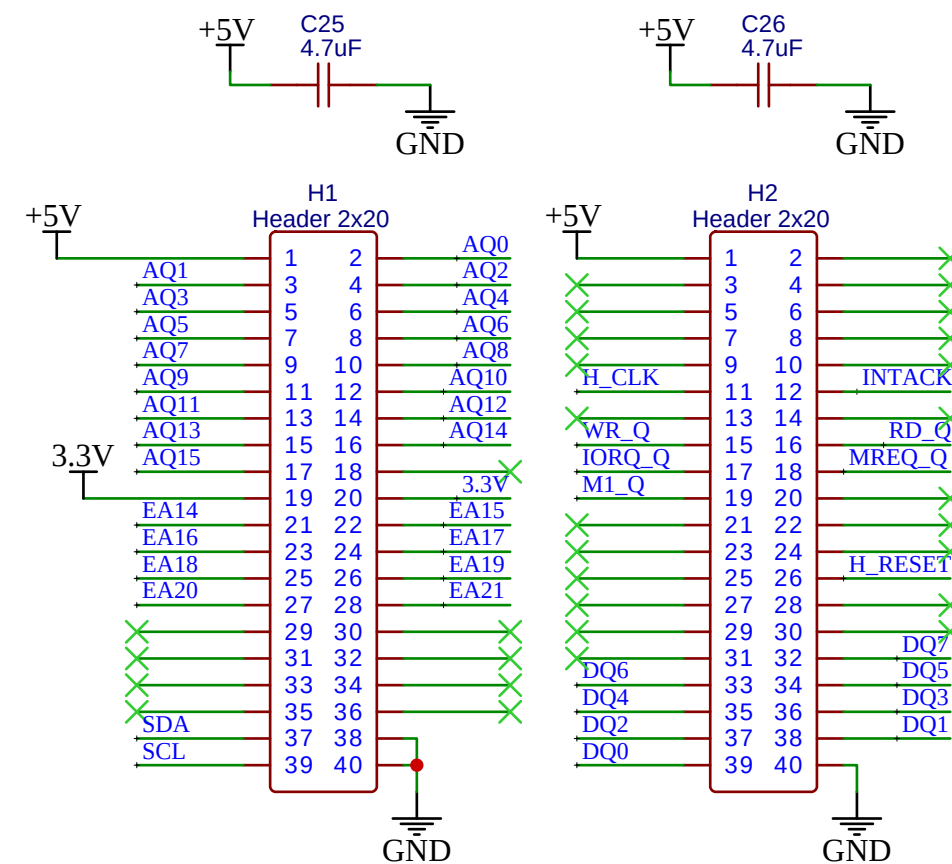
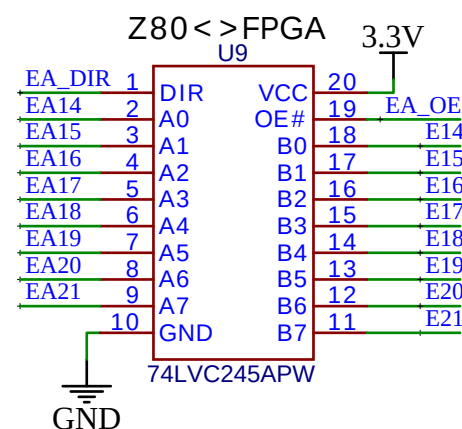
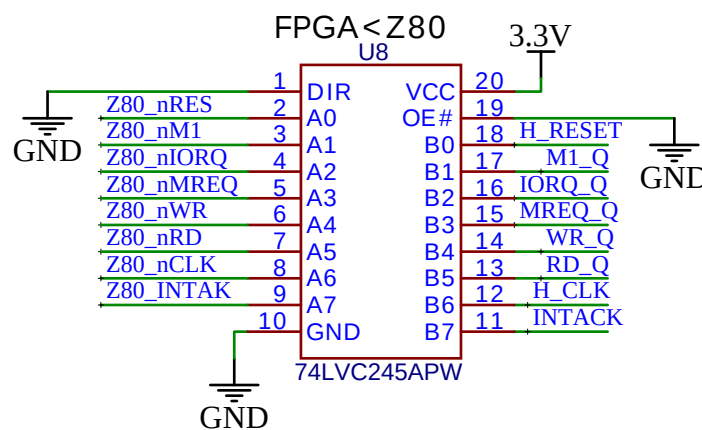
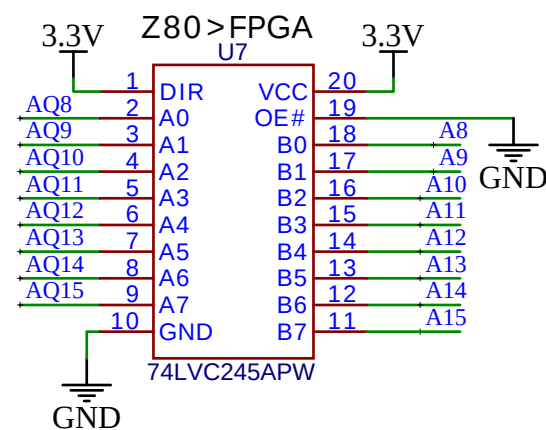
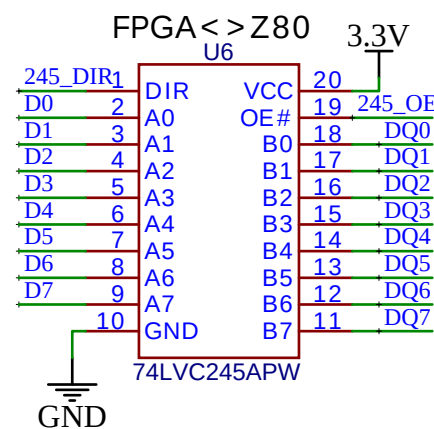
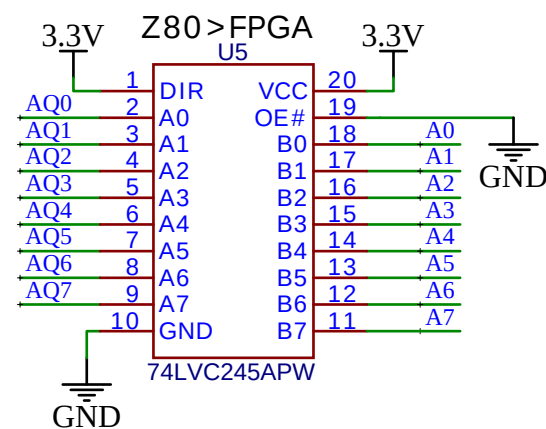
TITLE: Cyclone V GPU		REV: 1.3
	Company: 10103	Sheet: 1/1
	Date: 2020-09-22 Drawn By: nockieboy	

24-bit VGA VIDEO OUTPUT

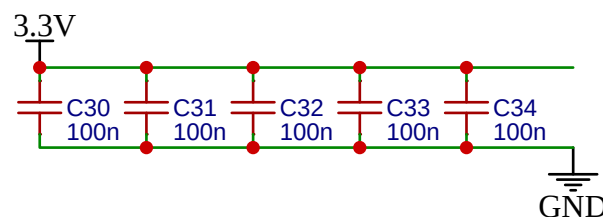


TITLE: Cyclone V GPU		REV: 1.0
EasyEDA	Company: 10103	Sheet: 1/1
	Date: 2020-08-23	Drawn By: nockieboy

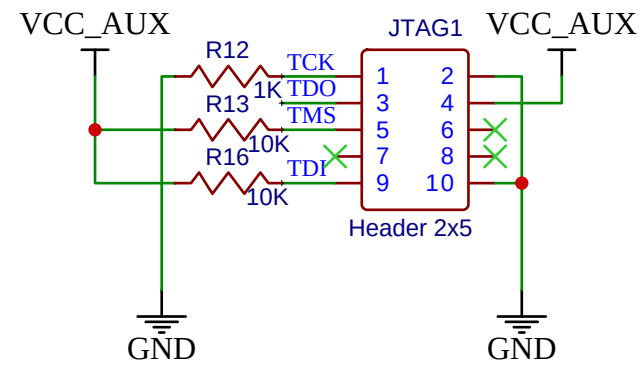
5V <-> 3.3V SYSTEM BUS CONVERTERS



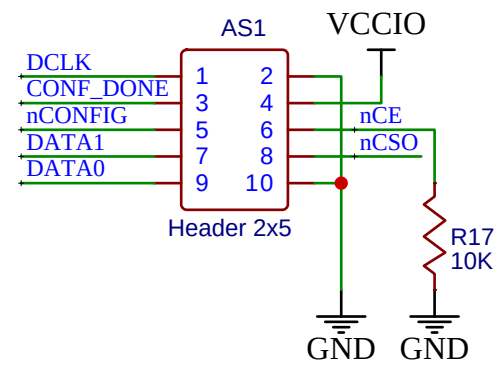
SYSTEM BUS HEADERS



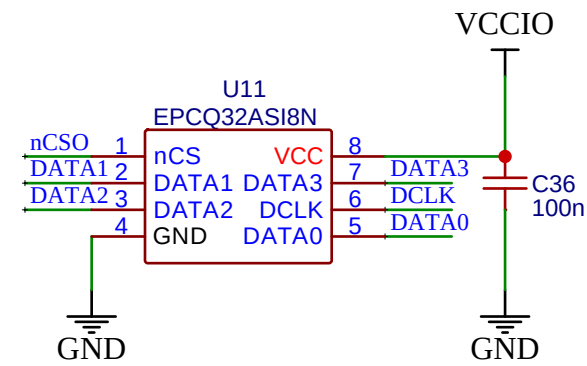
CLOCK & FPGA CONFIGURATION



JTAG HEADER

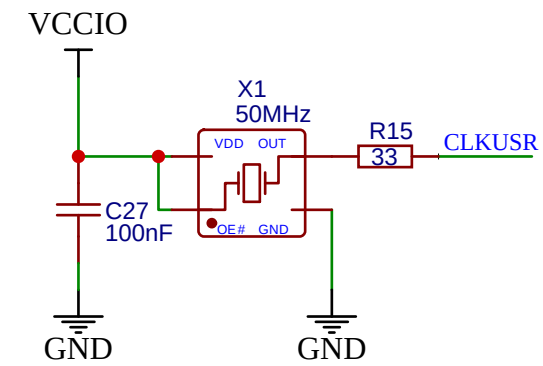


AS HEADER

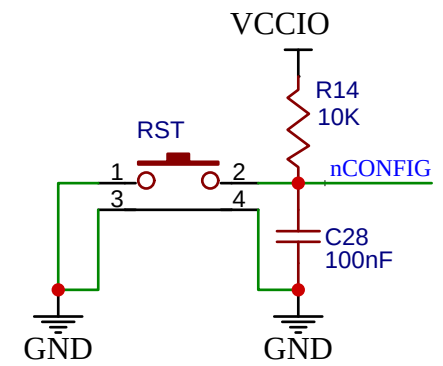


CONFIG EEPROM

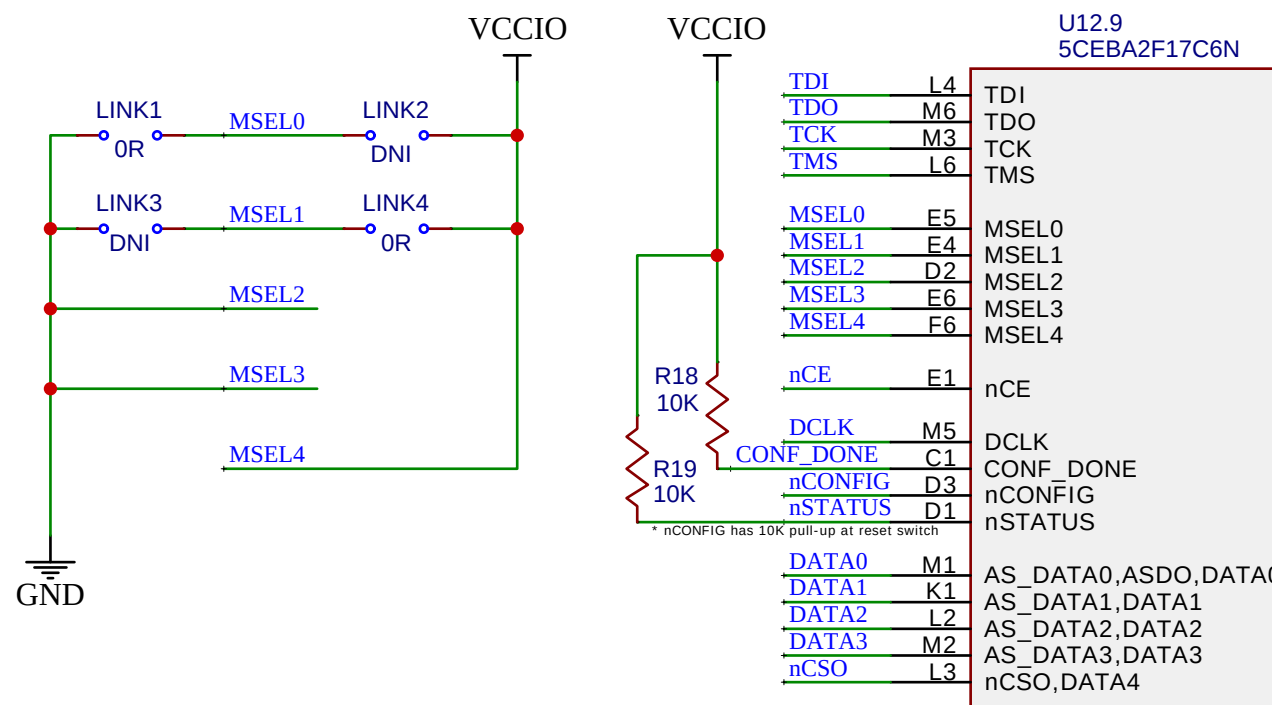
* Minimum 32Mbit EEPROM required for 21Mbit image



50 MHz CLOCK



FPGA RESET

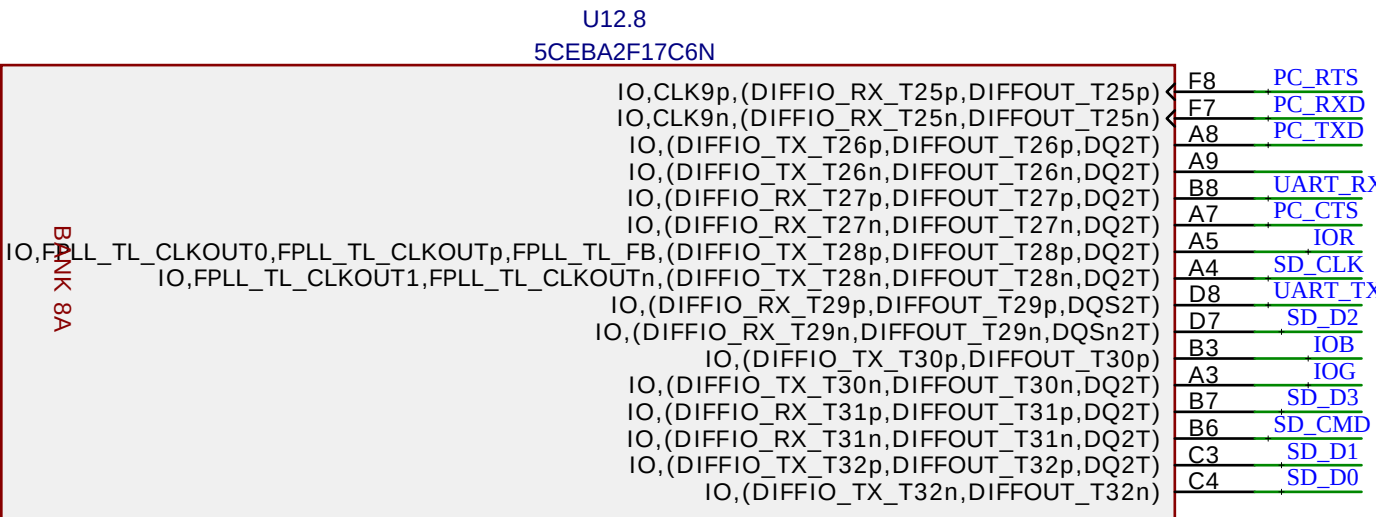
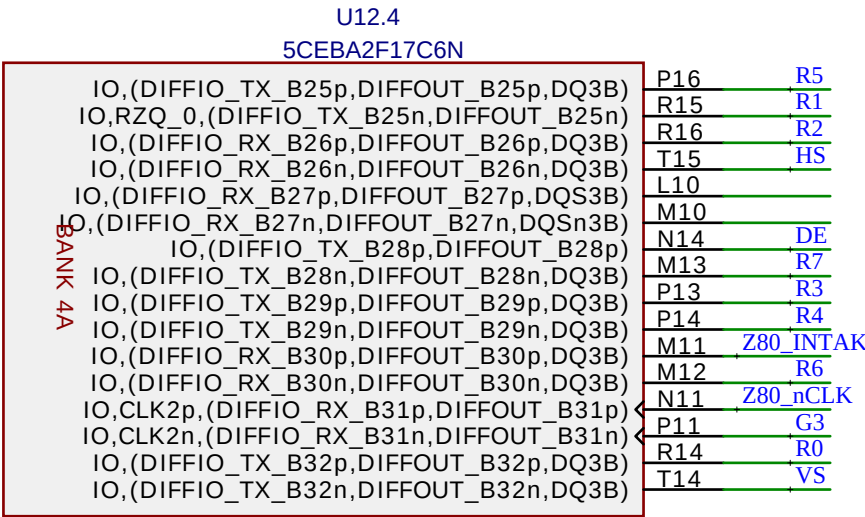
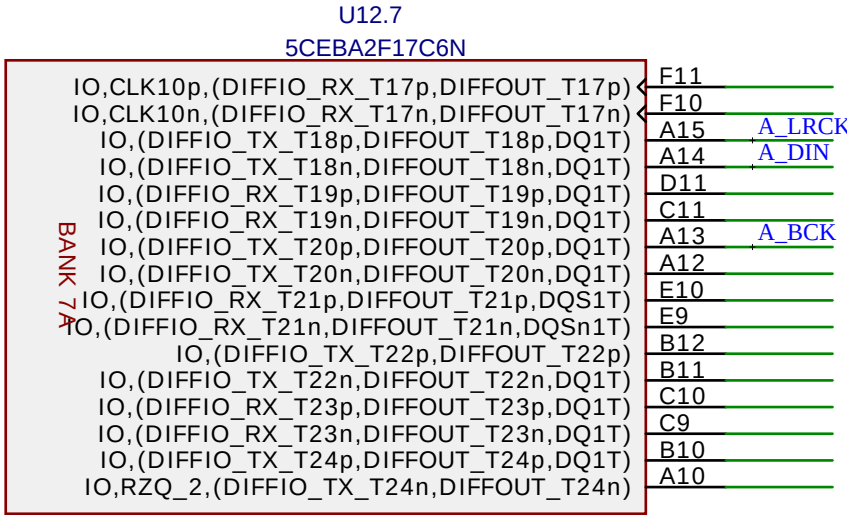
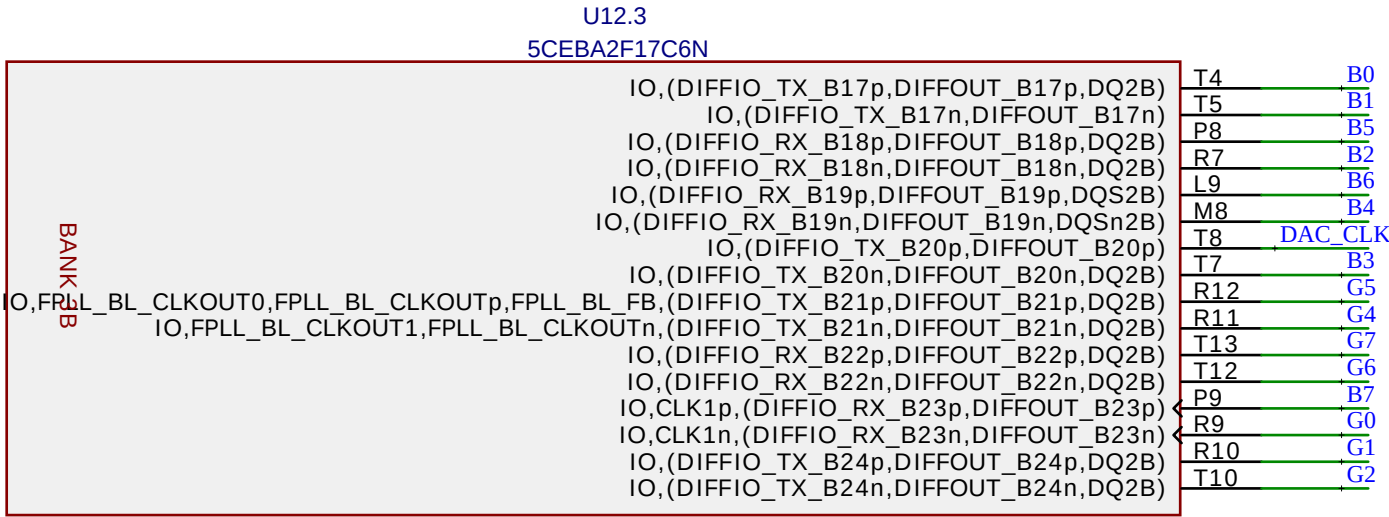
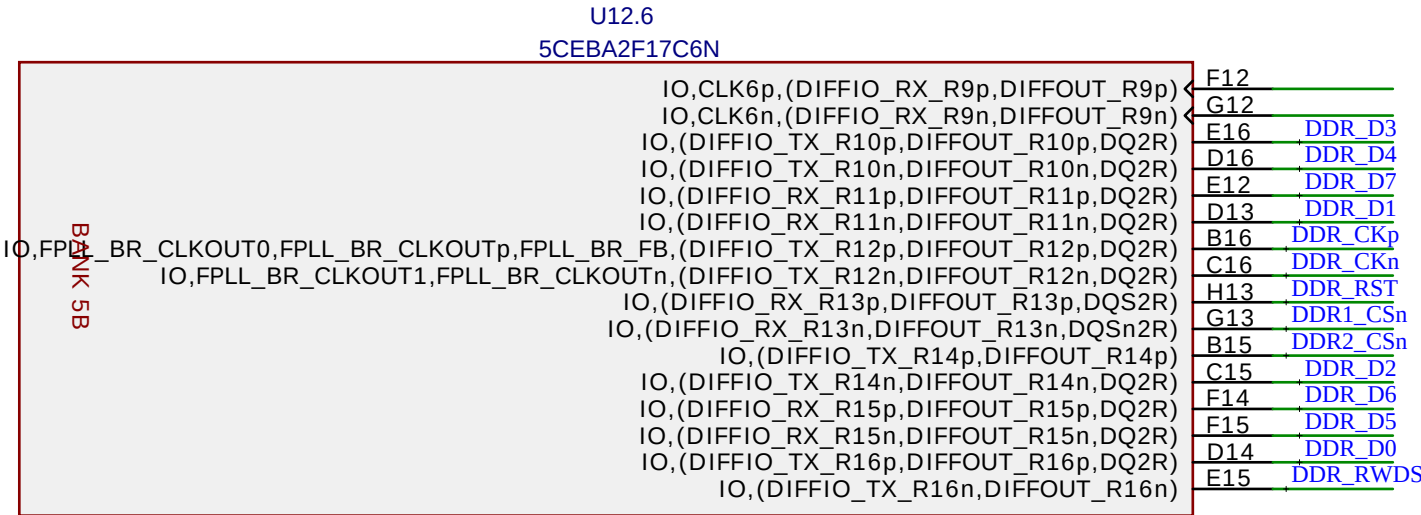
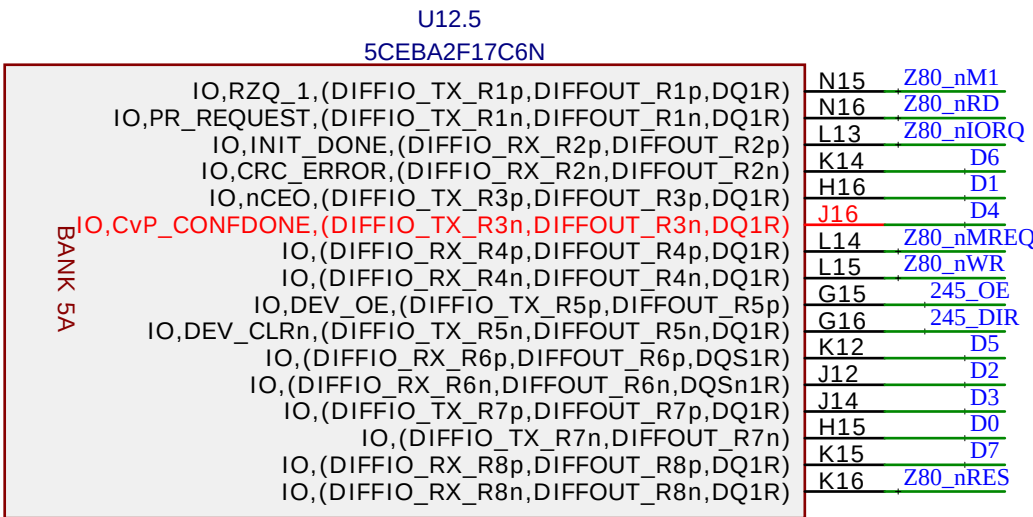
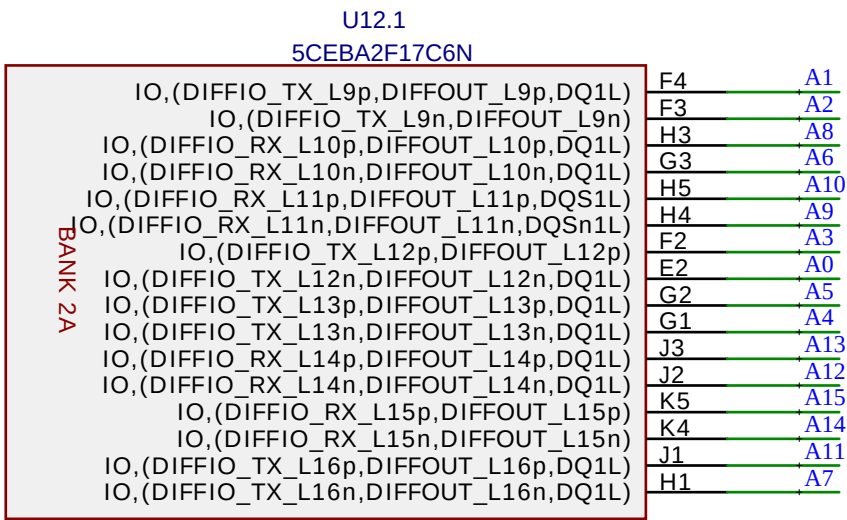
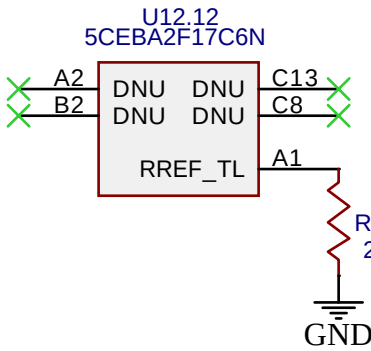


AS FAST (x4) 10010 configuration @ 3.3V with J2 pins 1-2 connected.
AS STANDARD (x1) 10011 configuration @ 3.3V with J2 pins 2-3 connected.

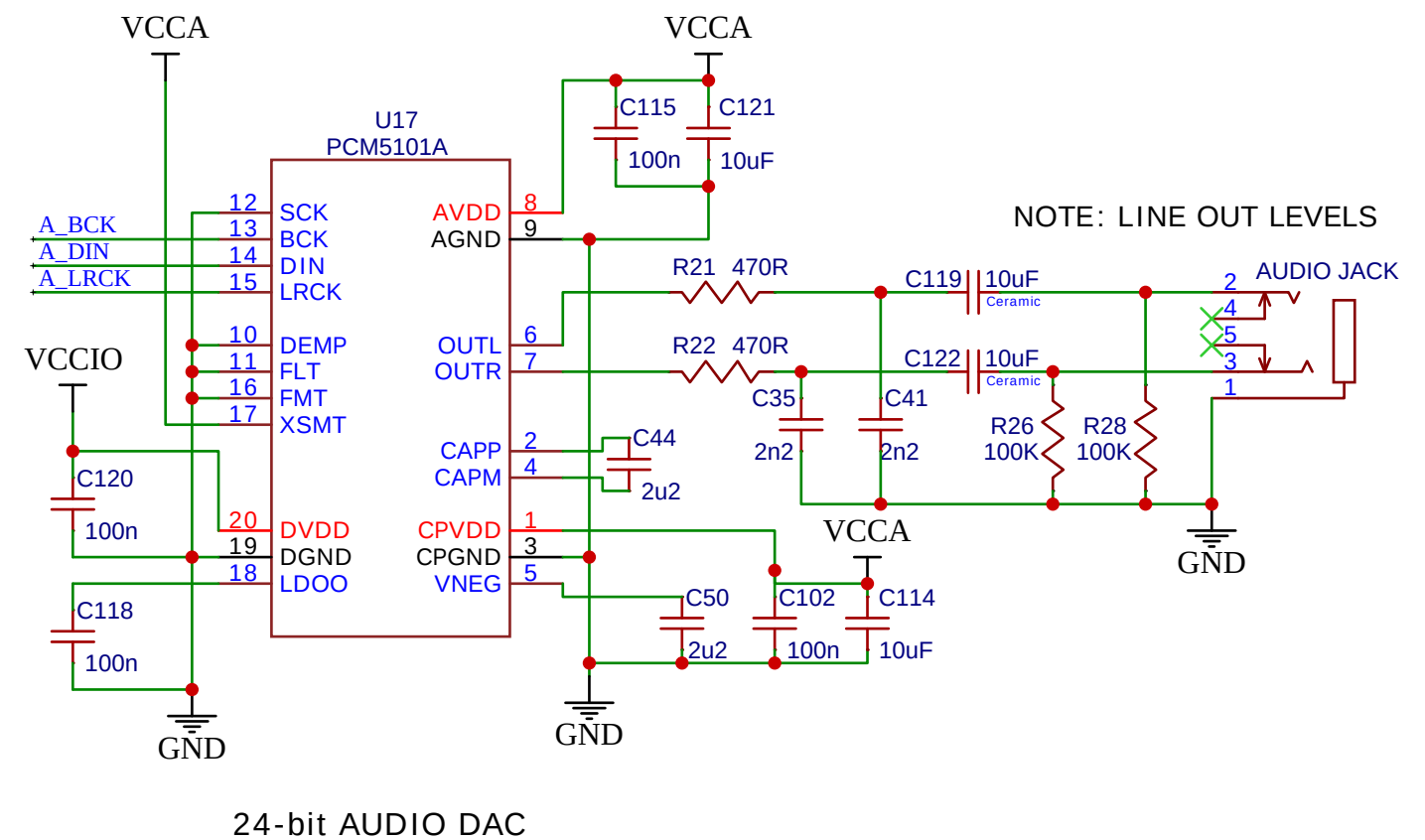
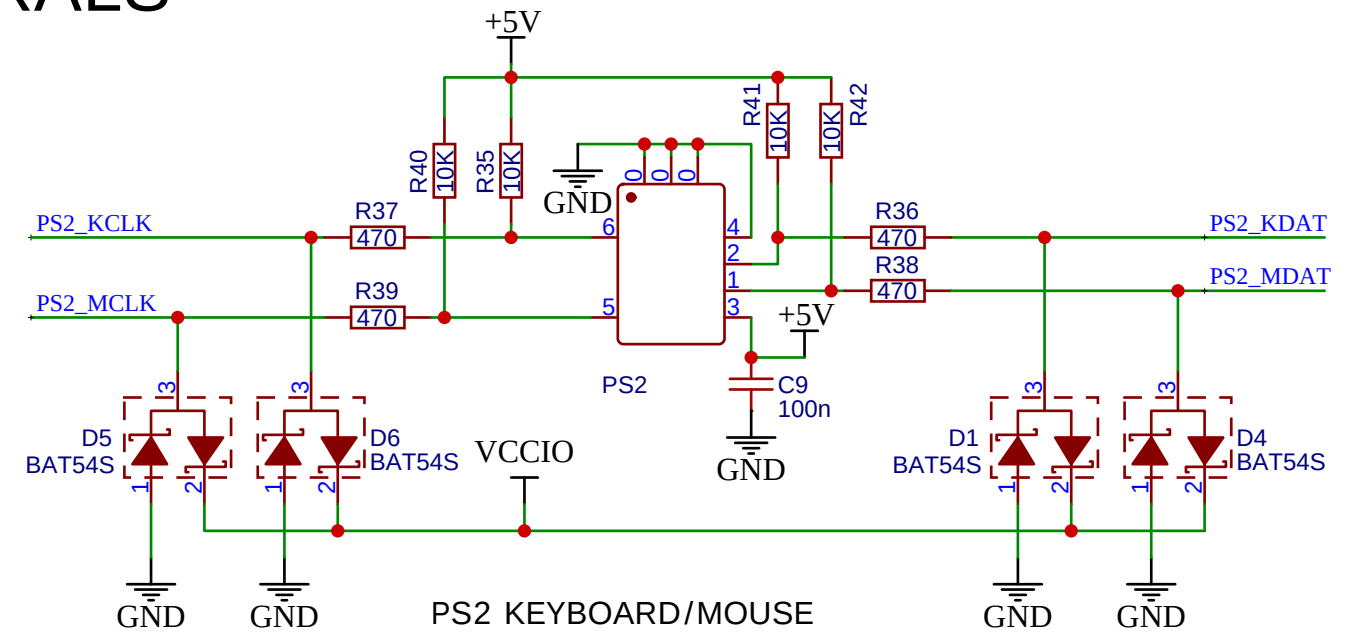
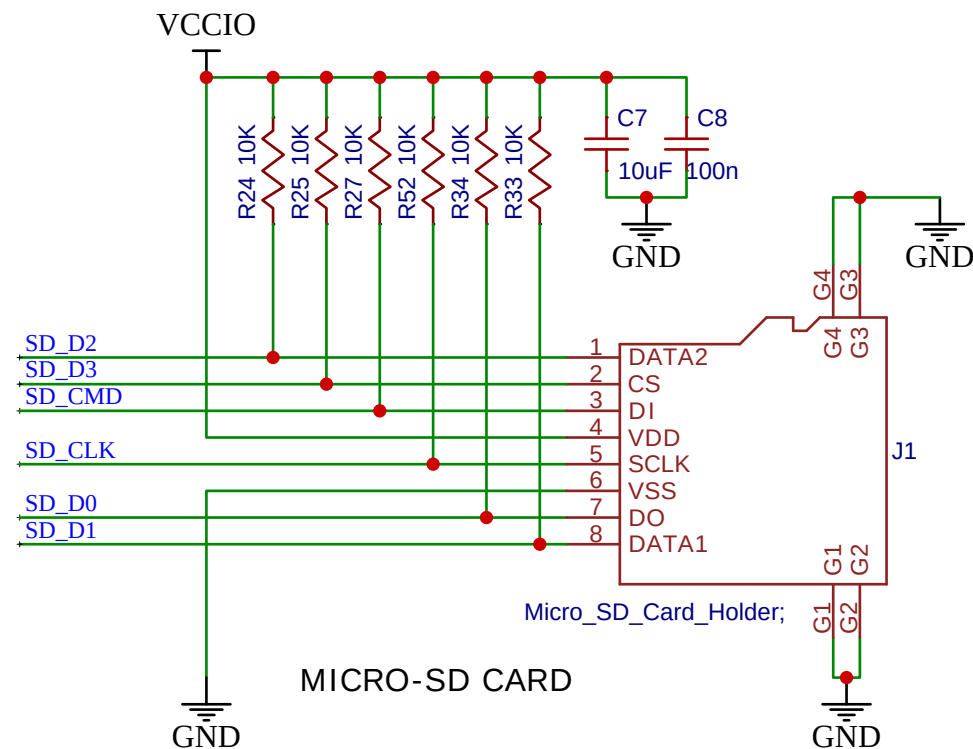
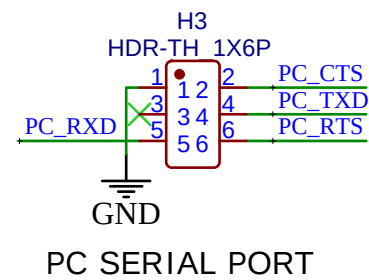
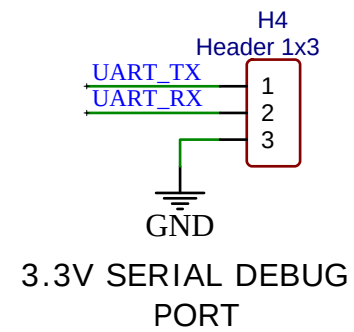
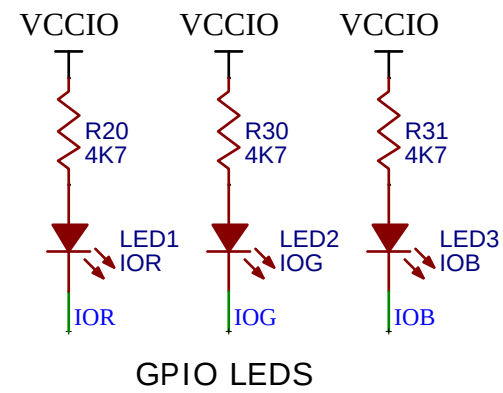
MSEL Pin Settings 7-2 in Cyclone V Device Handbook Volume 1: Device Interfaces and Integration

Cyclone V FPGA

NOTE: Cyclone V A2 and A4 versions are pin-compatible and interchangeable on this PCB design.

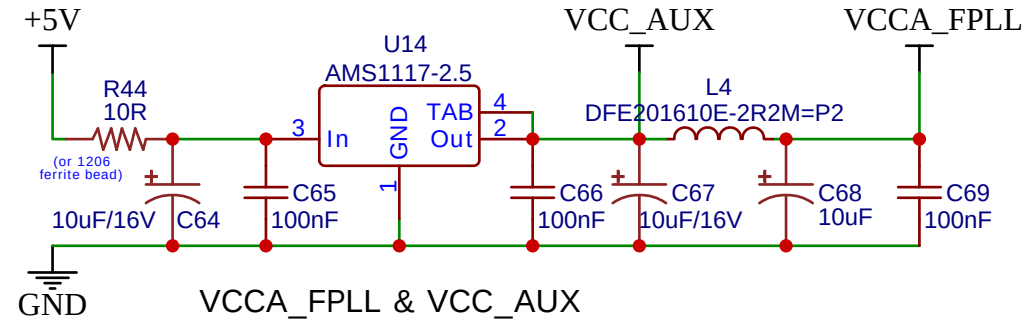
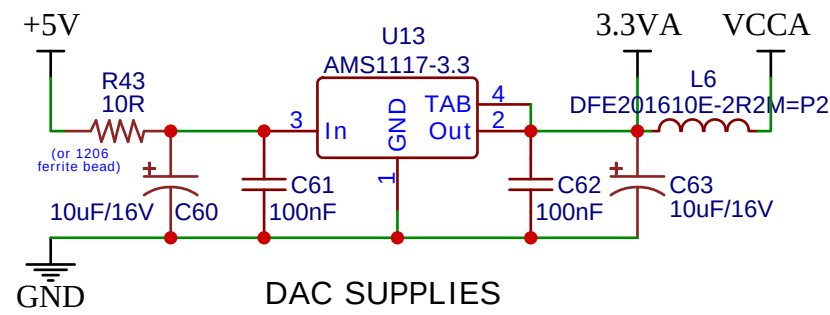


PERIPHERALS

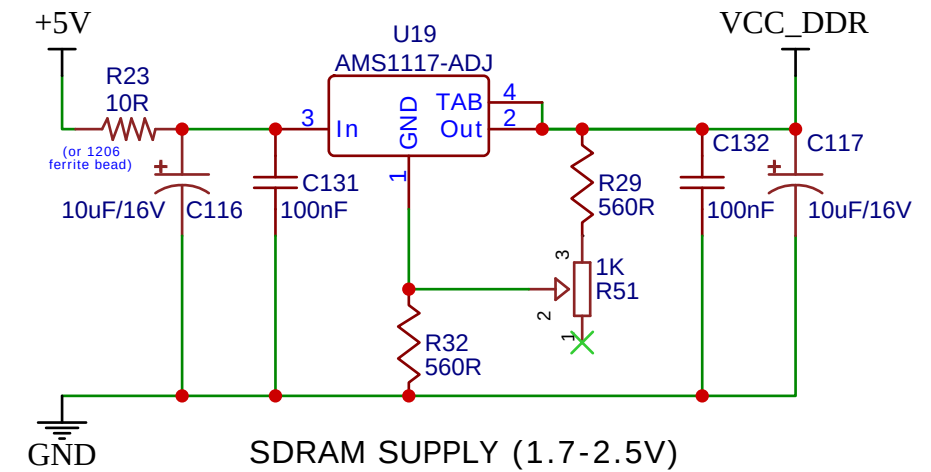
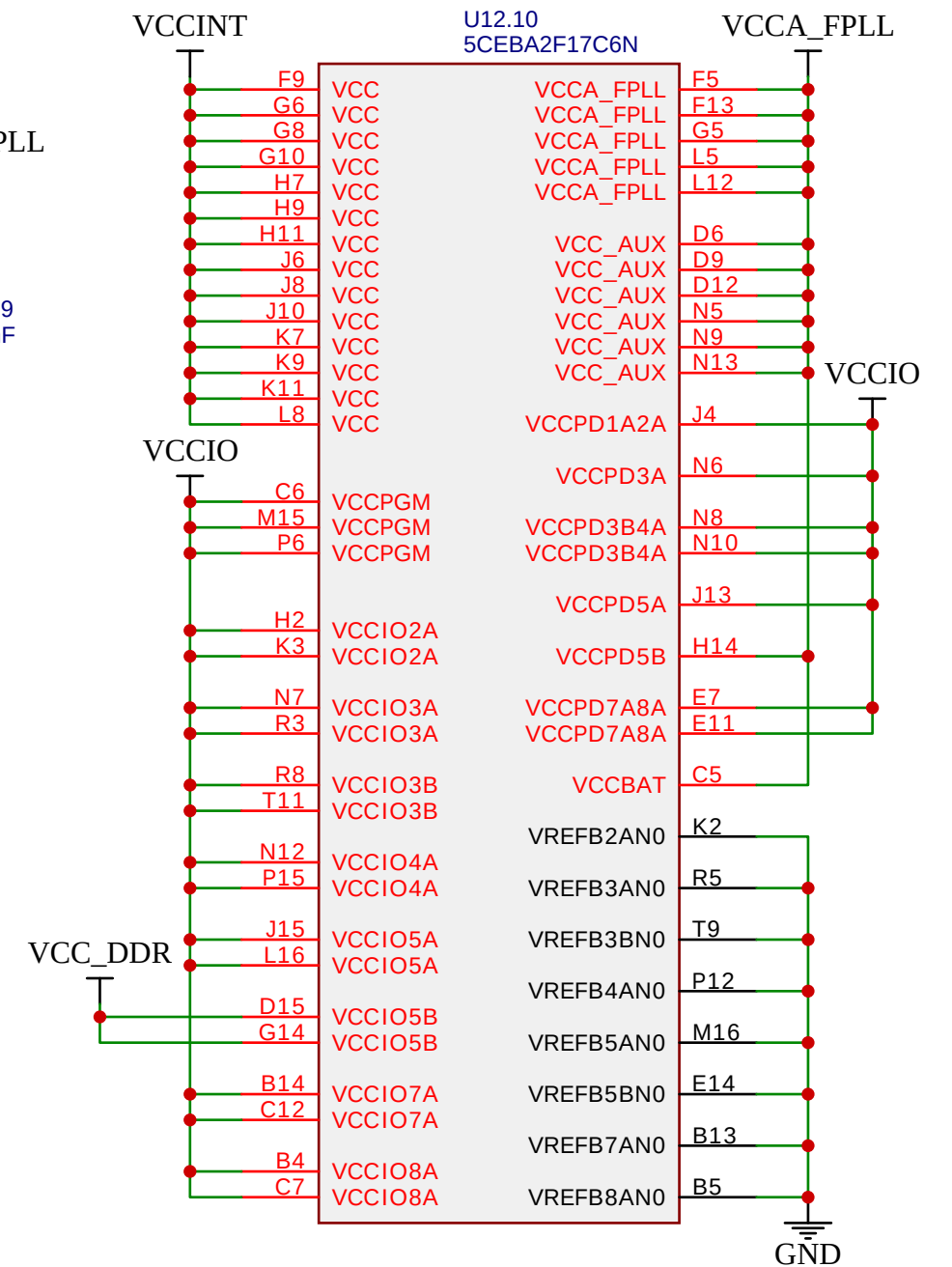
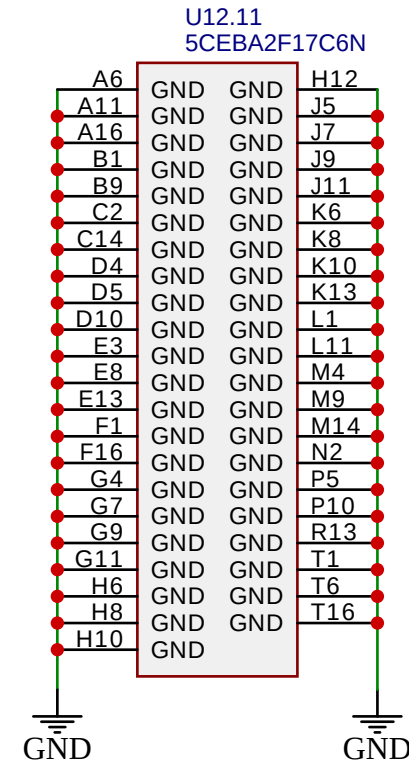
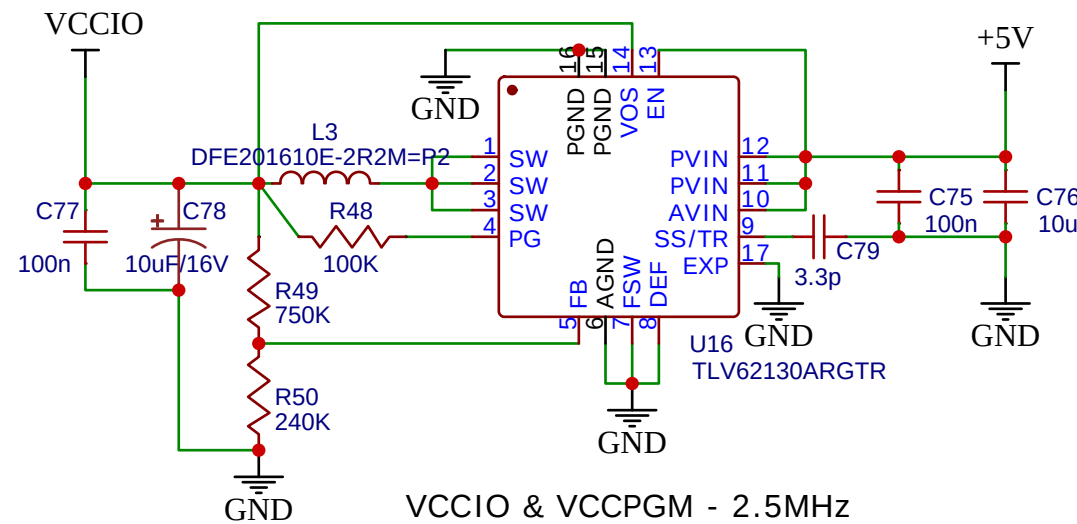
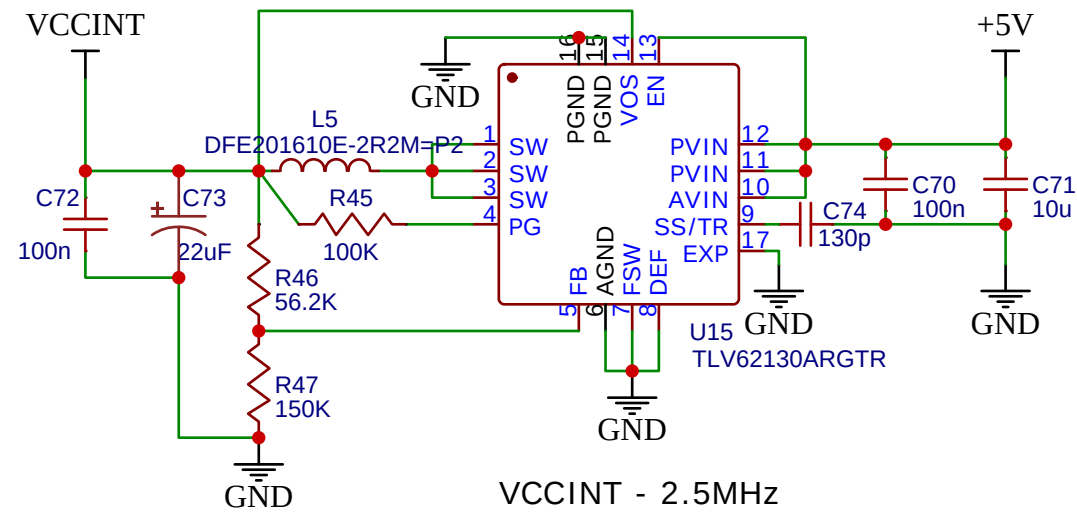


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POWER SUPPLIES



DESIGN NOTE: All 10uF/22uF components are SMD 3216 tantalum caps.

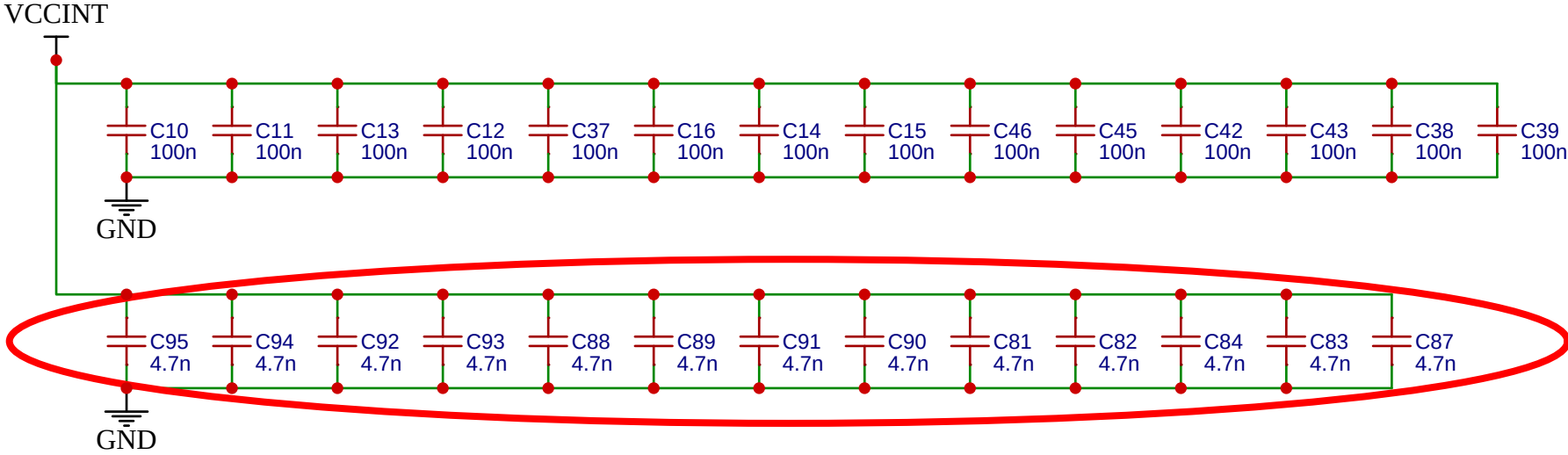


Supplies: U13 - 3.3V supply (3.3VA, VCCA)
 U14 - 2.5V supply (VCCA_FPLL, VCC_AUX)
 U15 - 1.1V supply (VCCINT)
 U16 - 3.3V supply (VCCIO)
 U19 - 1.8-2.5V supply (VCC_DDR)

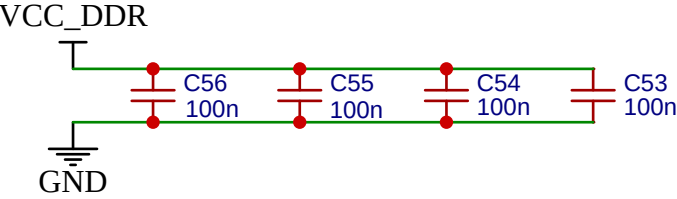
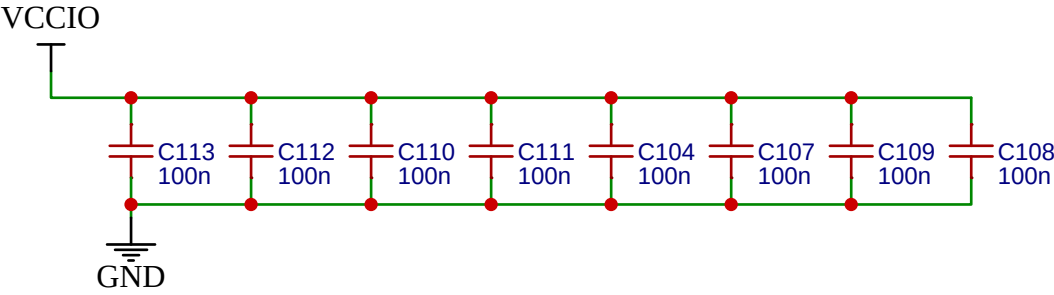
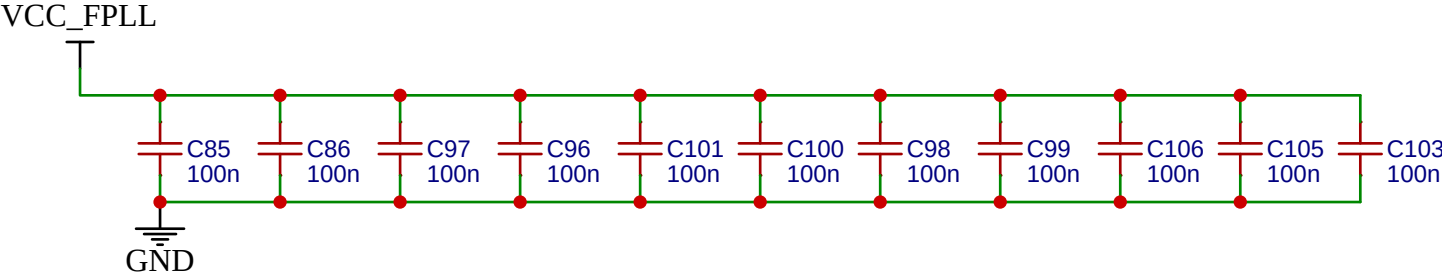
TITLE: Cyclone V GPU		REV: 1.5
EasyEDA	Company: 10103	Sheet: 1/1
	Date: 2020-10-03	Drawn By: nockieboy

FPGA DECOUPLING

Note: Place capacitors near FPGA pins

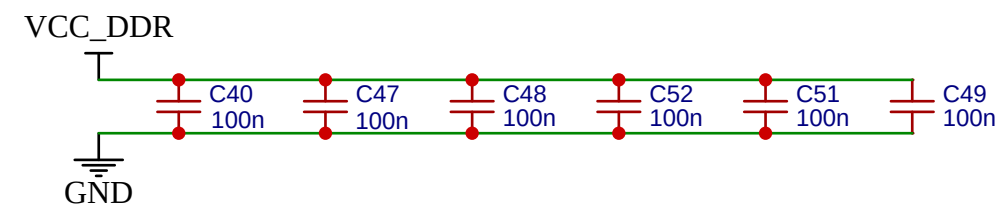
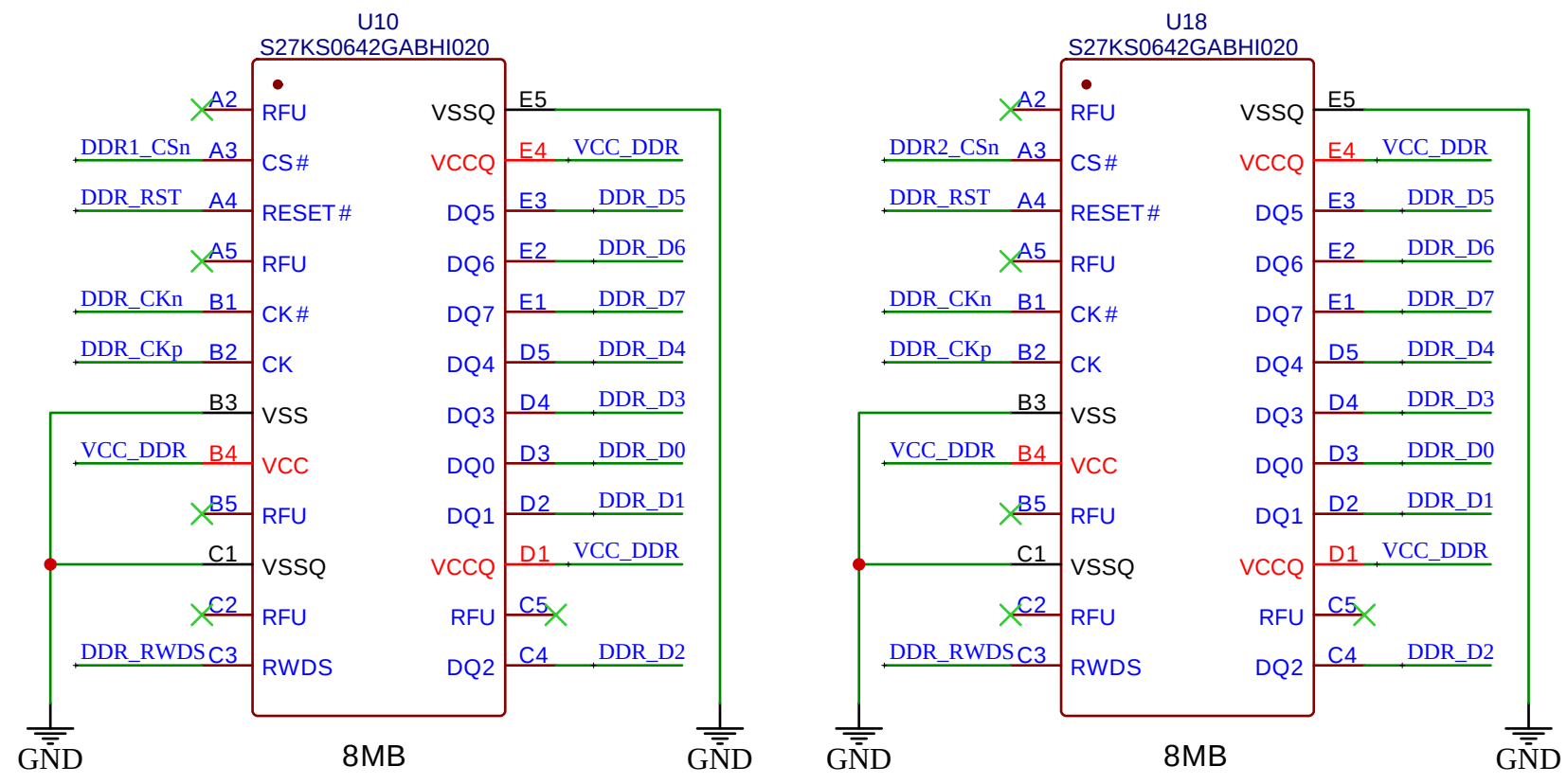


Are these needed?



TITLE: Cyclone V GPU		REV: 1.0
EasyEDA	Company: 10103	Sheet: 1/1
	Date: 2020-10-20 Drawn By: nockieboy	

FPGA EXTERNAL MEMORY



TITLE: Cyclone V GPU		REV: 1.3
	Company: 10103	Sheet: 1/1
	Date: 2020-10-27 Drawn By: nockieboy	