Hard Disk Interface for the Printer Port

IDE2LPT – removable storage via the printer port

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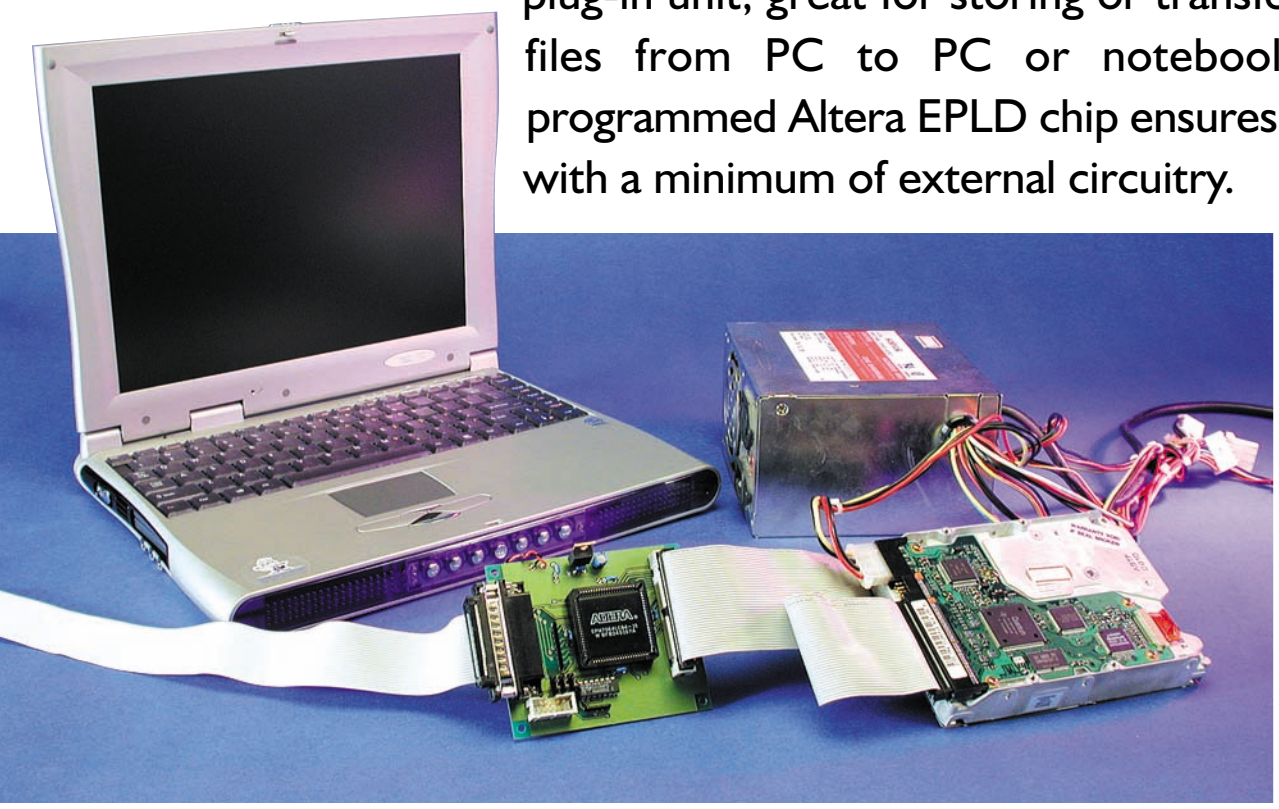
Can't even give away that hard disk drive on your redundant PC system? Why not use it as a portable drive? This interface adapter allows a standard low-cost internal hard drive to be used as a convenient mobile plug-in unit, great for storing or transferring large files from PC to PC or notebook. A pre-programmed Altera EPLD chip ensures a neat unit with a minimum of external circuitry.



It's difficult to believe that the first PC systems came without a hard disk drive. How did we ever manage? It was only when hard drives appeared that the real convenience of a PC was realised, we didn't mind that these drives could only store a few Mbytes and were about the same size and weight as a common house brick, it was certainly an improvement on reloading MS-DOS from a boot disk at every start-up.

Modern Hard Disk Drives (HDDs) are by comparison vastly improved, slim jewels of precision engineering. Floppy disks used to be sufficient to store and transfer complete programs but nowadays with ever-increasing program size a removable HDD seems a better alternative. Standard non-removable internal HDDs offer the highest storage capacity at the lowest cost but plug directly into the Integrated Disk Electronic (IDE) interface on the motherboard. The PC has no external

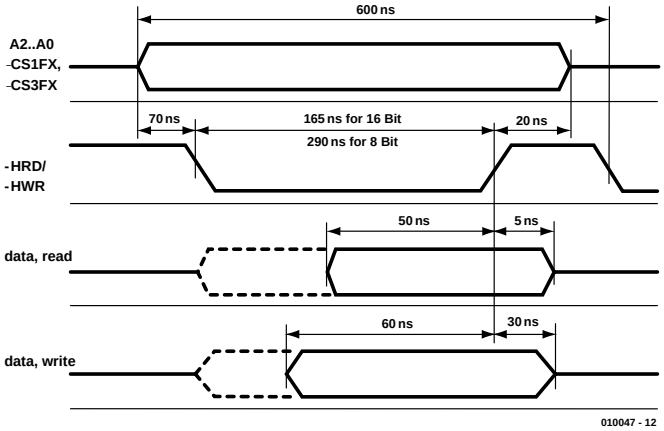


Figure 1. IDE bus read and write timing diagram.

Adapter Specification:

Maximum size of hard disk drive: Unlimited.
Maximum number of hard disk drives: 1
Data transfer rate: up to 100 kByte/s
Power requirements: 5 V / < 10 mA
(from an external 12 V supply)

IDE connector as standard. If we are to use such an HDD as a portable unit plugging into any PC, it will be necessary to adapt an existing external PC port.

PC's have always had a parallel printer port so it seemed like a good idea to develop an interface adapter (implemented as an Altera CPLD) along with some software that would allow data to be transferred to and from a hard disk via a printer port.

LPT to IDE

In the March 2001 edition of Elektor Electronics the article 'IDE hard disk interface for 8-bit controllers' described an adapter that enabled 8-bit controllers to use a hard disk with an IDE interface. That article described in detail the IDE interface (also known as the ATA interface) and its history so we will not repeat all the information here but just look at some of the important signals that are used in this design (a complete specification is available at www.t13.org). An overview of the signals on this 40-pin connector is given in Table 1.

The LPT2IDE interface makes use of the following signals:

HD15 to HD0 Data lines (8 or 16 bit wide bus, bi-directional).

CS1FX/Chip Select 0 this selects the command register blocks.

CS3FX/Chip Select 1 this selects the status register blocks.

HRD / I/O-read Read signal for I/O port address. Data is put onto the bus (HD0 to HD7 or HD0 to HD15) by the hard disk when this signal is low and latched into the

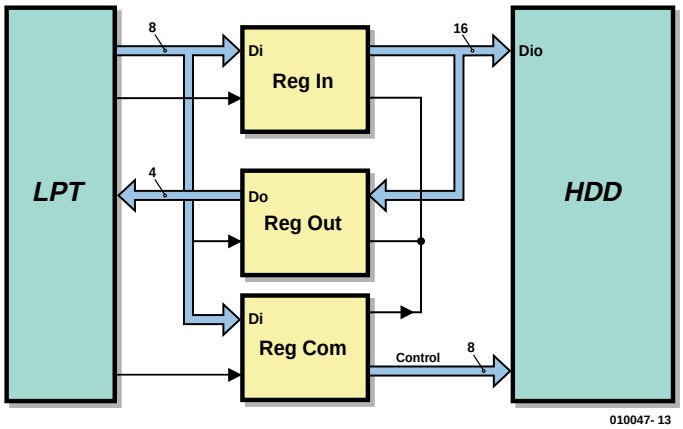


Figure 2. Block diagram of the LPT/IDE adapter.

Table 1. ATA Interface Pinning

Pin no.	Label	Description
1	-HRESET	RESET
2	GND	GND
3	HD7	Data bus bit 7
4	HD8	Data bus bit 8
5	HD6	Data bus bit 6
6	HD9	Data bus bit 9
7	HD5	Data bus bit 5
8	HD10	Data bus bit 10
9	HD4	Data bus bit 4
10	HD11	Data bus bit 11
11	HD3	Data bus bit 3
12	HD12	Data bus bit 12
13	HD2	Data bus bit 2
14	HD13	Data bus bit 13
15	HD1	Data bus bit 1
16	HD14	Data bus bit 14
17	HD0	Data bus bit 0
18	HD15	Data bus bit 15
19	GND	GND
20	N/C	key pin
21	DMARQ	DMA request
22	GND	GND
23	-HWR	I/O WRITE
24	GND	GND
25	-HRD	I/O READ
26	GND	GND
27	IORDY	I/O CHANNEL READY
28	SPSYNC:CSEL	SPINDLE SYNC or CABLE SELECT
29	-DMACK	DMA ACKNOWLEDGE
30	GND	GND
31	INTRQ	Interrupt request
32	-IOCS16	16 BIT I/O
33	HA1	ADDRESS BUS BIT 1
34	-PDIAG	PASSED DIAGNOSTICS
35	HA0	ADDRESS BUS BIT 0
36	HA2	ADDRESS BUS BIT 2
37	-CS1FX	CHIP SELECT 0
38	-CS3FX	CHIP SELECT 1
39	-DASP	DRIVE ACTIVE/DRIVE 1 PRESENT
40	GND	GND

host system on the rising edge.

HWR / I/O-write write signal for the I/O port address. The falling edge of this signal will latch the bus data (HD0 to HD7 or HD0 to HD15) into the hard disk register.

HA0, HA1, HA2 / Address bus Bit 0 to Bit 2. Registers or ports in the hard disk are selected with these address lines.

HRESET /Reset A low-level here will initialise the hard disk.

The diagram in **Figure 1** shows the timing for read and write cycles on the IDE bus. On the other side of the interface we have the parallel printer port using a standard 25-pin sub-D connector. The printer port has an 8-bit wide data bus together with six printer control signals (from PC to printer) and five printer status signals (from printer to the PC). Data to the LPT1 is sent by writing to address 378h (write only), the control register is (again write only) at address 37Ah and the status register is at address 379h (read only). A fuller description of the printer port addressing for both LPT1 and LPT2 is given in **Table 2**.

The printer port data transfer rate is less than 150 kBytes/s, but has the advantage that all the signal lines can be software controlled, this simplifies the design of both the control software and hardware.

Table 2. Signals and registers: LPT interface and LPT/IDE converter

Addresses LPTI/LPT2	Description					
378h/278h	Data Registers DATA7..DATA0 (write-only)					
379h/279h	Status-Register (read-only)					
	Bit	LPT Name	IDE2LPT Name	Status	Read Status	Function
	7	BUSY	LI3	I	0	DATA3 from converter
	6	SLCT	LI2	I	I	DATA2 from converter
	5	PE	LII	I	I	DATA1 from converter
	4	ACK	LI0	I	I	DATA0 from converter
	3	ERROR	—	I	I	—
	2	—	—	—	0	—
	I	—	—	—	0	—
	0	—	—	—	0	—
37ah/27ah	Control Register					
	Bit	LPT Name	IDE2LPT Name	Status	Read Status	Function
	7	—	—	—	0	
	6	—	—	—	0	
	5	—	—	—	0	
	4	—	—	—	0	
	3	SLCT_IN	RCWR	0	I	Write signal for Reg_COM
	2	INIT	RLWR	0	0	Write signal for Reg_IN from DATA7 - DATA0 to HD7 - HD0
	I	AUTO_FD	RHWR	0	I	Write signal for Reg_IN from DATA7 - DATA0 to HD15 - HD8
	0	STROBE	HRESET	0	I	Reset HDD

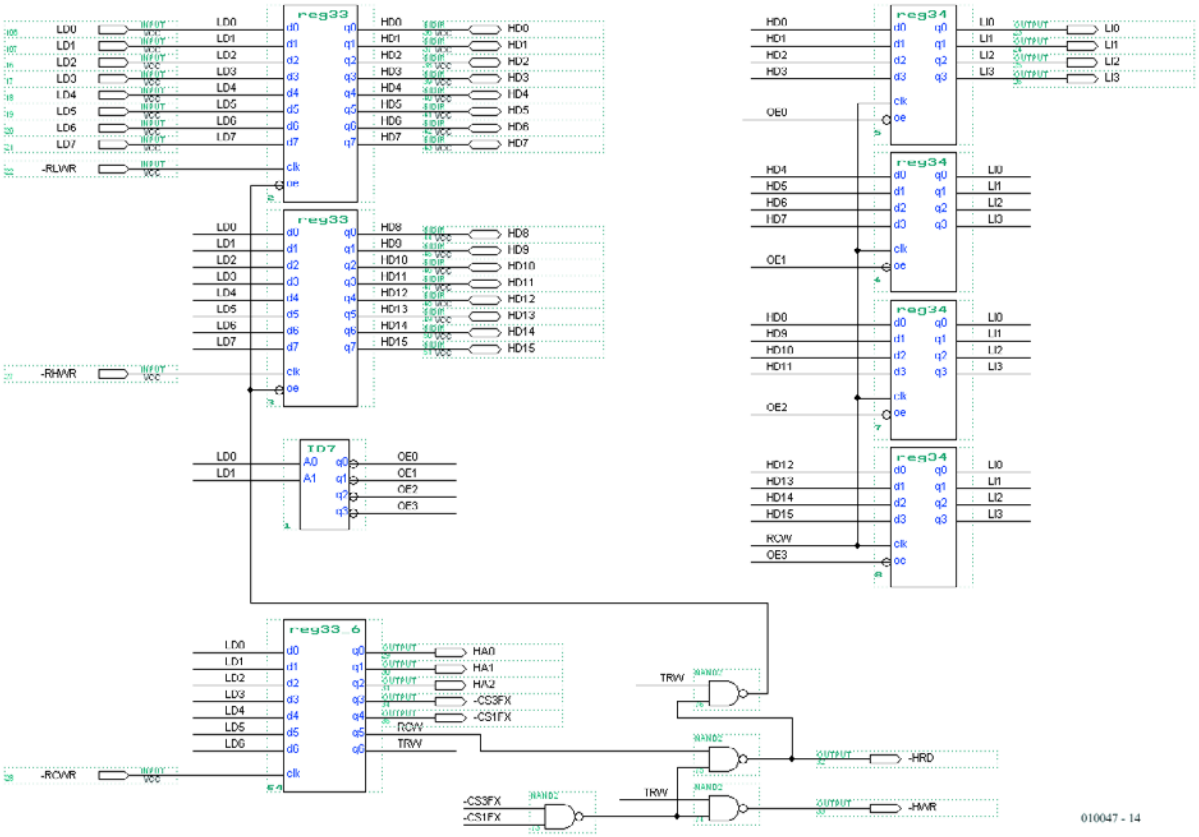


Figure 3. The chip circuit defined in AHDL and programmed into a CPLD.

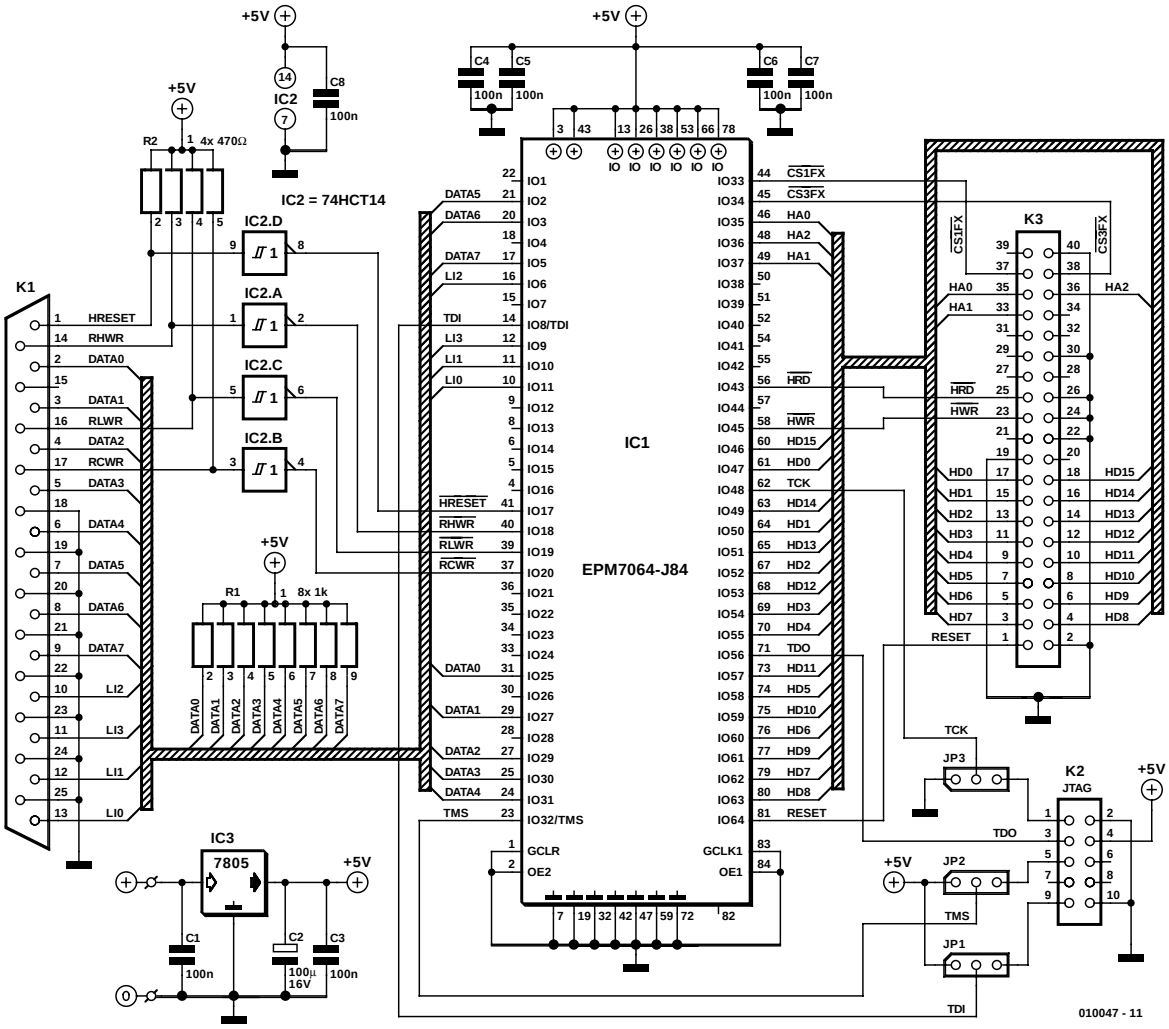


Figure 4.Circuit diagram of the LPT/IDE adapter. The JTAG connector allows in-circuit programming of the CPLD.

Table 3. Control Register signals in LPT/IDE converter

Bit	Name	Function	
7	—	—	
6	TRW	Write signal -HWR on IDE Bus.	Active level: 1.
5	RCW	Read signal -HRD on IDE Bus.	Active level: 1.
4	-CS1FX	CHIP SELECT 0.	Active level: 0.
3	-CS3FX	CHIP SELECT 1.	Active level: 0.
2..0	HA2 - HA0	ADDRESS BUS	

The adapter circuit

In the world of hard disk interfaces the data transfer rate of the printer port is not especially fast. It is therefore pointless to use all the features and speed enhancing techniques that are available on the IDE interface such as Direct Memory Access (DMA), 16 bit data transfer, standby and diagnostics. The IDE to LPT interface adapter is basically just a buffer between the two interfaces. **Figure 2** shows a block diagram of the circuit. Writing to the HDD is performed in two, eight bit wide bytes that are stored in the input register (Reg In) and sent to the HDD as 16 bit words. In the read direction the 16 bit wide data is stored in the output register (Reg Out) and read out in 4 bit wide nibbles to the LPT status register where it is read by the computer. Controlling the data transfer is performed by instructions sent to the command register (Reg Com) and are listed in **Table 3**. Additional control logic is used to prevent prohibited conditions on the IDE bus. (see **Table 4**).

The majority of the LPT/IDE adapter circuitry has been implemented in a CPLD. This entails defining the entire circuit of registers and logic in the Hardware Description Language AHDL. A pre-programmed Altera logic chip of the EPM 7064 family from Altera is available from the Elektor Electronics Readers Services and the source file for the chip is also available as a Free Download from the Elektor Electronics website. Figure 3 is the chip internal circuit diagram produced by this program. Figure 4 shows the circuit diagram of the adapter card where IC1 is the CPLD chip. In addition to this chip is IC2 which is a 74HCT14 inverting buffer with input hysteresis giving improved immunity to noise on the RHWR, RLWR, RCWR und HRESET inputs.

IC3 produces 5 V necessary for the adapter card from an external 12 V power source. (see 'plugging it all together'). Connecter K2 (JTAG) is used by IC1 and allows the chip to be re-programmed and de-bugged. The chip software 'MAX2plus' is available free of charge from the Altera website *(www.altera.com)* and the chip programming software (called 'BitBlaster') is also available from Altera but this time for a small fee. It is not necessary to purchase BitBlaster or use the socket K2 because IC1 is available pre-programmed from the Elektor Electronics (see Readers Services). The JTAG socket is used by any of the Altera CPLD 7000 family with the S suffix (here the EPM7064S). The three programming input signals to IC1 (TCK, TMS and TDI) should be jumpered to earth at JP1, JP2 and JP3 in normal circuit operation but for de-bugging and re-reprogramming the jumpers must be moved to connect these signals through to K2.

The double-sided PCB shown in Figure 5 can be ordered from Elektor Electronics. If you have the means to produce your own PCB then the necessary files are freely available from the Elektor Electronics website at *www.elektor-electronics.co.uk.*

COMPONENTS LIST

Resistors:
R1 = SIL array 8 x 1kΩ
R2 = SIL array 4 x 470Ω

Capacitors:
C1,C3-C8 = 100nF
C2 = 100µF 16V radial

Semiconductors:
IC1 = 7064LC84-15 (Altera), programmed, order code **010047-31**
IC2 = 74HCT14N
IC3 = 7805

Miscellaneous:
JP1,JP2,JP3 = 3-way pinheader with jumper
K1 = 25-way sub-D-plug (male), PCB mount
K2 = 10-way boxheader
K3 = 40-way boxheader
2 solder pins
Extension cable for PC PSU (see text)
Printer extension cable (1:1)
IDE cable
PCB, order code **010047-1**

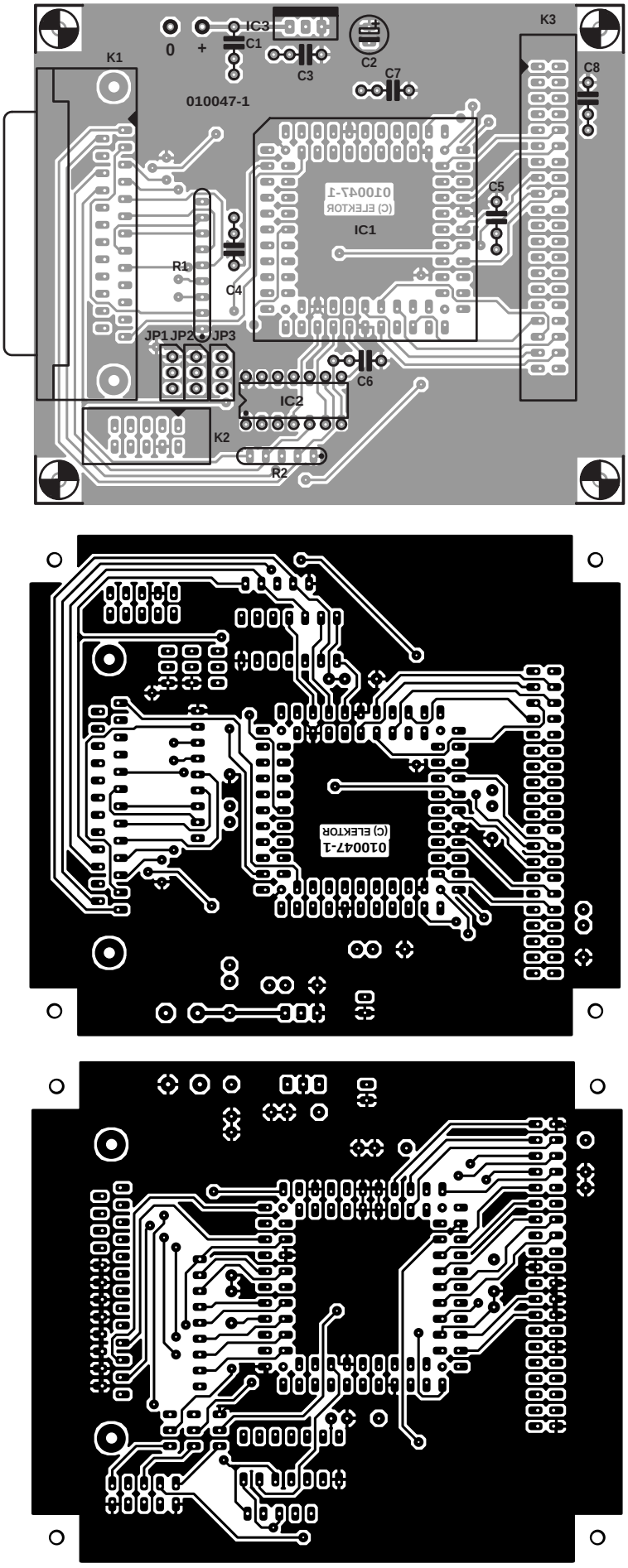


Figure 5. Layout of the double-sided PCB.

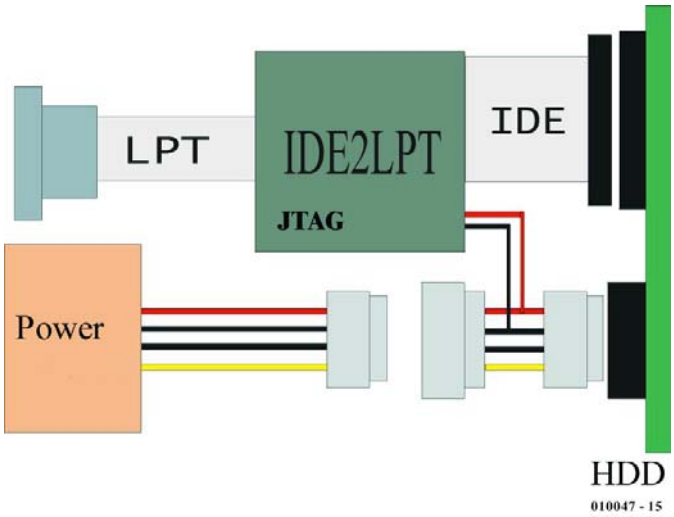


Figure 6. Wiring of the unit together with a PC power supply.

Software

As with any PC port a driver program is necessary to pass information in and out of the LPT/IDE adapter. Two versions of the 'LPT2IDE' driver program are available, one runs in DOS while the other runs in Windows. Firstly the program 'ide2lpt.exe' runs under MS-DOS from version 3.3 upwards. It is not unlike standard IDE driver routines, in fact we have adapted an existing IDE driver to read and write via the printer port. Additional test and search features have also been included and thanks go to Ewgenij Kuleschow for the driver source code. To install the driver a line must be added to the config.sys file:

```
device=[path]\ide2lpt.exe [options]
```

normally:

```
device=c:\lpt2ide\i2l4.exe
```

For different settings or tests the options can be added to the program name at the DOS command prompt e.g. the option /T (I2L4.EXE/T) for test.
Other options available are:

/H Help
/L:LPT The LPT port Address (378h for LPT1 and 278h for LPT2)
/G:SEC:HEAD Defines the HDD parameters (used for fixed drives operating in LBA mode): SEC indicates the number of sectors and HEAD the number of heads. The format is in decimal.
/LLBA mode
/V Request hard disk parameters.

The DOS driver uses FAT12, FAT16, BIG and Extended Partition while FAT32 is supported by the second driver that runs under Windows 9x.

Installation of the Windows driver in Win95 begins by first ensuring that you have the drivers stored on a floppy disk. From the Windows start up select 'Start' then 'settings', 'control panel' and 'Add new Hardware'. Now in the Hardware Wizard click 'Next' and select 'No' from 'Do you want Windows to search for new hardware?' now click 'Next', scroll down the list of controllers in 'Hardware types' and click-on SCSI controllers. Click 'Next' and select 'Have disk' now choose 'Browse' and find the folder on the floppy where the drivers are stored, select ide2lpt.inf and ide2lpt.mpd. Now click 'OK'. Driver installation will take place automatically but before you can use them it will be necessary to restart the computer.

If other Windows applications access the printer port while data is transferring to and from the hard disk it can cause a problem. It is therefore recommended that no other Windows programs are allowed to access the printer port while the IDE2LPT program is running.

Plugging it all together

Figure 6 shows all the interconnections between the parts of the complete adapter. A standard printer cable can be used to connect the portable hard disk unit to the LPT port of the PC. Alternatively a cable can be made-up using flat ribbon cable with crimp-on (IDC) D-type connectors. Ideally the cable length should be less than 30 cm. If you suspect that sources of radio frequency interference (RFI) are causing problems then the eight data lines DATA0 to DATA7 may benefit by connecting decoupling capacitors of between 12 to 22 pF from each data line down to earth at the adapter connector K1.

Power for the hard disk drive and adapter PCB is best provided by a separate PC Power Supply Unit (PSU). These units provide the necessary supply voltages with bags of current to spare. There should be no problem in finding such a unit especially if you are cannibalising a redundant PC system. Alternatively a new unit can be purchased quite cheaply. Power connections between the HDD and the PSU can be made with a standard computer internal power expansion cable with two wire taps taken off to provide +12 V and 0 V to the adapter card. These two wires should be soldered to the pins labelled + and 0 next to C1 on the PCB.

Gigabytes to go

Whether you are purchasing a new hard disk drive for this project or recycling a unit from a redundant PC system, this design gives even low-spec PCs (those without CD or CD-RW drives) the ability to store, back-up or transfer large files to and from other PC systems.

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Postscript:

The interface described in this article was built on a prototype board (see photos) and tested with a number of PCs and hard disk drives. These test runs were completed without problems.
Just before the closing date of this issue, we received information from the author regarding possible timing problems with a number of older PCs. According to the author, such problems occur in rare cases, only on motherboards containing a Pentium I processor, and depending on the I/O chip set fitted.