6_Part 2_ Interface circuits

6.4 Interface circuits

The relay coil and MDAC control signals are produced in the microcontroller PCB (slot 2 of the card frame, connectors JM1 and JM2) and reach the relay and MDAC PCBs via the interface PCB (slot 3, connectors JI1 and JI2). The relay PCB has connector JR1 and the MDAC PCB has connectors JS1 to JS4.

For details of the power supplies and opto-couplers see section 5.2.12.

The control lines are in the form of 4 bits of data, 3 bits of address and 3 lines for selecting the channel: -
a). Bridge ratio (relay coils and MDAC)
b). Carrier amplitude MDAC
c). Fine gain MDAC.

The final control line is a write pulse (active low). See fig. 6.4.3.

The required data, address and channel are established followed by a short pulse of the write control.

The data lines are labelled D0 (LSB) to D3 (MSB) consistent with the data sheet for the AD 7542. See fig. 6.4.2.

The address lines are labelled A0 (LSB) to A2 (MSB) according to the usual convention. See fig. 6.4.3.

The non-inverting buffer therein (IC14: 74LS04) is actually four inverting buffers in series: -

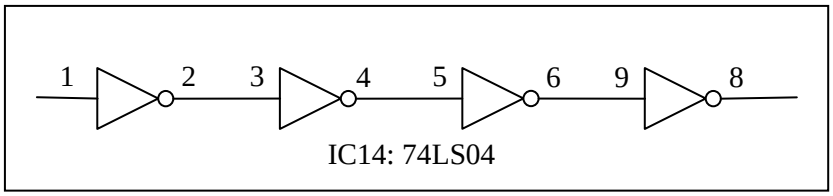


Fig. 6.4.1 Non-inverting buffer

The inputs of the unused buffers of IC14 are pulled up to 5V (B) by *R16 (1k0)*.

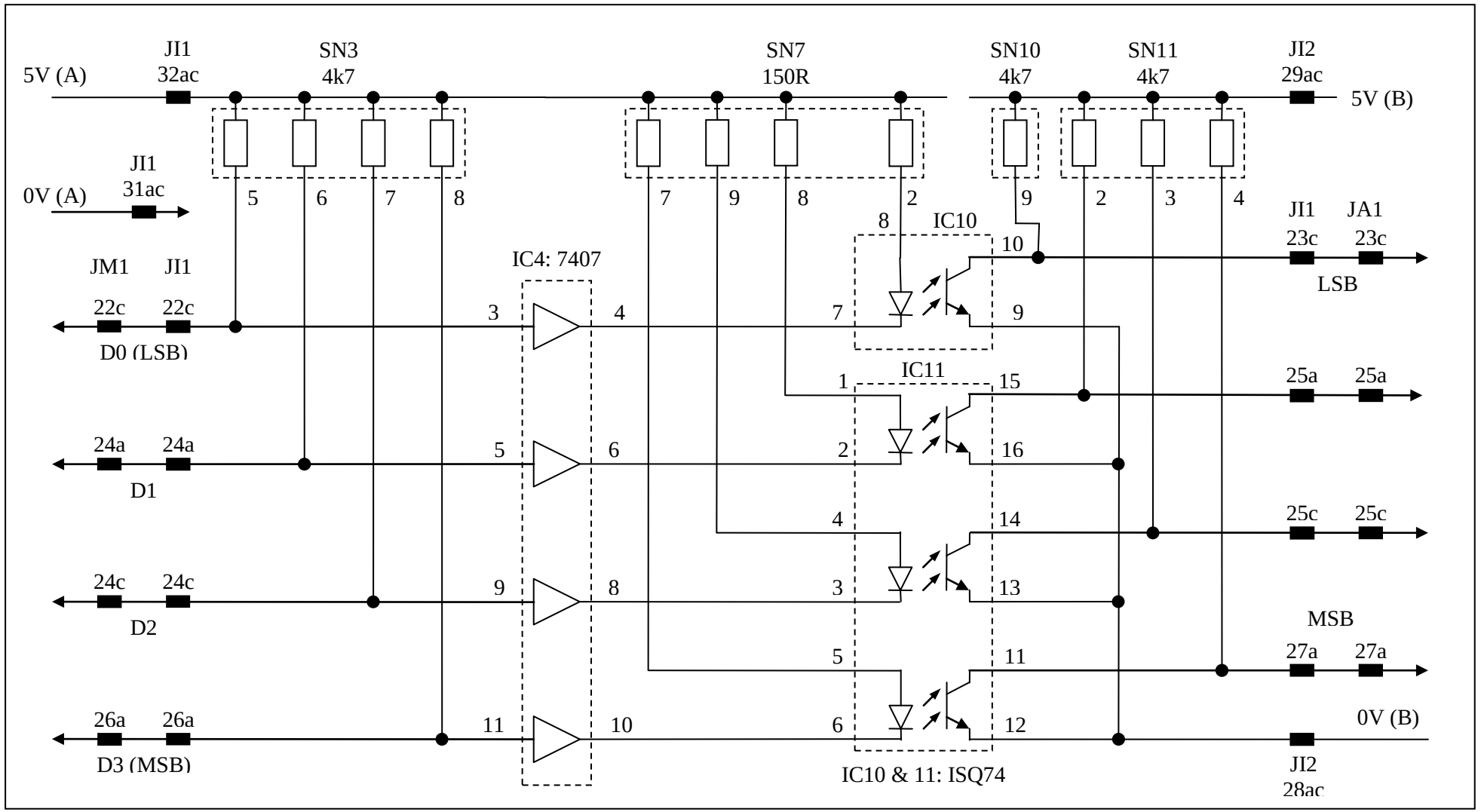


Fig. 6.4.2 Data interface

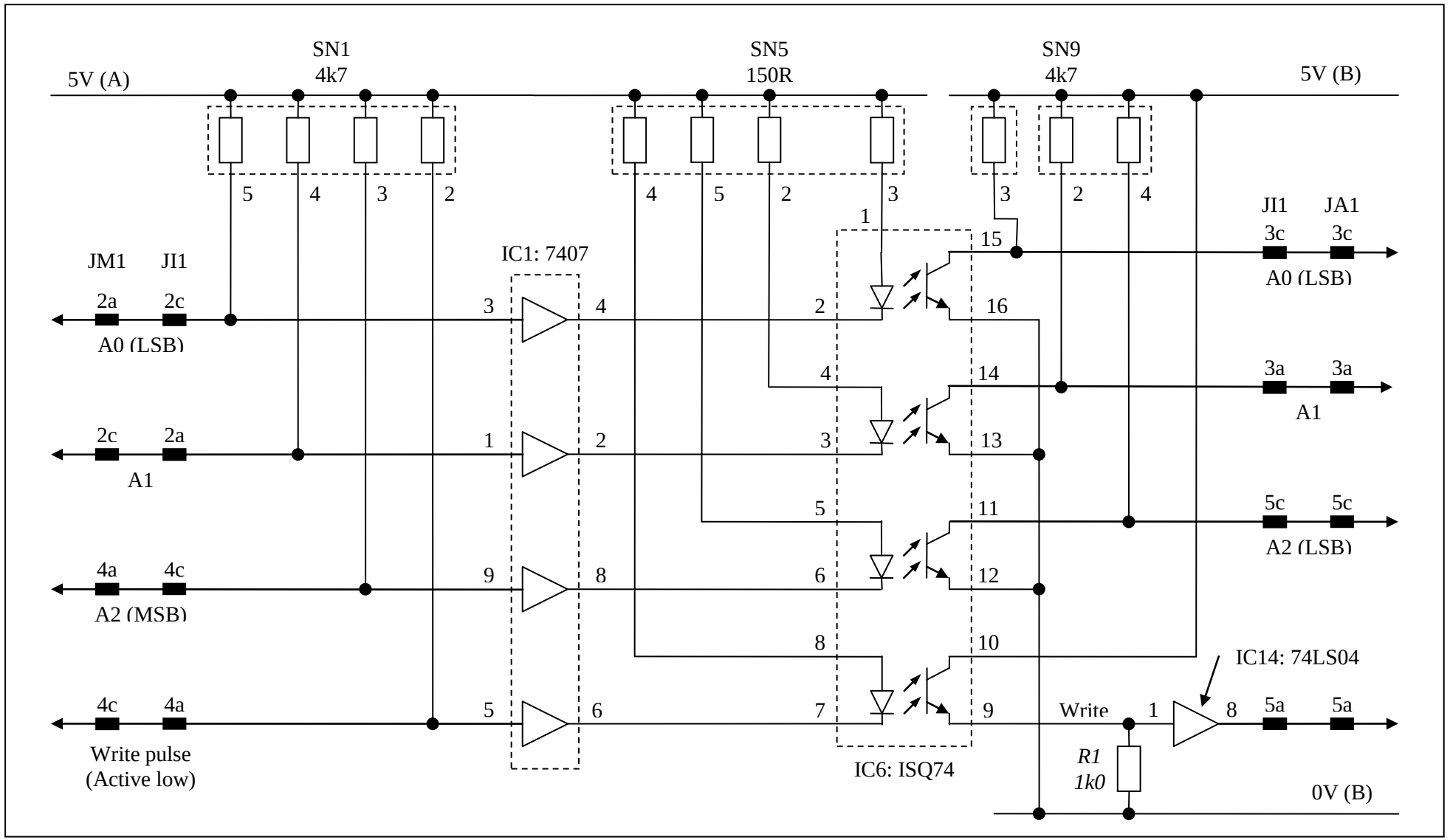


Fig. 6.4.3 Address lines and write pulse interface

In addition to the three address lines there are three controls for selecting the target for the data: -
a). Fine gain control MDAC chip enable.
b). Bridge ratio: the ratio transformer relays and MDAC for the last three decades.
c). Fine control of bridge current MDAC.

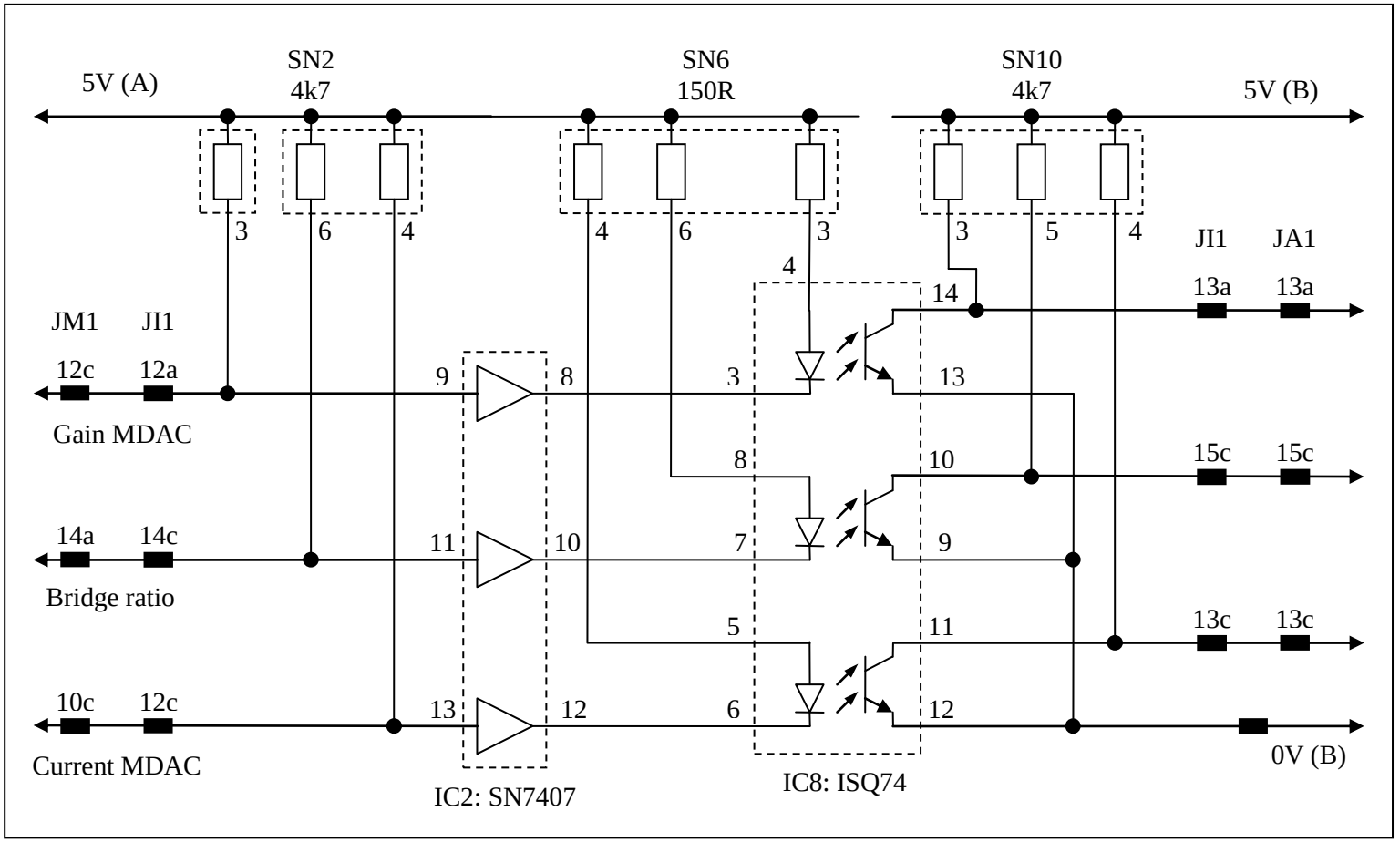


Fig. 6.4.4 Channel select interface

Similarly for the unity and zero ratio check relay drivers: -

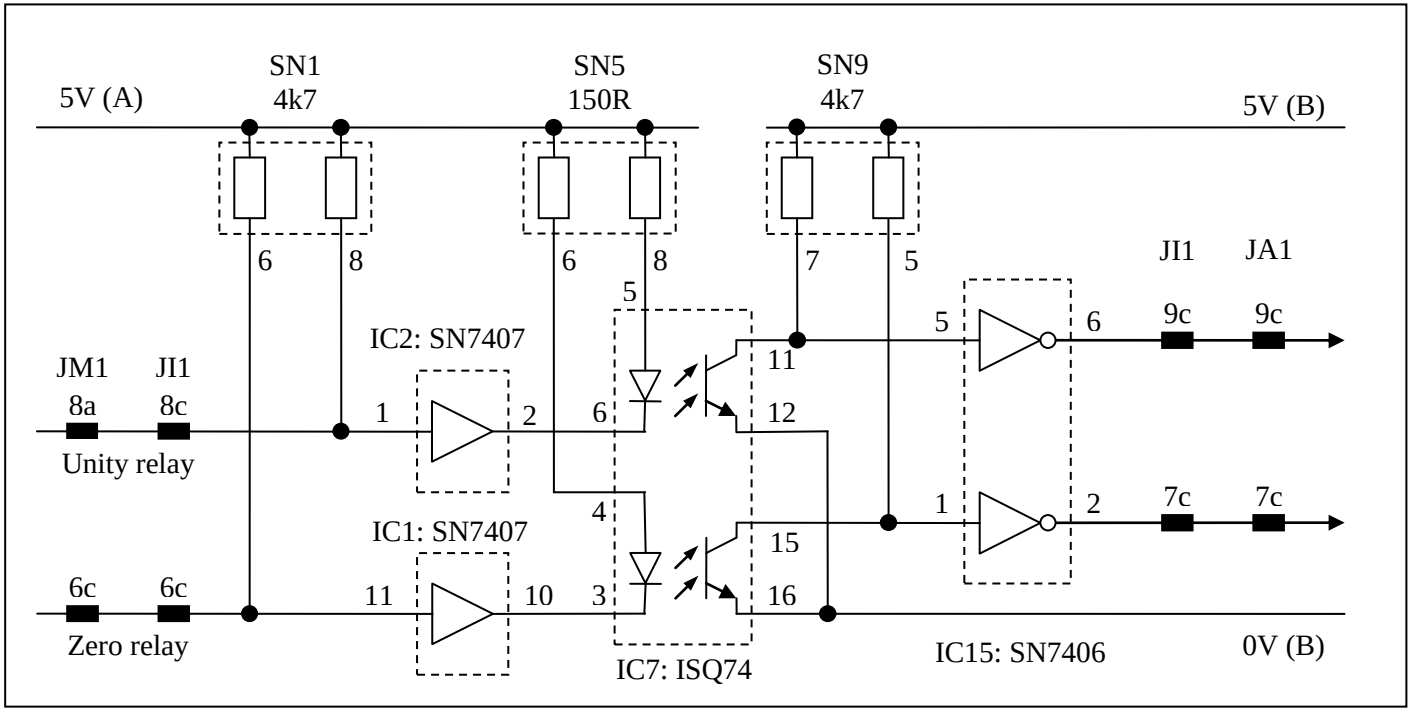


Fig. 6.4.5 Zero and unity ratio check interface

ASL F18 circuits

Data, address and write pulse (active low) controls can be traced from the interface chip IC8 (8255) on the microcontroller PCB (slot 2) through the interface PCB (slot 3) to the amplifier/filter PCB (slot 6): -

Control	Port	Pin	JM1	JI1 (input)	JI1 (output)	JA1 (input)
D3 (MSB)	A3	1	26a	26a	27a	27a
D2	A2	2	24c	24c	25c	25c
D1	A1	3	24a	24a	25a	25a
D0 (LSB)	A0	4	22c	22c	23c	23c
A2 (MSB)	A6	38	4a	4c	3c	3c
A1	A5	39	2c	2a	3a	3a
A0 (LSB)	A4	40	2a	2c	5c	5c
WR	A7	37	4c	4a	5a	5a

Similarly for the channel select controls from IC8 (8255) port B: -

Control	Port	Pin	JM1	JI1 (input)	JI1 (output)	JA1 (input)
Gain MDAC	B1	19	12c	12a	13a	13a
Bridge ratio	B2	20	14a	14c	15c	15c
Current MDAC	B0	18	12a	12c	13c	13c

Zero and unity ratio check interface is via the amplifier/filter PCB (slot 6): -

Control	Port	Pin	JM1	JI1 (input)	JI1 (output)	JA1 (input)
Zero	B3	21	6c	6c	7c	7c
Unity	B4	22	8a	8c	9c	9c

How do the control lines reach the MDAC PCB? There must be another connector on the amplifier/filter PCB.

The ratio is also displayed on the front panel via eight seven-segment LEDs mounted on the display PCB.

The interface from the microcontroller PCB to the display PCB (including manual balance rotary switches, buttons and LED indicators) is included here for completeness.

The ratio is also displayed on the eight digit 7-segment LED display on the display PCB. The BCD data for each digit originates from IC7 (8155) on the microcontroller PCB and passes via connectors J4 and JD1. Once stable the data is latched with a write pulse (WRP) on pin 5 of the CD4511 latch/decoder (active low): -

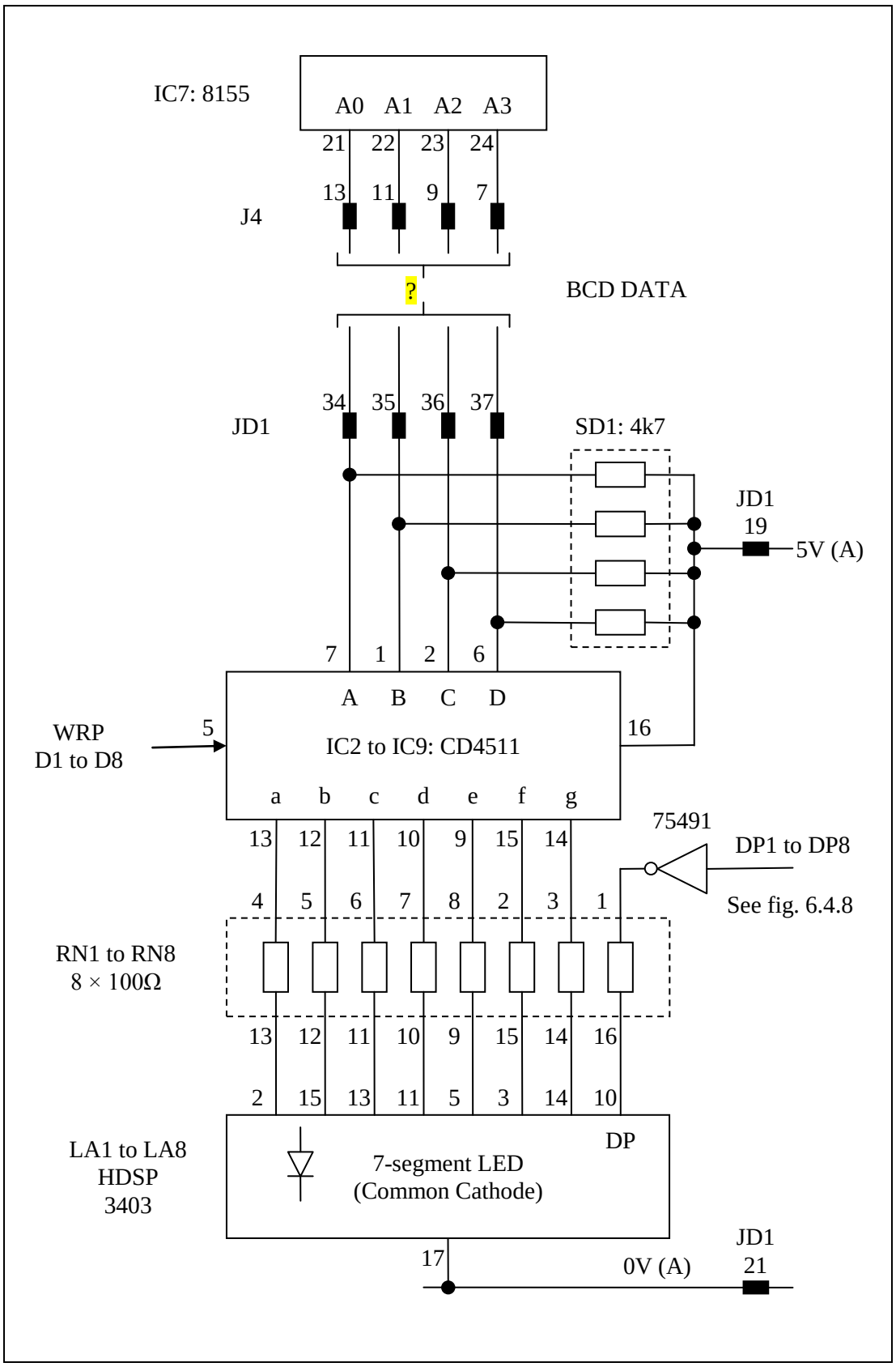


Fig. 6.4.6 Display data interface

Information required: the order of connection between J4 and JD1 (probably A0 to A etc as both are LSB).

ASL F18 circuits

The relevant chips, resistor networks and LEDs are labelled as follows: -

Digit	1 (MSD)	2	3	4	5	6	7	8 (LSD)
4511	IC2	IC3	IC4	IC5	IC6	IC7	IC8	IC9
R Network	RN1	RN2	RN3	RN4	RN5	RN6	RN7	RN8
LED	LA1	LA2	LA3	LA4	LA5	LA6	LA7	LA8

The relevant display digit is selected by decoding a 4-bit address bus to 1 of 8 write pulses (active low). The ADDRESS bus also originates from port A of IC7 (8155) on the microcontroller PCB. The DATA bus connections are repeated for convenience: -

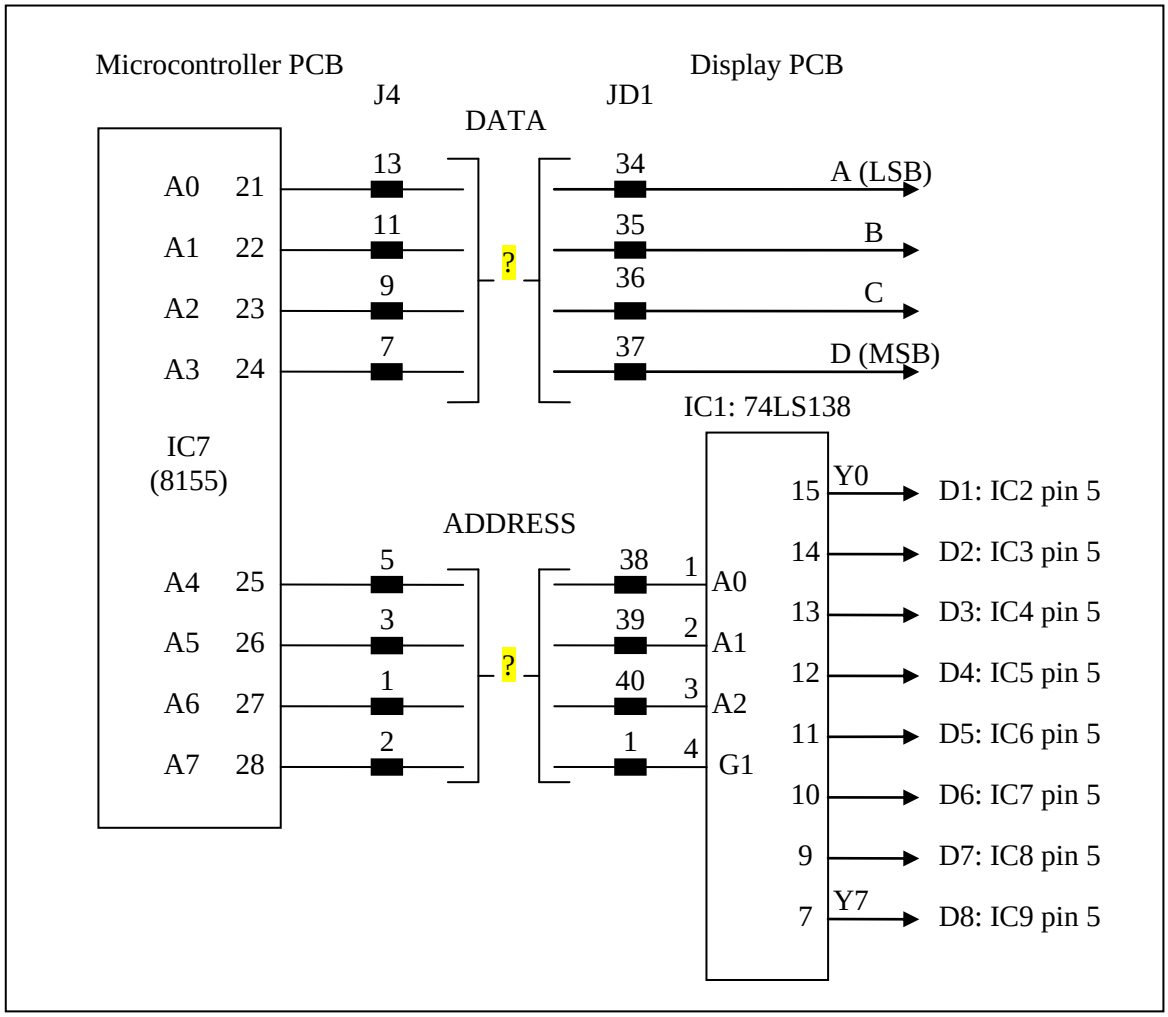


Fig. 6.4.7 Display address and data interface

Information required: the order of connection between J4 and JD1 (probably A4 to A0 etc as both are LSB).

Enable control G1 is active high.

The unused enable controls of IC1 (74LS138 pins 4 and 5) are active low and hard-wired to 0V.

Power supplies to IC1 are 5V (pin 16) and 0V (pin 8).

The relevant decimal point is illuminated by decoding a separate (3-bit) address bus originated from port B of IC7 (8155): -

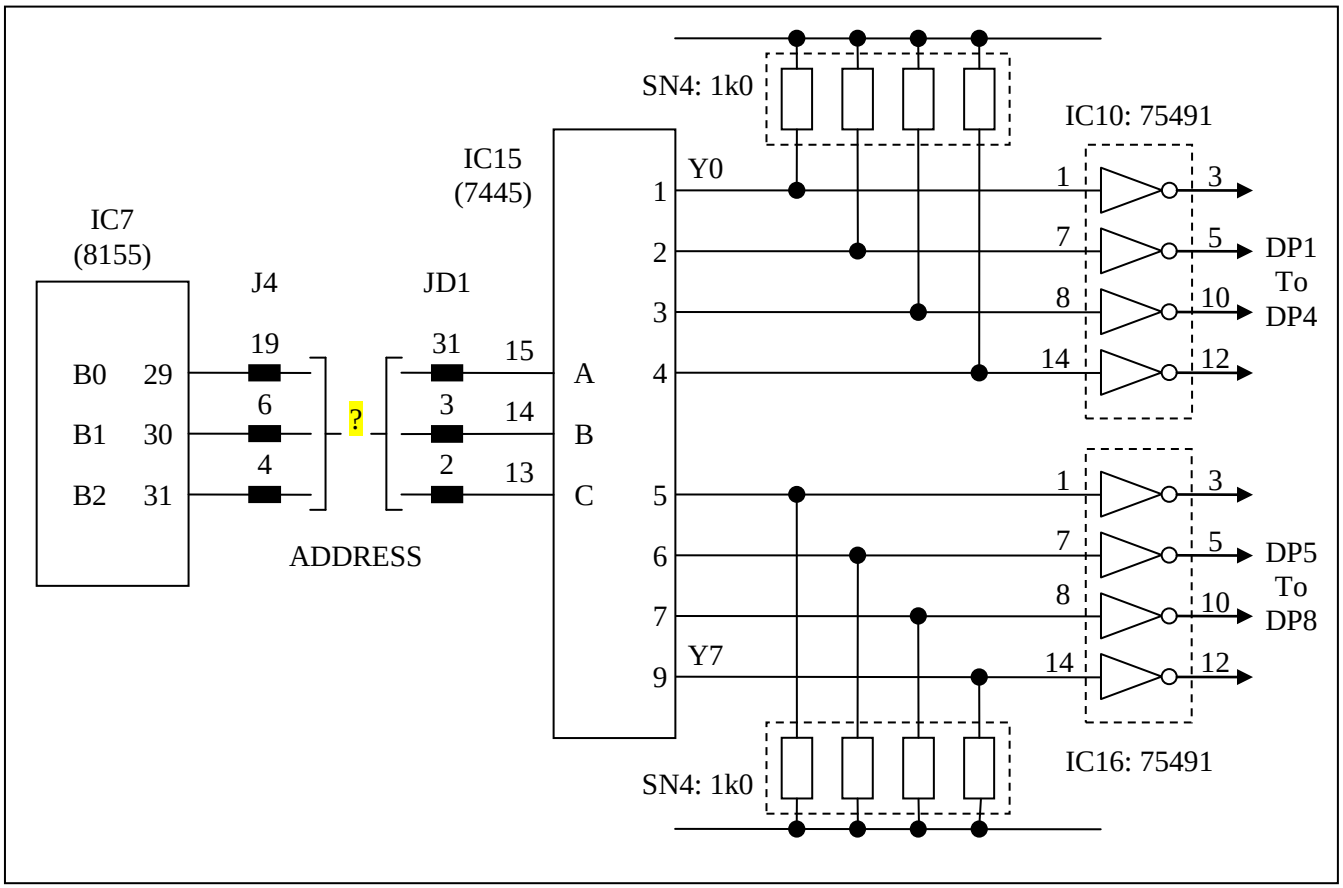
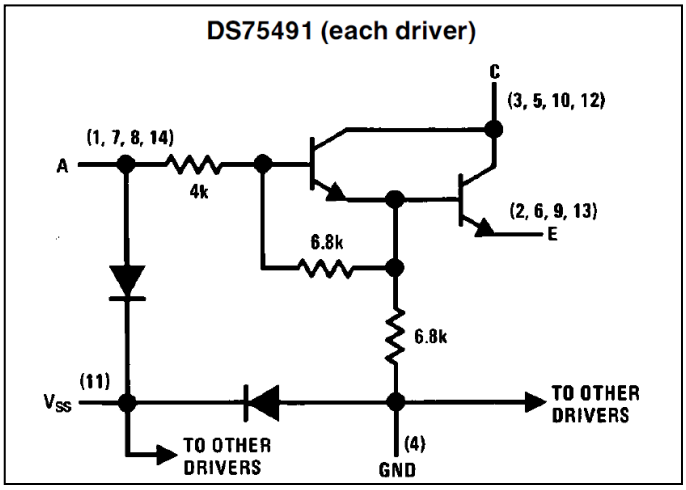


Fig. 6.4.8 Data interface

Information required: -
1. The order of connection between J4 and JD1 (probably B0 to A etc as both are LSB).
2. Please confirm the pin connections for IC10?

The decoded output of the 7445 is low so that the inverted outputs of IC10 (75491) are employed. These are the collectors of the Darlington pairs. The emitters are connected to 5V (A). Viz: -



Whereas NPN transistors are partly symmetrical the current gain with C and E interchanged is much reduced.

The ratio can be set manually with eight rotary switches. The relevant switch is selected by a 1 of 8 decoded address (active low) originating from port B of IC7 (8155). The BCD data returns to IC7 port C via connectors JD1 and J4. The diodes ensure that only the selected switch output can be pulled low. Viz: -

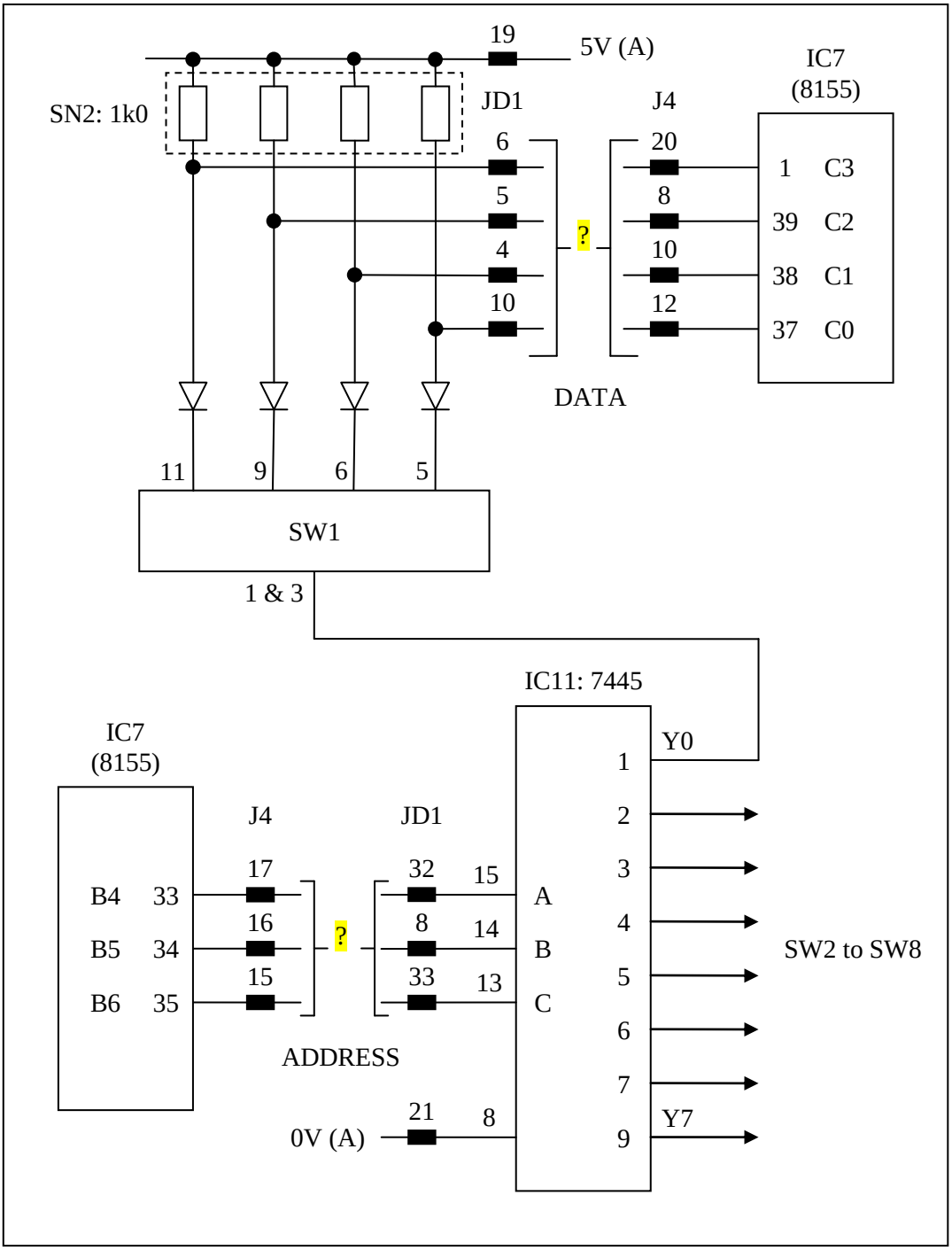


Fig. 6.4.9 Data interface

Information required: -
1. The order of connection between J4 and JD1 (probably B4 to A etc as both are LSB).
2. Pin connections for the switches and order of connection between JD1 and J4. Which is LSB etc?

The interface circuits for the buttons and LED indicators are also here for completeness – they are also on the display PCB.

There are four LEDs for overload indication (which is which?) and an array of buttons, each with its own LED.

Firstly the LED and button matrix: -

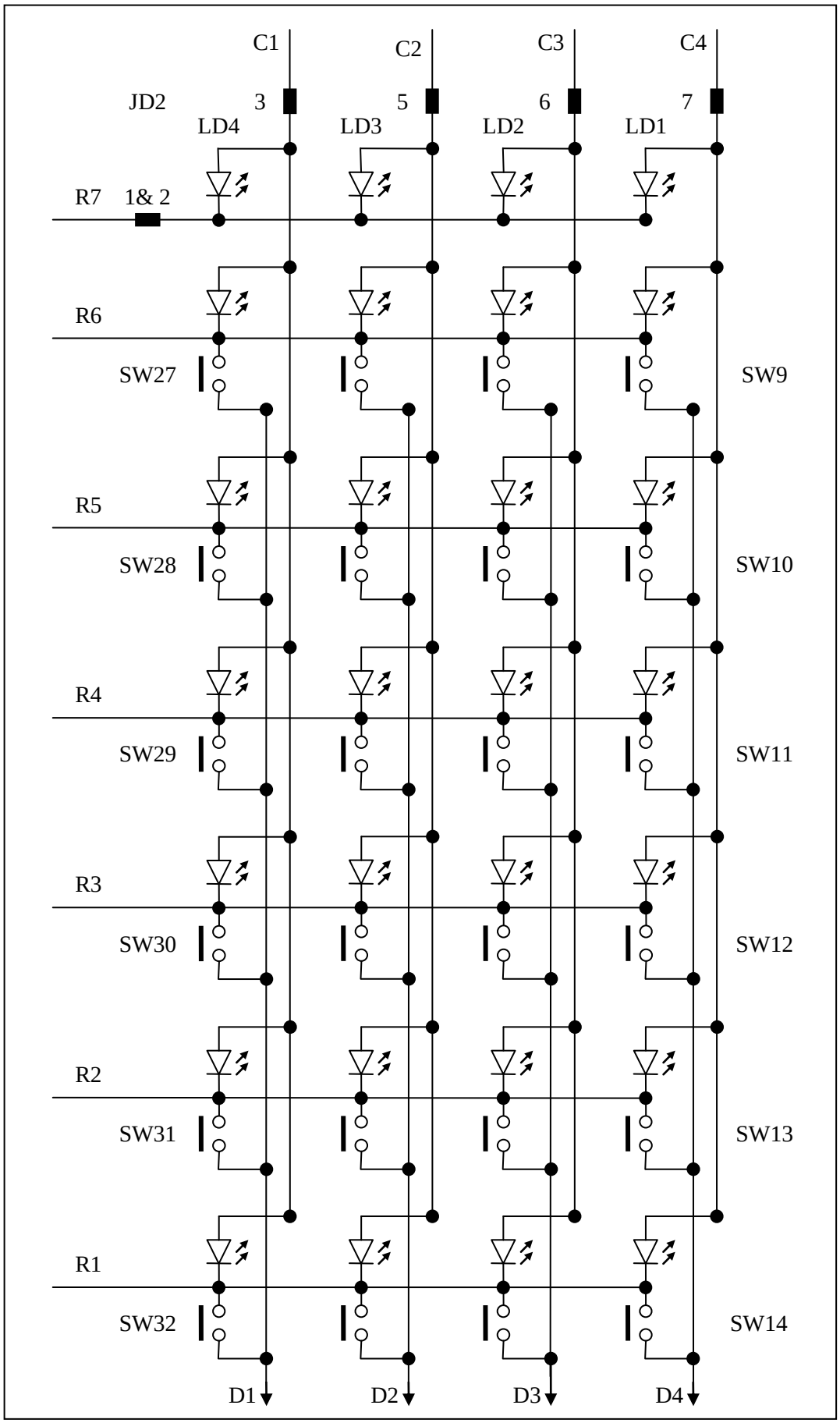


Fig. 6.4.10 LED and button matrix

The matrix is scanned by the keyboard/display interface IC6 (8279) on the microcontroller PCB. First is the LED driver circuit: -

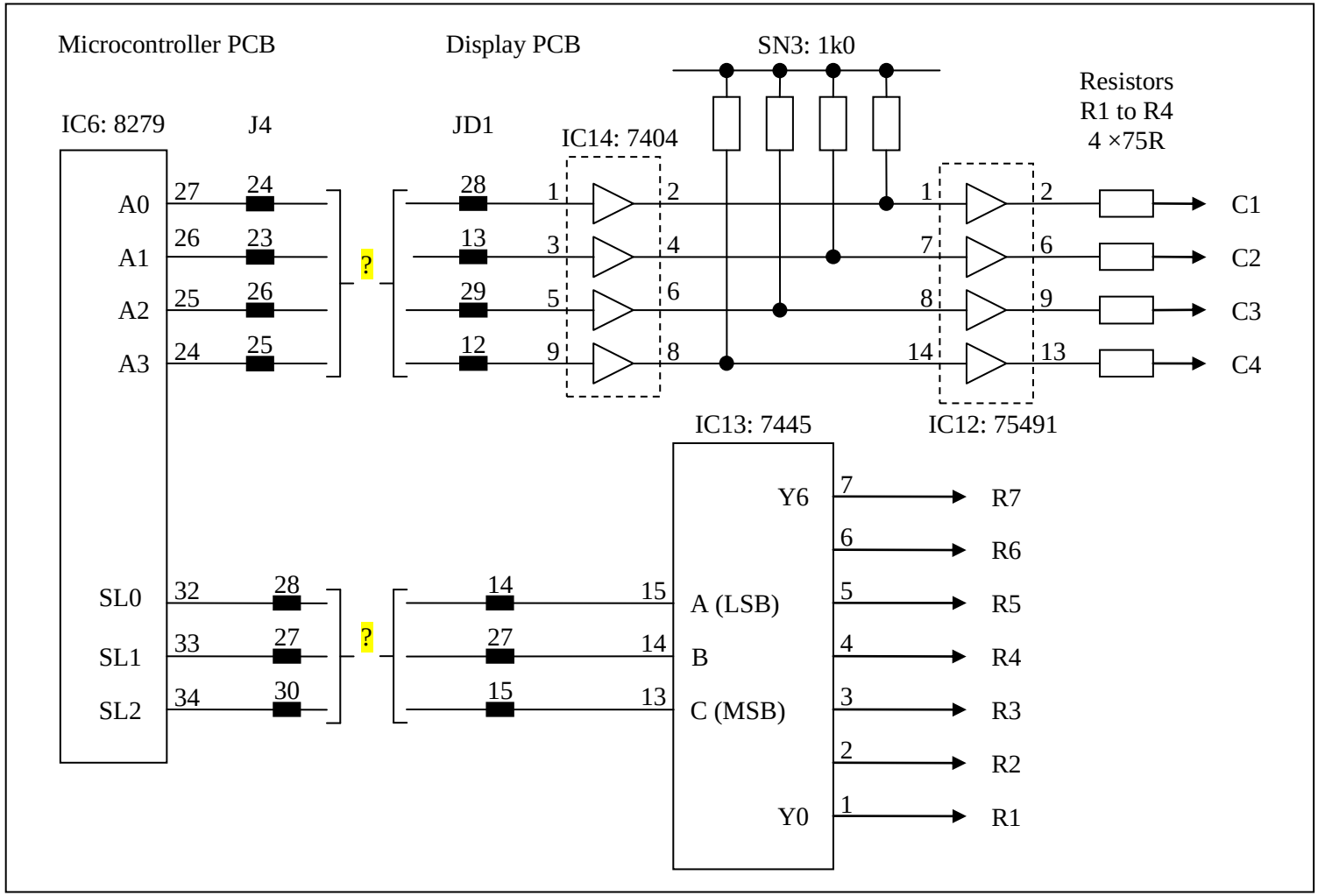


Fig. 6.4.11 LED interface

Information required: the order of connection between J4 and JD1 (probably SL0 to A etc as both are LSB. A0 to C1 etc appear to be arbitrary).

The column select lines (A0 to A3) appear to be pre-decoded (1 of 4: internally set) obviating the need for an external decoder.

The data lines from the matrix return to IC6 (8279): -

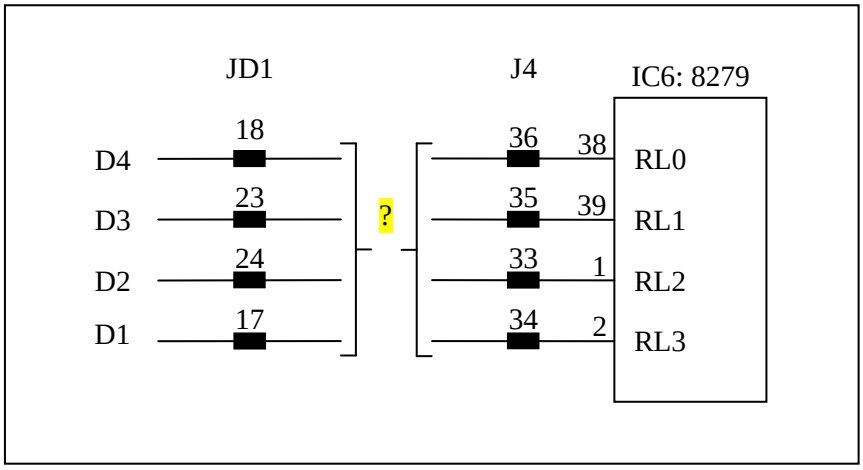


Fig. 6.4.12 Data interface

Information required: the order of connection between JD1 and J4. The order appears to be arbitrary.

The return lines (RL0 to RL3) have internal pull-ups so that they are only pulled low by the selected row (R1 to R7 are active low) and a button press.