5. The null detector pre-amp and PCB1

The null detector consists of three modules. In this document are: -
a). A low noise pre-amplifier with transformer for noise matching in a mumetal box for screening.
b). An amplifier/filter PCB in slot 6 of the card frame (PCB1).

In a second document (5_The null detector PCB2): -
c). Phase sensitive detectors and quadrature servo in slot 5 of the card frame (PCB2).

The card frame slots are numbered from right to left, as seen from the top and front. Please check.

For an overview see section 1.7. More details can be found in the monographs [1, 2 and 3].

5.1 The low noise pre-amplifier

Near ideal impedance matching, from 0.3Ω – 300Ω to a BJT matched pair, is achieved with a single-stage transformer. The transformer has three settings (nominally 1, 10 and 100Ω source resistance): -

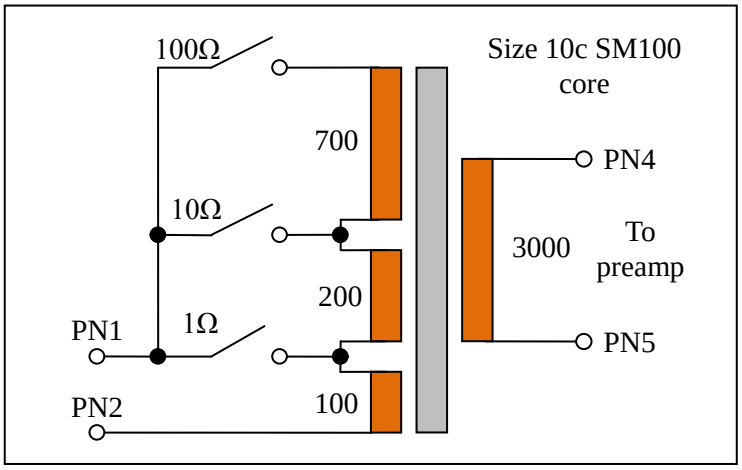

Fig. 5.1.1 A noise matching transformer for low source resistance

The transformer ratio is selected by one of three glass-encapsulated (SPST) reeds: -

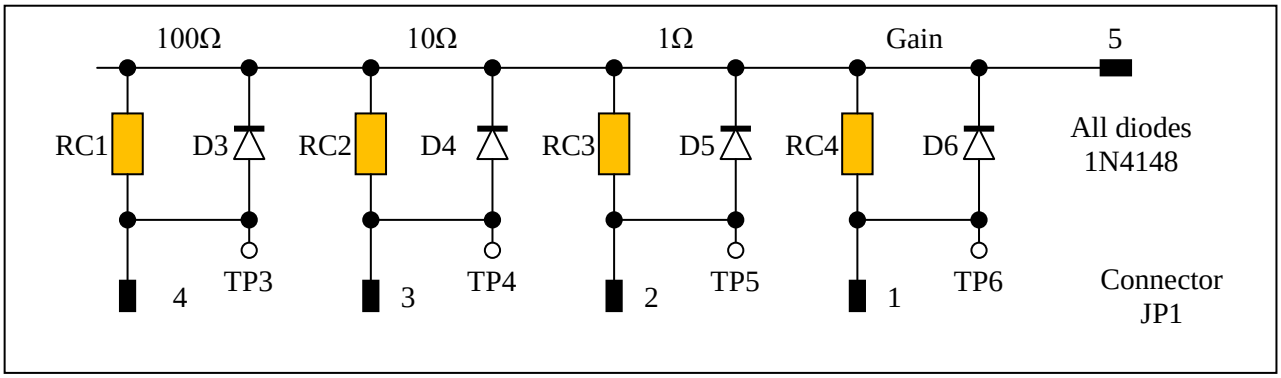

Fig. 5.1.2 Relay coils

The fourth coil selects the gain of the pre-amp with a SPDT reed. See fig. 5.1.3.

See section 5.2.10 and 5.2.12 for the relay control line interfaces.

1. Part 3, monograph 5: “Noise matching transformers”.
2. Part 5, monograph 2: “Low noise BJT pre-amps”.
3. Part 5 monograph 1: “Null detectors – the basics”

The low noise pre-amp (×1 or ×1000) employs a long-tail pair front-end: -

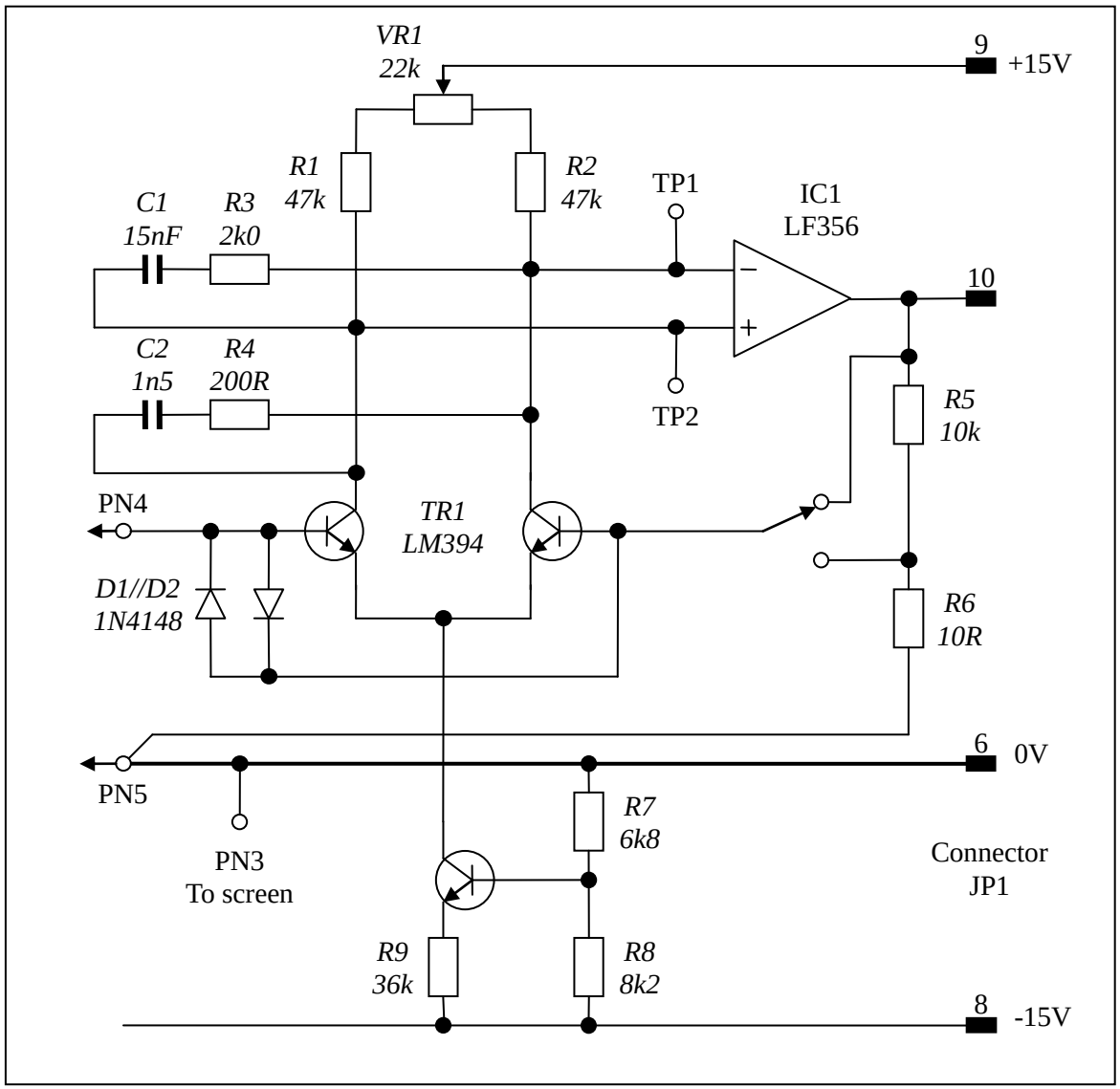

Fig. 5.1.3 Pre-amplifier

Each transistor operates at 0.1mA. According to the data sheet the expected input noise resistance is approximately 3kΩ (at 75Hz) and1.3kΩ (at 25Hz). In practice the noise matching is good (> 60%) from 0.4Ω to 400Ω [1]: -

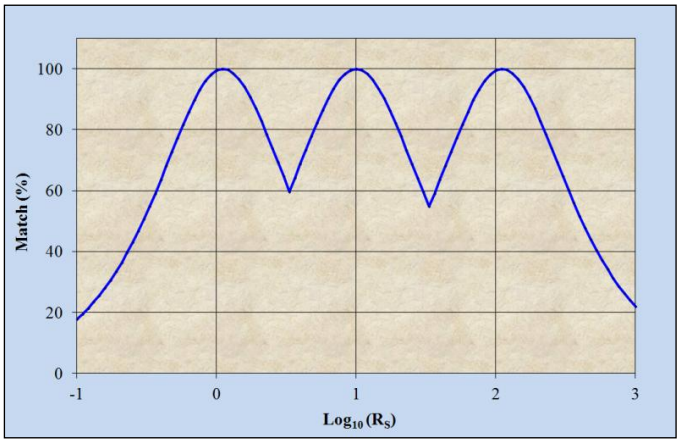

Fig. 5.1.4 Noise matching (theoretical)

1. Part 3, monograph 5: “Noise matching transformers”.

5.2 Amplifier and filter PCB

Most of the amplification and filtering is on a double euro-card in slot 6 of the card frame. The overview is repeated here for convenience. For details on the frequency select and gain control interfaces see section 5.2.12: -

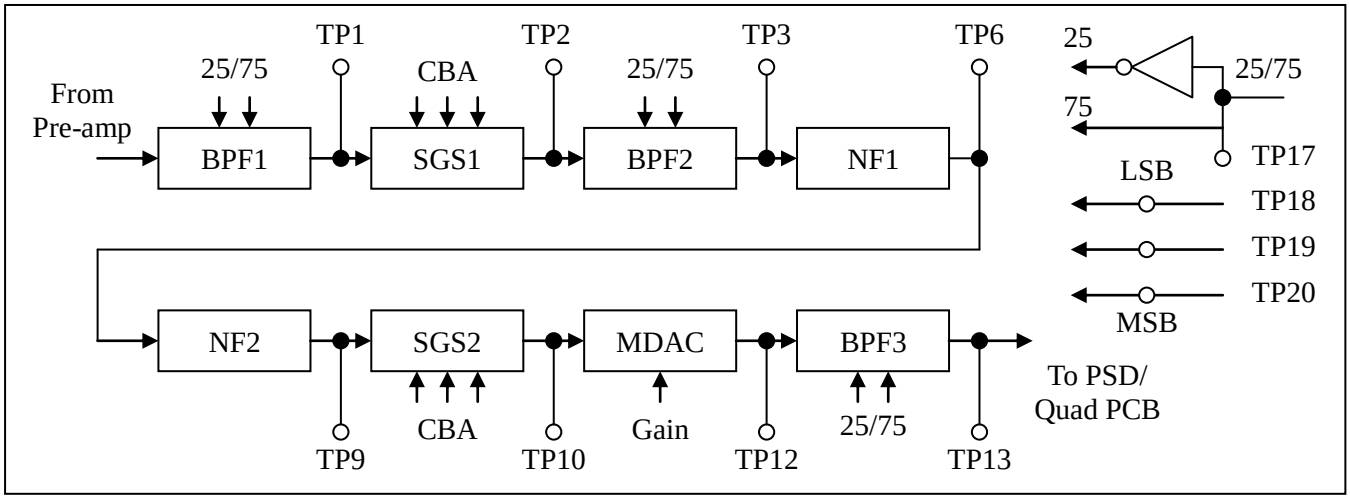

Fig. 5.2.1 Overview of amplifier/filter PCB

The frequency select control (25/75) arrives via connector JA1 17a. See section 5.2.12 for details.

5.2.1 Band-pass filter BPF1

The first band-pass filter is selectable (25Hz or 75Hz). Low noise is essential, hence the superior op-amp.

The 25/75Hz control lines are derived from a single control line (see fig. 5.2.8.1): -

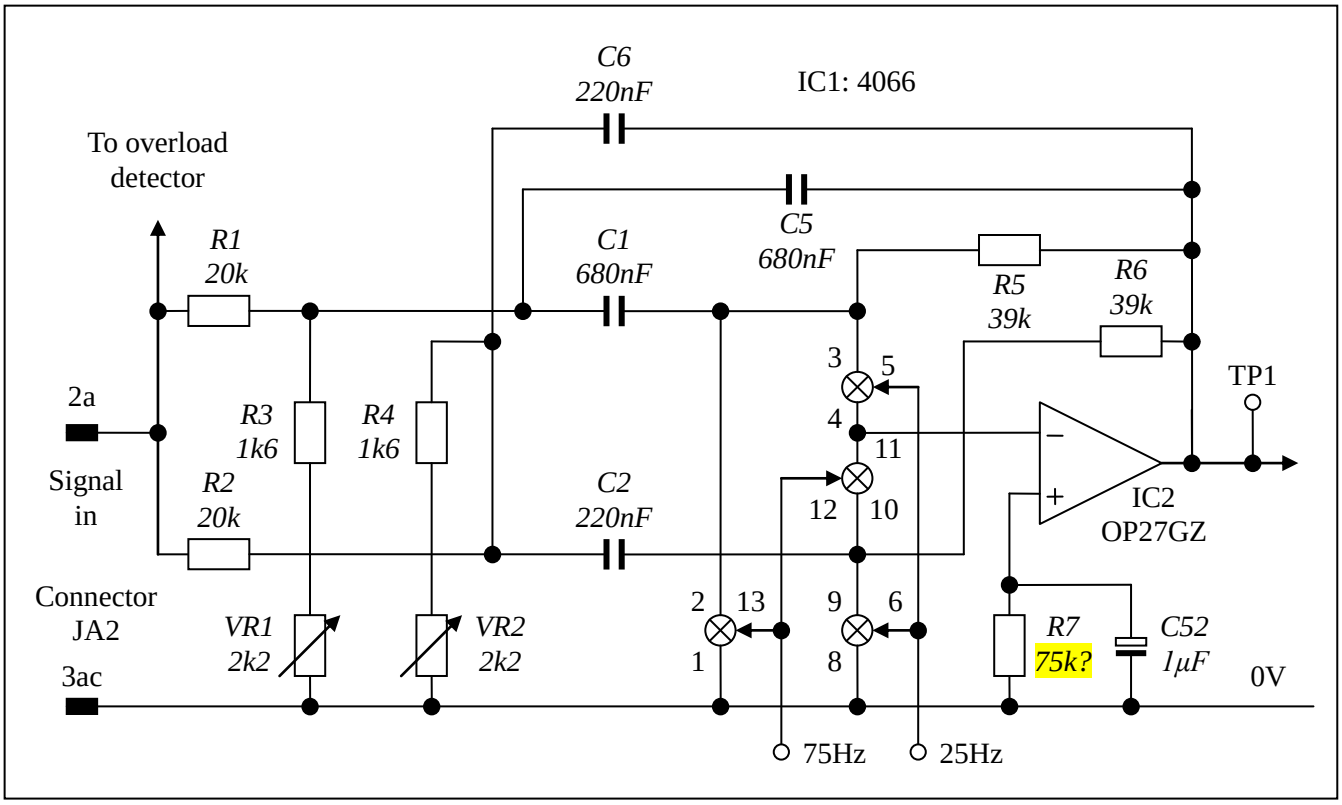

Fig. 5.2.1.1 Band-pass filter BPF1 (75Hz)

The offset trimmer for IC2 (not shown) is *VR3*. The power supply for IC1 is +7V5 (pin 14) and -7V5 (pin 7).

5.2.2 Switched gain stage (SGS1)

The first switched gain stage also requires very low noise, hence another superior op-amp: -

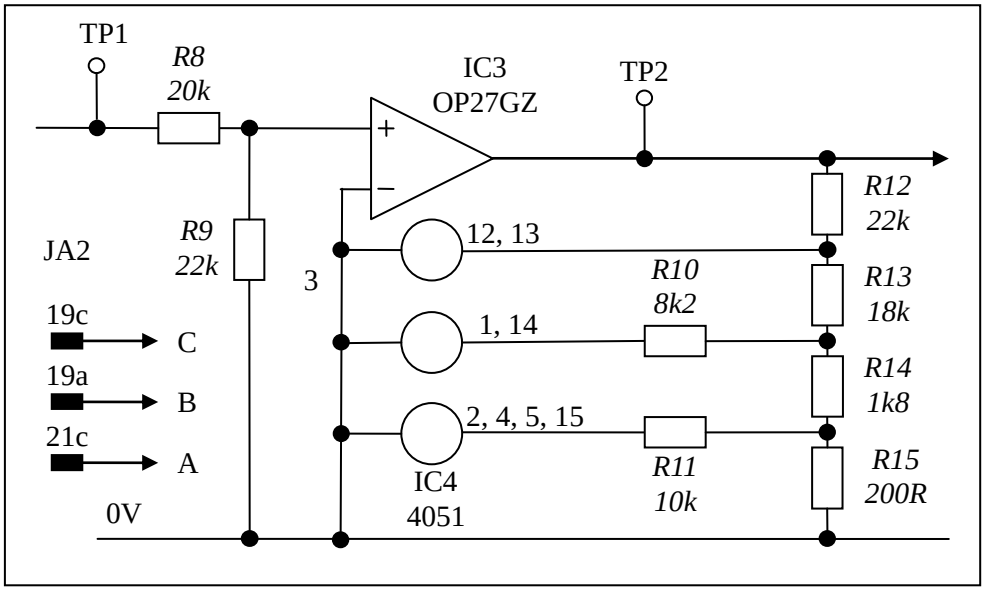

Fig. 5.2.2.1 Switched gain stage (SGS1)

The offset trimmer for IC3 (not shown) is *VR4*.

The C, B, and A control lines, as defined in the CD4051 data sheet, set the gain according to the truth table: -

C (MSB) Pin 9	B Pin 10	A (LSB) Pin 11	Gain (actual)	Gain (relative)	Total gain* (relative)
0	0	0	1.1	×1	×1
0	0	1	11	×10	×10
0	1	0	110	×100	$\times 10^2$
0	1	1	1.1	×1	$\times 10^3$
1	0	0	11	×10	$\times 10^4$
1	0	1	110	×100	$\times 10^5$
1	1	0	110	×100	$\times 10^5$
1	1	1	110	×100	$\times 10^5$

*The total gain includes the gain of the pre-amplifier.

Power supply for the CD4051 is: V_{DD} = +7V5 (pin 16), V_{SS} = 0V (pin 8) and V_{EE} = -7V5 (pin 7).

For details on the gain control interface see section 5.2.12.

5.2.3 Band-pass filter BPF2

The second band-pass filter is also selectable (25Hz or 75Hz): -

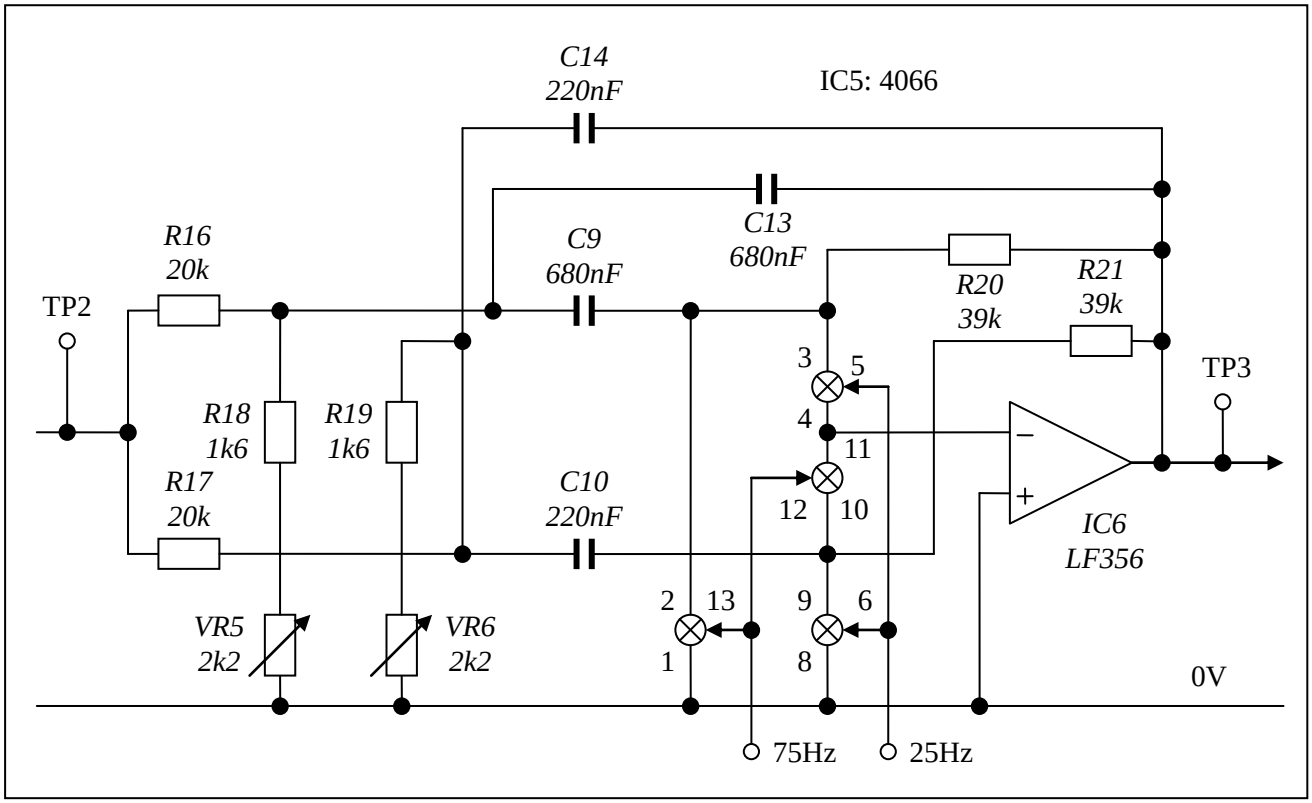

Fig. 5.2.3.1 Band-pass filter BPF2 (75Hz)

The offset trimmer for IC6 (not shown) is *VR7*.

The power supply for IC5 is +7V5 (pin 14) and -7V5 (pin 7).

5.2.4 Notch filter NF1

The first notch filter includes band-pass filters for 150Hz and 50Hz: -

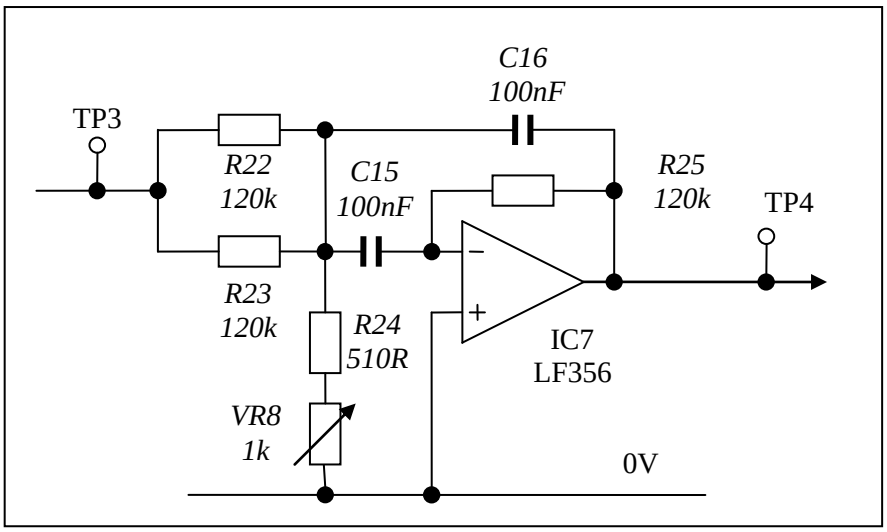

Fig. 5.2.4.1 Band-pass filter (150Hz)

Similarly: -

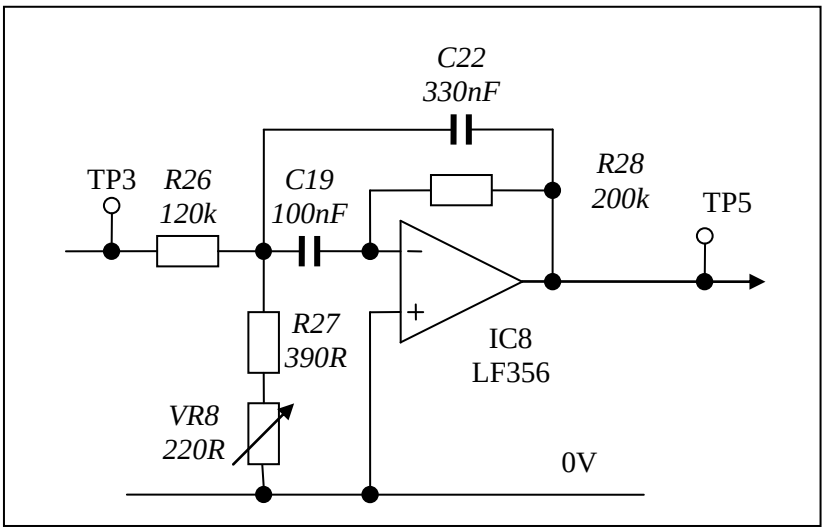

Fig. 5.2.4.2 Band-pass filter (50Hz)

The outputs of the band-pass filters are added to the original signal at the input of an amplifier: -

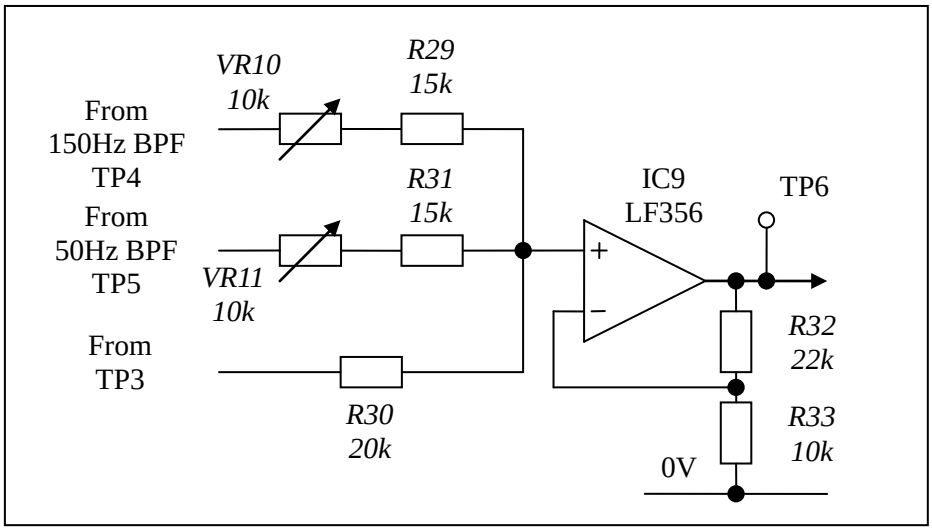

Fig. 5.2.4.3 Summing junction and amplifier

The offset trimmer for IC9 (not shown) is *VR12*.

The summing junction is not a virtual earth so that there is some interaction between the controls.

5.2.5 Notch filter NF2

Similarly: -

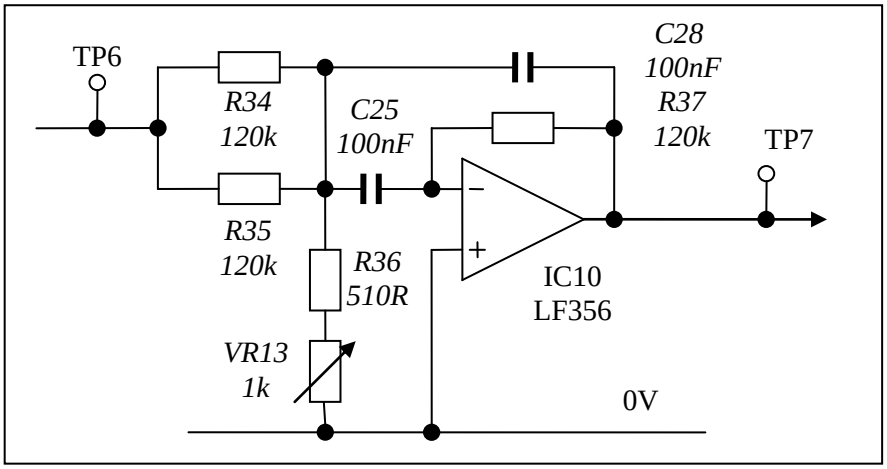

Fig. 5.2.5.1 Band-pass filter (150Hz)

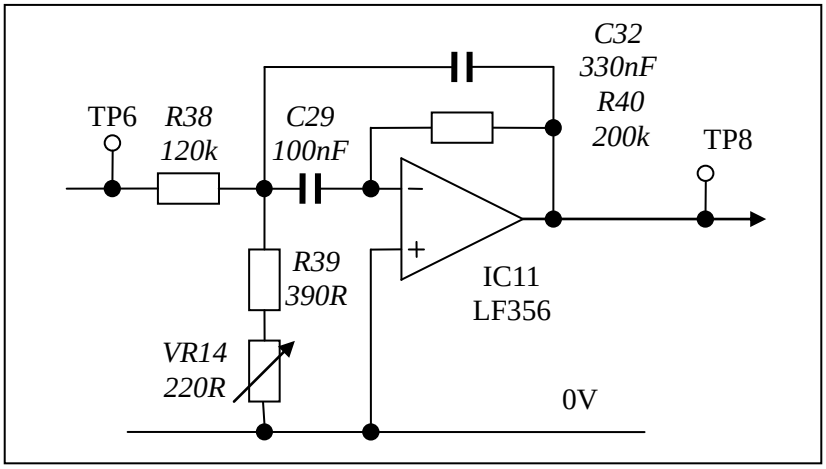

Fig. 5.2.5.2 Band-pass filter (50Hz)

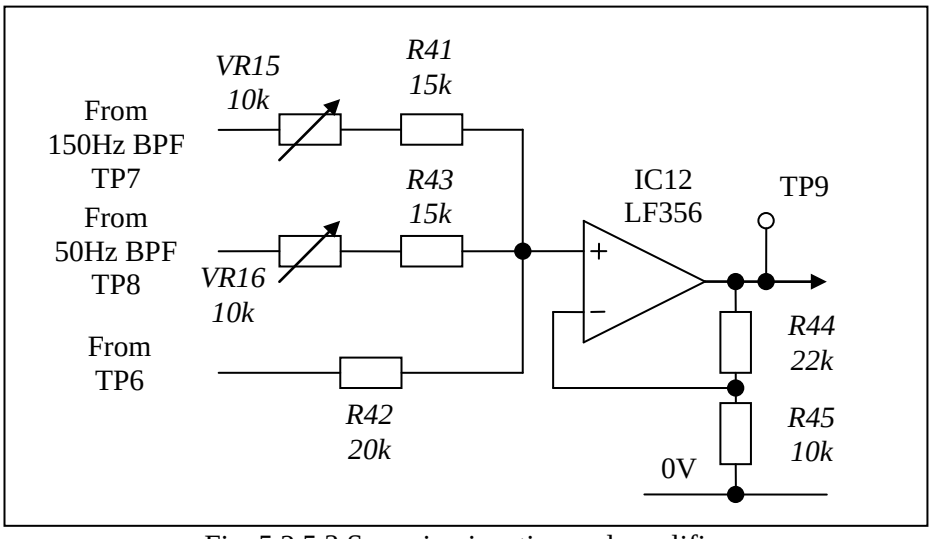

Fig. 5.2.5.3 Summing junction and amplifier

The offset trimmer for IC12 (not shown) is *VR17*.

5.2.6 Switched gain stage (SGS2)

The second switched gain stage provides for extra gain of up to ×100: -

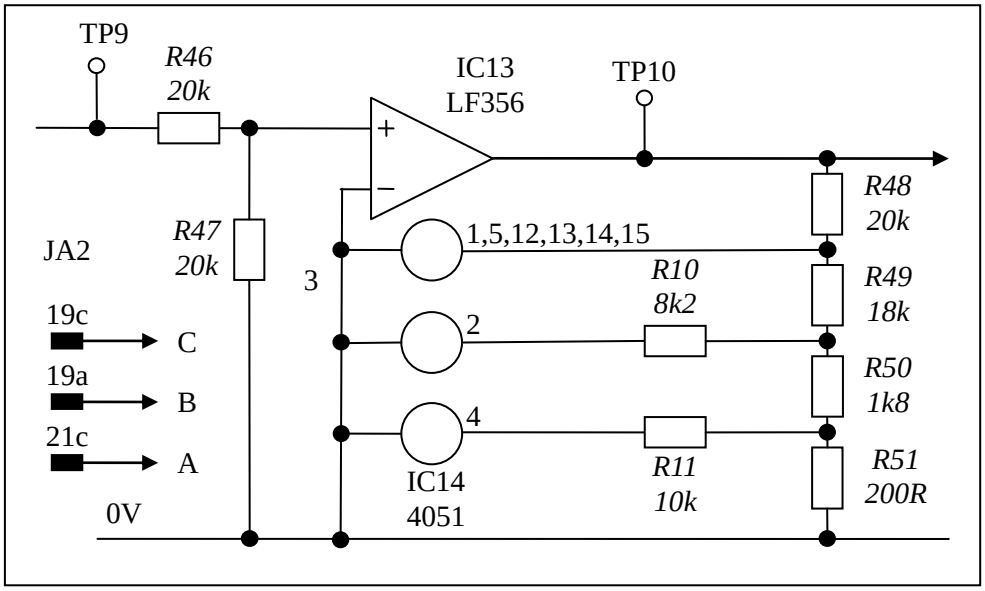

Fig. 5.2.6.1 Switched gain stage (SGS2)

The offset trimmer for IC13 (not shown) is *VR18*.

The C, B, and A control lines, as defined in the CD4051 data sheet, set the gain according to the truth table: -

C (MSB) Pin 9	B Pin 10	A (LSB) Pin 11	Gain (actual)	Total gain* (relative)
0	0	0	1	×1
0	0	1	1	×10
0	1	0	1	$\times 10^2$
0	1	1	1	$\times 10^3$
1	0	0	1	$\times 10^4$
1	0	1	1	$\times 10^5$
1	1	0	10	$\times 10^6$
1	1	1	100	$\times 10^7$

*****The total gain includes the pre-amplifier and SGS1.

Power supply for IC14 is: V_{DD} = +7V5 (pin 16), V_{SS} = 0V (pin 8) and V_{EE} = -7V5 (pin 7).

For more detail on the gain control interface see section 5.2.12.

5.2.7 MDAC variable gain stage

The overall gain includes a multiplying digital to analogue converter (MDAC with 12 bit binary code): -

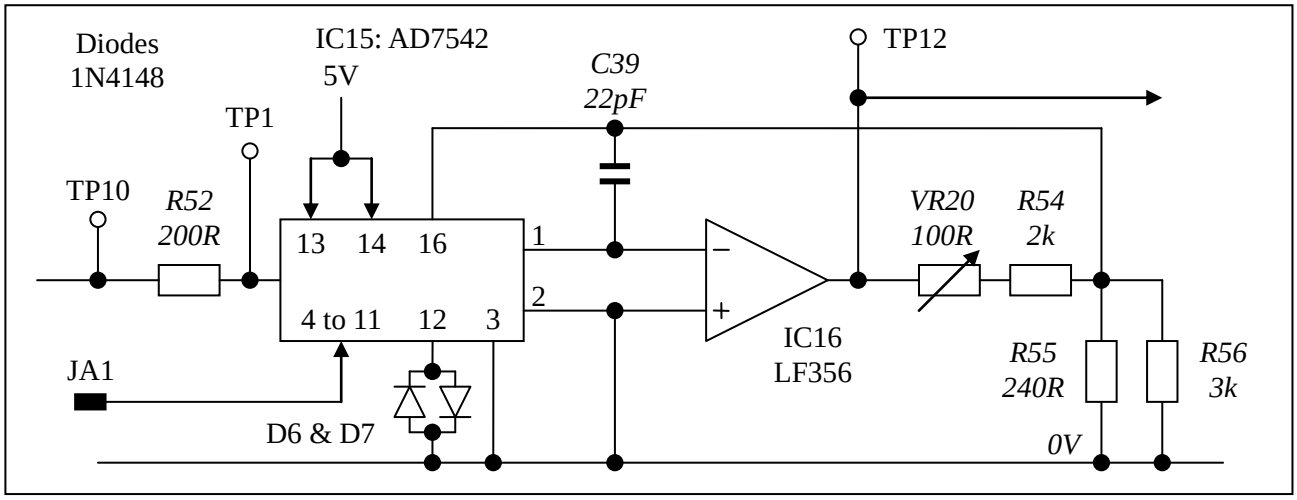

Fig. 5.2.7.1 MDAC variable gain stage

The offset trimmer for IC16 (not shown) is *VR19*.

The maximum gain is ×10 which can be set precisely with *VR20.*

It is not clear why pin 12 (DGND) is connected to 0V via diodes.

The 5V (logic) supply is produced locally: -

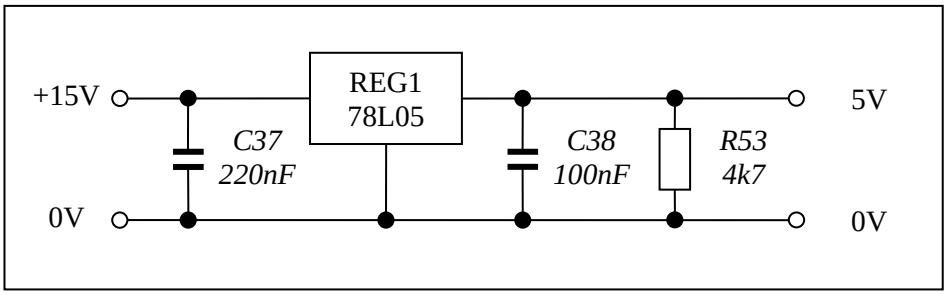

Fig. 5.2.7.2 Local 5V supply

The data and control lines arrive via connector JA1: -

IC Pin	4	5	6	7	8	9	10	11
Function	D3 (MSB)	D2	D1	D0 (LSB)	Chip select Active low	Write Active low	A0	A1
JA1 pin	27a	25c	25a	23c	13a	5a	3c	3a

For more detail on the MDAC interface see section 6.4.

The gain is set by the microcontroller in automatic balance mode. In manual balance mode it is set by the ten turn potentiometer on the front panel. The potentiometer is supplied with high precision ±10V reference voltages from a circuit on the microcontroller PCB: -

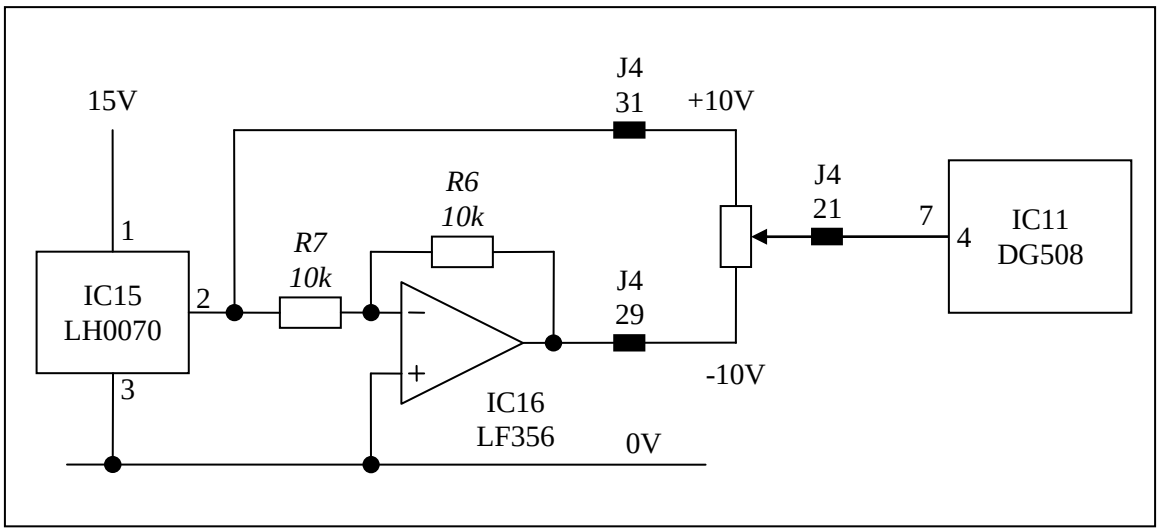

Fig. 5.2.7.3 Reference voltage circuit

Unusually the op-amp (IC16) does not have an offset trimmer.

The output of the potentiometer returns to the microcontroller PCB where it is input to channel 4 (pin 7) of IC11 (DG508) and from there to the ADC.

5.2.8 Band-pass filter BPF3

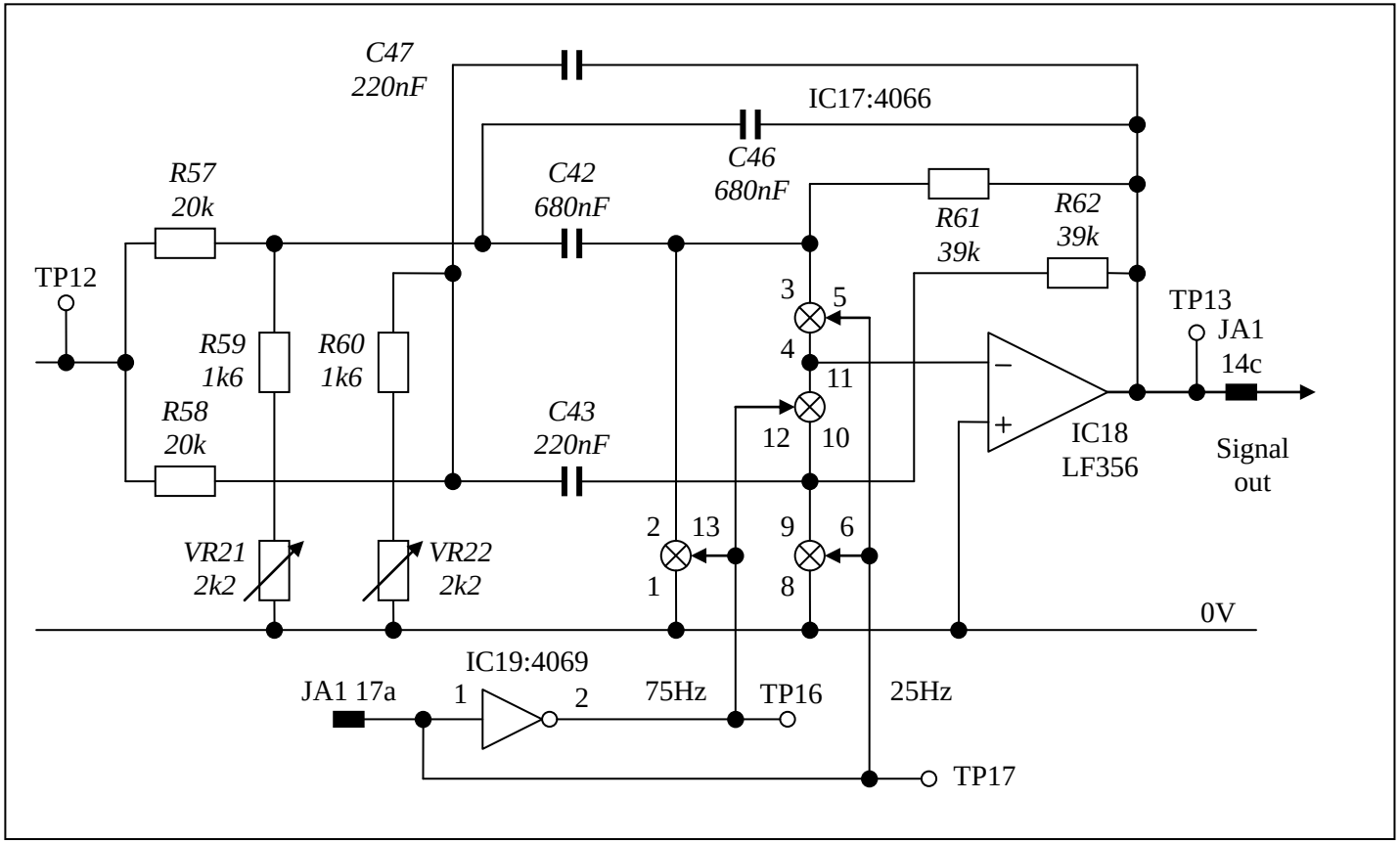

Fig. 5.2.8.1 Band-pass filter BPF3 (75Hz)

The offset trimmer for IC18 (not shown) is *VR23*. The power supply for IC17 is +7V5 (pin 14) and -7V5 (pin 7).

5.2.9 Pre-amp overload detector

Also on the amplifier/filter PCB1 is a pre-amp overload detector: -

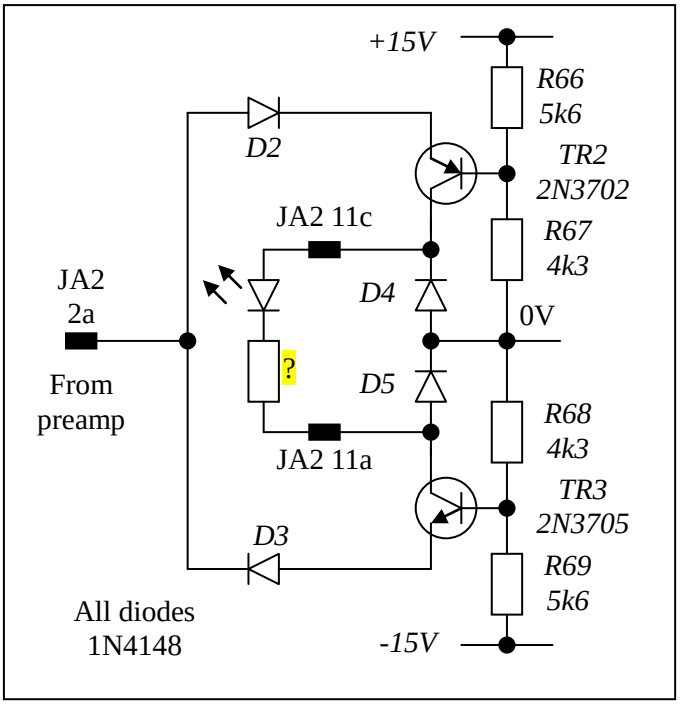

Fig. 5.2.9.1 Pre-amp overload detector

Overload is when the output of the pre-amp exceeds approximately ±8V. There appears to be no resistor in series with the photodiode.

For more detail on the (opto-coupled) interface to the microcontroller PCB see fig 5.2.12.6.

5.2.10 Pre-amp gain decoder

The three bit "gain bus" is also decoded by a CD4051 for the pre-amp gain: -

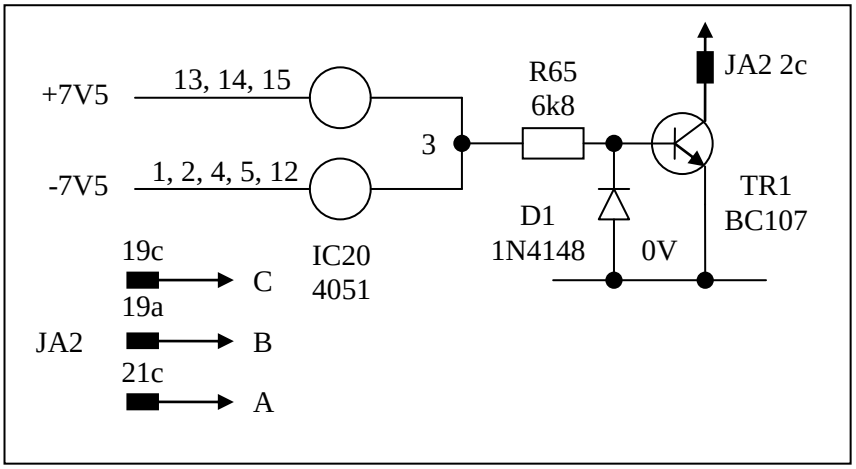

Fig. 5.2.10.1 Preamp gain decoder

The C, B, and A control lines, as defined in the CD4051 data sheet, set the gain according to the truth table: -

C (MSB) Pin 9 TP20	B Pin 10 TP19	A (LSB) Pin 11 TP18	TR1	Pre-amp gain
0	0	0	on	×1
0	0	1	on	×1
0	1	0	on	×1
0	1	1	off	×1000
1	0	0	off	×1000
1	0	1	off	×1000
1	1	0	off	×1000
1	1	1	off	×1000

Power supply for the CD4051 is: V_{DD} = +7V5 (pin 16), V_{SS} = 0V (pin 8) and V_{EE} = -7V5 (pin 7).

For details on the (opto-coupled) interface see section 5.2.12.

5.2.11 Power supply and other controls via connectors JA1 and JA2

In addition to the MDAC data and control lines (see section 5.2.6) the main power supply (±15V), input, output and filter controls enter via connector JA2: -

	Main PSU (From dist. PCB)			Main PSU (To pre-amp)			Pre-amp overload		Gain bus			Signal	
Function	+15V	0V	-15V	+15V	0V	-15V	LED		C	B	A	In	Out
JA2 pin	31a,c	32a,c	30a,c	4a,c	3a,c	5a,c	11a	11c	19c	19a	21c	2a	14c

The frequency select line enters via JA1. The MDAC controls are repeated here for convenience: -

IC Pin	4	5	6	7	8	9	10	11	Frequency select
Function	D3 (MSB)	D2	D1	D0 (LSB)	Chip select Active low	Write Active low	A0	A1	0 (75Hz) or 1 (25Hz)
JA1 pin	27a	25c	25a	23c	13a	5a	3c	3a	17a

5.2.12 Interface circuits

The pre-amp source impedance control signals are produced by the microcontroller module (slot 2 of the card frame, connectors JM1 and JM2) and reach the pre-amp module via the interface PCB (slot 3, connectors JI1 and JI2). See fig. 5.2.12.4.

The signals are opto-isolated with the main 5V (A) supply for the non-inverting buffers (SN7407) on the microcontroller side and a lower rated 5V (B) supply for the inverting buffers (SN7406) and opto-coupler pull-up resistors on the analogue side.

The 12V supply appears to be only for the diodes to limit spikes when the current is switched off for the (inductive) relay coils.

The main 5V (A) supply arrives at the card frame, as a pair, via power distribution PCB connector JT1 and enters the interface PCB via JI1. The 12V and 5V (B) supplies, on the other hand, arrive as two pairs via JT5 of the power distribution PCB and enter the interface PCB via JI2: -

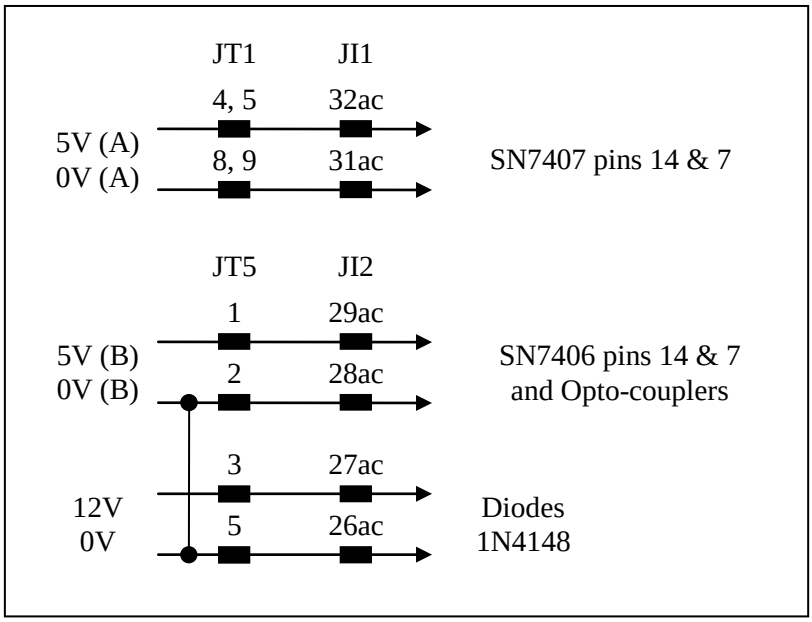

Fig. 5.2.12.1 Power supply routes

It is not clear if the 0V for the 5V (B) supply and 12V supply are connected together within the interface PCB. They are certainly connected together within the power distribution PCB.

There is no provision for go/return paths for the relay currents!

The inputs of the four unused buffers of IC16 (SN7406, pins 5, 9, 11 & 13) are pulled up to 5V (B) by *R16* (1k0).

The interface circuit for frequency select (25Hz/75Hz) requires a locally derived ±7V5 supply: -

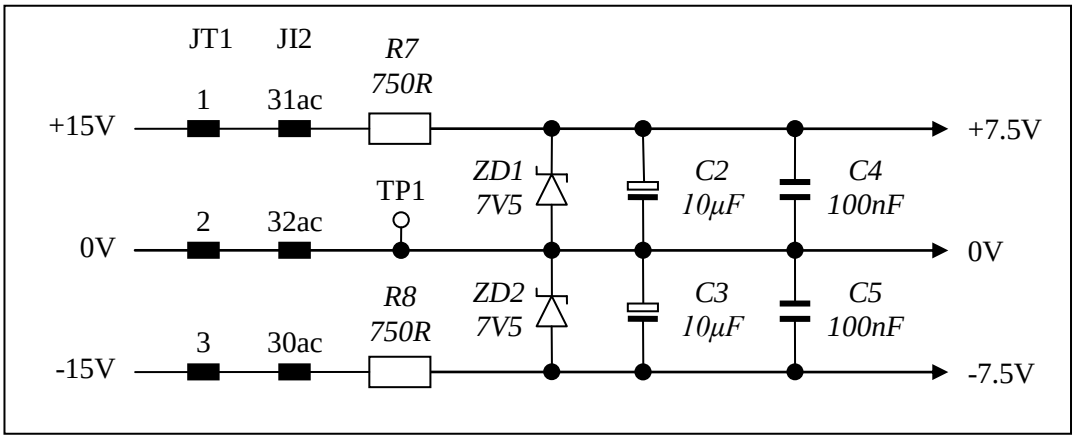

Fig. 5.2.12.2 Locally derived ±7V5 supply

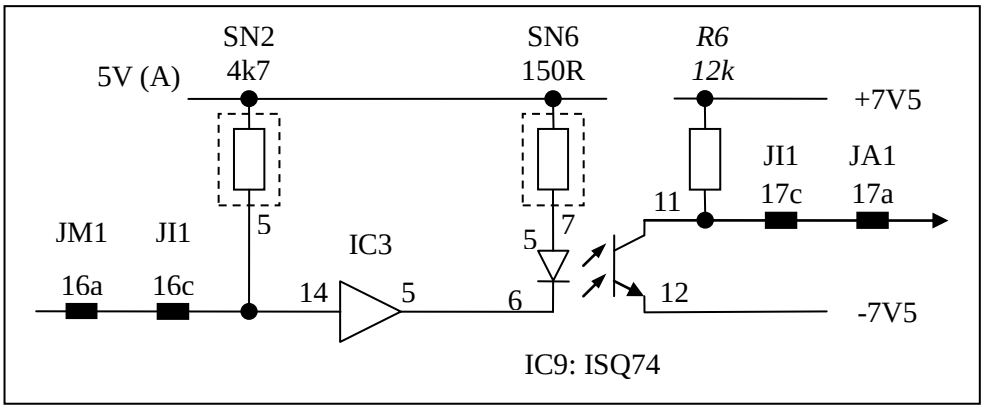

Fig. 5.2.12.3 Frequency select interface

N.B. The frequency select control line also goes to the carrier generator PCB (slot 4) via connector JC1 17a.

It would seem that the original reference for the quad opto-coupler is RS 307-064 (RS components).

Pin 1 is the common (5V) connection of the resistor networks (SN1, SN2 etc.)

The gain select control lines are also opto-coupled but with 0V and +7V5 output logic levels. See fig. 5.2.9.5.

The truth table is repeated here for convenience: -

C (MSB)	B	A (LSB)	Total gain (relative)
0	0	0	×1
0	0	1	×10
0	1	0	$\times 10^2$
0	1	1	$\times 10^3$
1	0	0	$\times 10^4$
1	0	1	$\times 10^5$
1	1	0	$\times 10^6$
1	1	1	$\times 10^7$

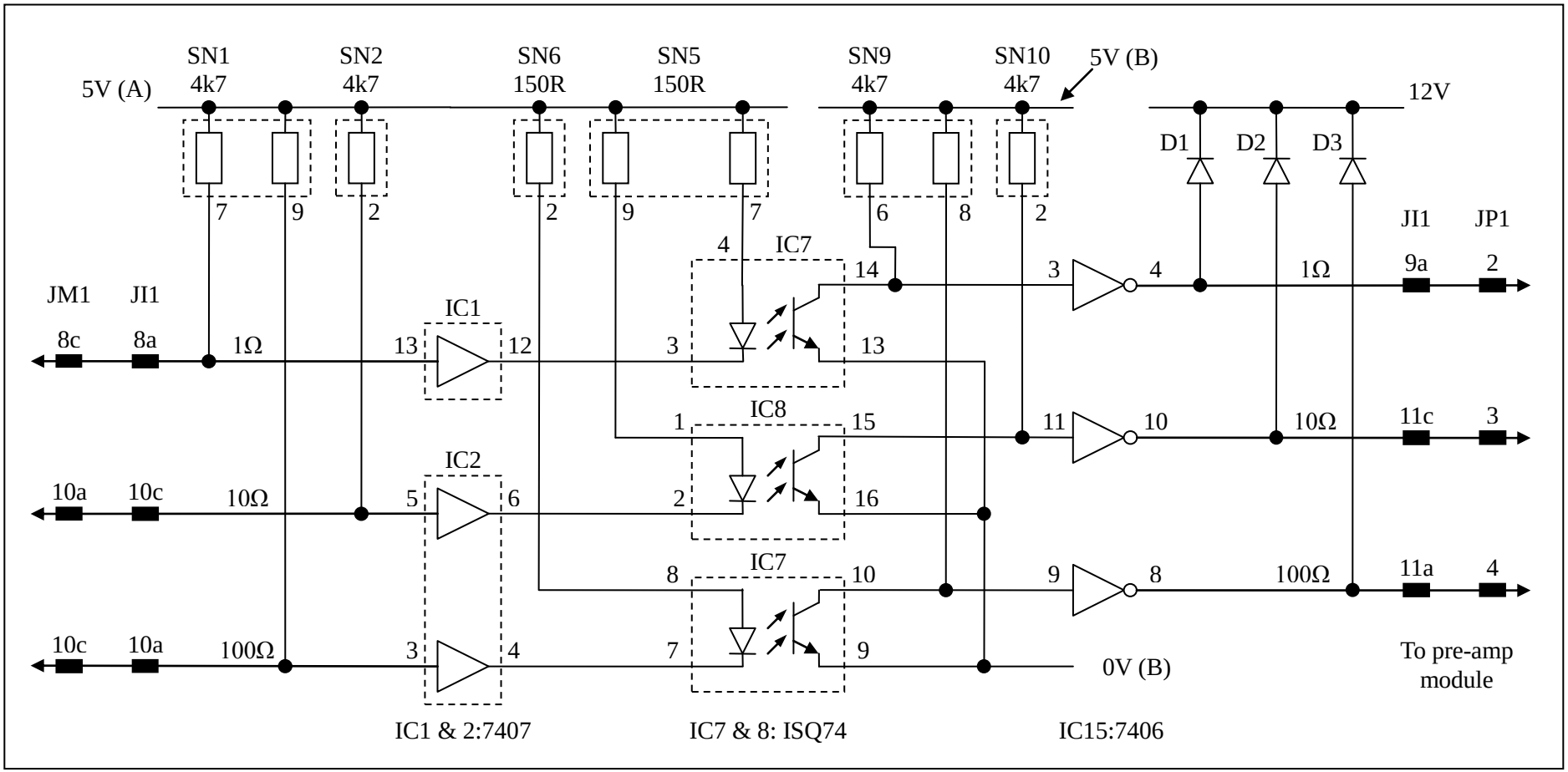

Fig. 5.2.12.4 Source impedance (relay) control interface

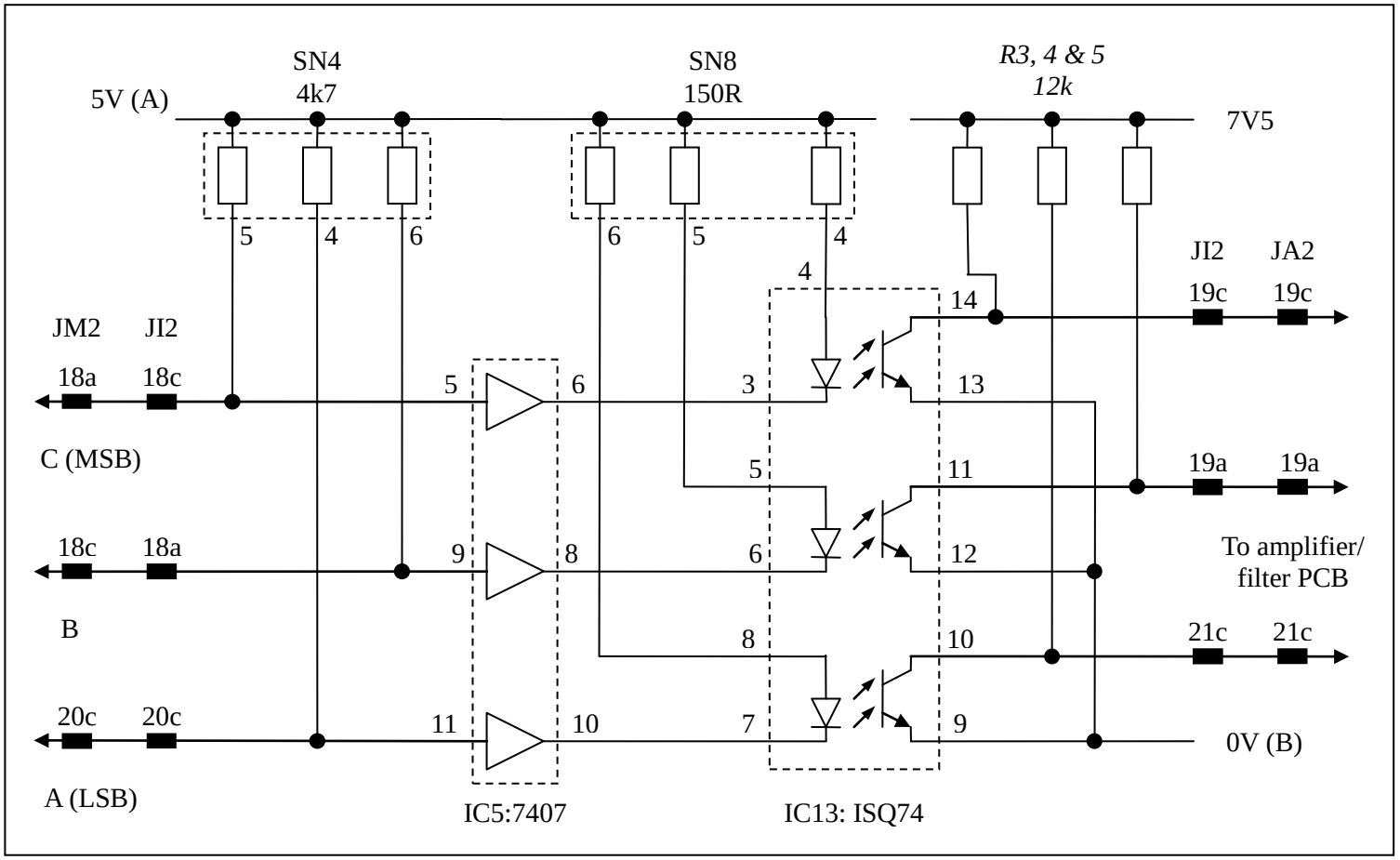

Fig. 5.2.12.5 Gain select interface

The pre-amp overload detector (see section 5.2.9) interface is as follows: -

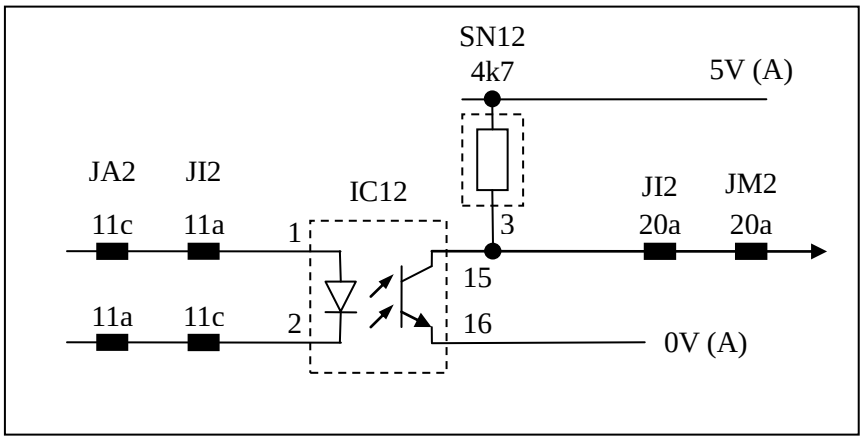

Fig 5.2.12.6 Pre-amp overload detector interface

There appears to be no resistor in series with the photodiode.

Similarly for the “carrier” (guard amplifier output) overload interface: -

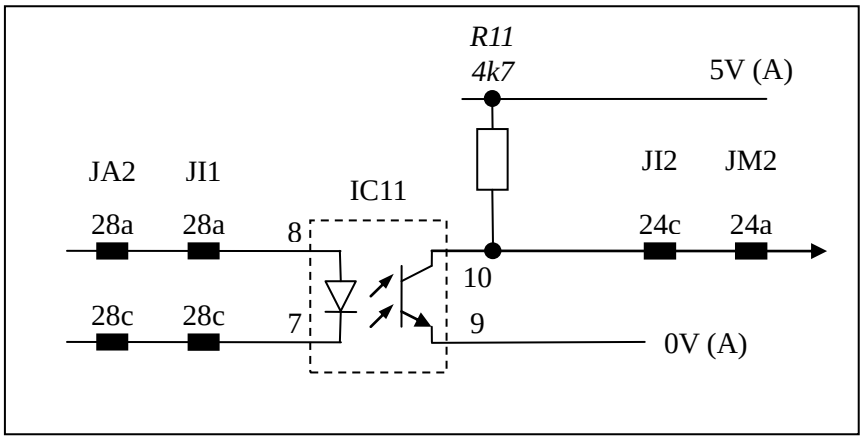

Fig. 5.2.12.7 Carrier overload detector interface

The control lines can also be traced to the input/output ports on the microcontroller PCB (slot 2).

The pre-amp noise matching control lines originate from IC8 (8255) port B: -

Control	Port	Pin	JM1	JI1 (input)	JI1 (output)	JP1 (input)
1Ω	B5	23	8c	8a	9a	2
10Ω	B6	24	10a	10c	11c	3
100Ω	B7	25	10c	10a	11a	4

The frequency select line originate from IC8 (8255) port C: -

Control	Port	Pin	JM2	JI1 (input)	JI1 (output)	JA1 (input)
Freq	C2	16	16a	16c	17c	17a

The gain select lines originate from IC9 (8255) portC: -

Control	Port	Pin	JM2	JI2 (input)	JI2 (output)	JA1 (input)
C (MSB)	C5	12	18a	18c	19c	19c
B	C4	13	18c	18a	19a	19a
A (LSB)	C3	17	20c	20c	21c	21c

The pre-amp and carrier overload signals arrive at IC9 (8255) port B: -

Overload	JA1 (output)	JI2 (input)	JI2 (output)	JM2 (input)	Port	Pin
Pre-amp	11c &11a	11a &11c	20a	20a	B6	24
Carrier	28a & 28c	28a &28c	24c	24a	B4	22