6. Ratio transformer, MDAC, negative and simulated capacitors

6.1 Introduction

The major advance of the F18 design, compared to the F17 [1], was to eliminate the noise contribution of the followers by connecting the primary ratio winding directly across the reference resistor. This requires even higher input impedance as the reference resistance could be up to 100Ω.

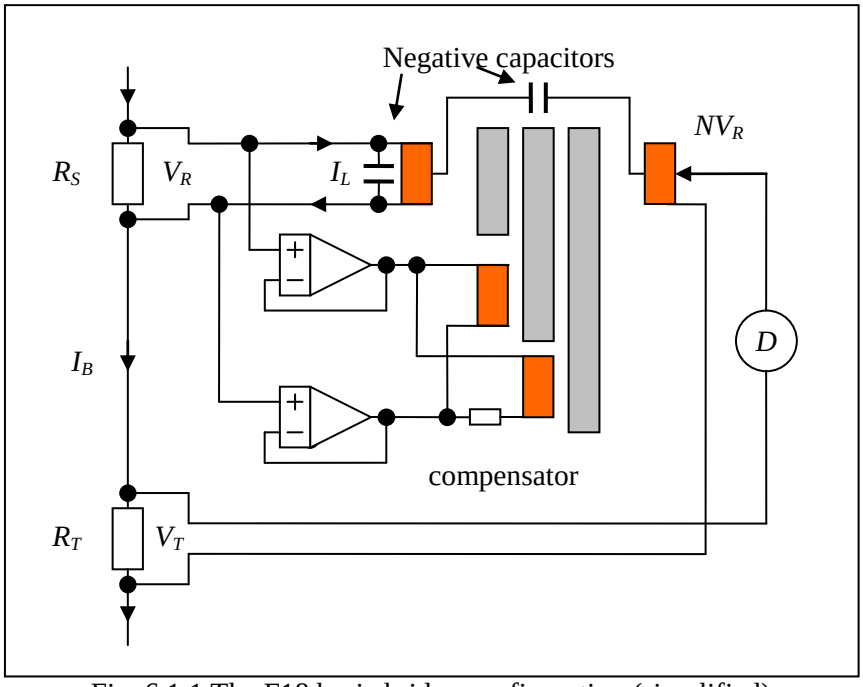


Fig. 6.1.1 The F18 basic bridge configuration (simplified)

This approach results in positive feedback and possible instability depending on the source resistance [2]. Stability was restored by adding extra resistance in series with the first energising winding. Unfortunately this would reduce accuracy significantly (or increase the minimum operating frequency). JDY found an elegant and ingenious solution – a large capacitor in parallel with the extra resistance [2, 3]. At low frequency (where the instability occurs) the capacitor has little effect and the resistance dominates, maintaining stability. At the operating frequency the impedance of the capacitor is much reduced and the bootstrapping effect is largely restored.

The target input impedance was >10GΩ (the real part). The main limitation, it was found, was the inter-winding capacitances. It was found necessary to use PTFE insulated wire and a pair of negative capacitors [4] to neutralise the inter-winding capacitance plus a final manual adjustment - the "Wolfendale tweek". This was "not elegant" according to JDY but we were in a hurry to get it into production! He was also unhappy with the "ratio tweek" – a final ratio adjustment.

The follower current noise flows through the source resistance and the voltage generated appears across the ratio primary. Best performance is achieved, therefore, when the noise resistance of the followers is significantly greater than the source resistance. A noise resistance of 1 to 3kΩ was found to be a good compromise.

For more detail see [5].

1. Part 3, monograph 6: "An F17 type ratio transformer bridge".
2. Part 3, monograph 4: "Three-stage ratio transformers".
3. Part 6, monograph 1: "A simulated large capacitor circuit".
4. Part 6, monograph 2: "A simulated negative capacitor circuit".
5. Part 3, monograph 7: "An F18 type ratio transformer bridge".

6.2 The divider

The divider consists of two three-stage ratio transformers [1] for decades 1 to 4 and a multiplying digital to analogue converter for decades 5, 6 and 7. Fig. 6.2.1 depicts the structure of the transformer with the usual convention – a winding that is horizontally adjacent to a toroidal core has windings around that core [2].

6.2.1 The ratio transformer (decades 1 to 4)

The first "decade" actually consists of two digits (range 0.0 to 1.2) representing 13 taps of a ratio winding, each with a glass-encapsulated reed, relay coil and catching diode, driven by a BCD to decimal decoder driver (SN7445) and 4 bit register (SN74LS175): -

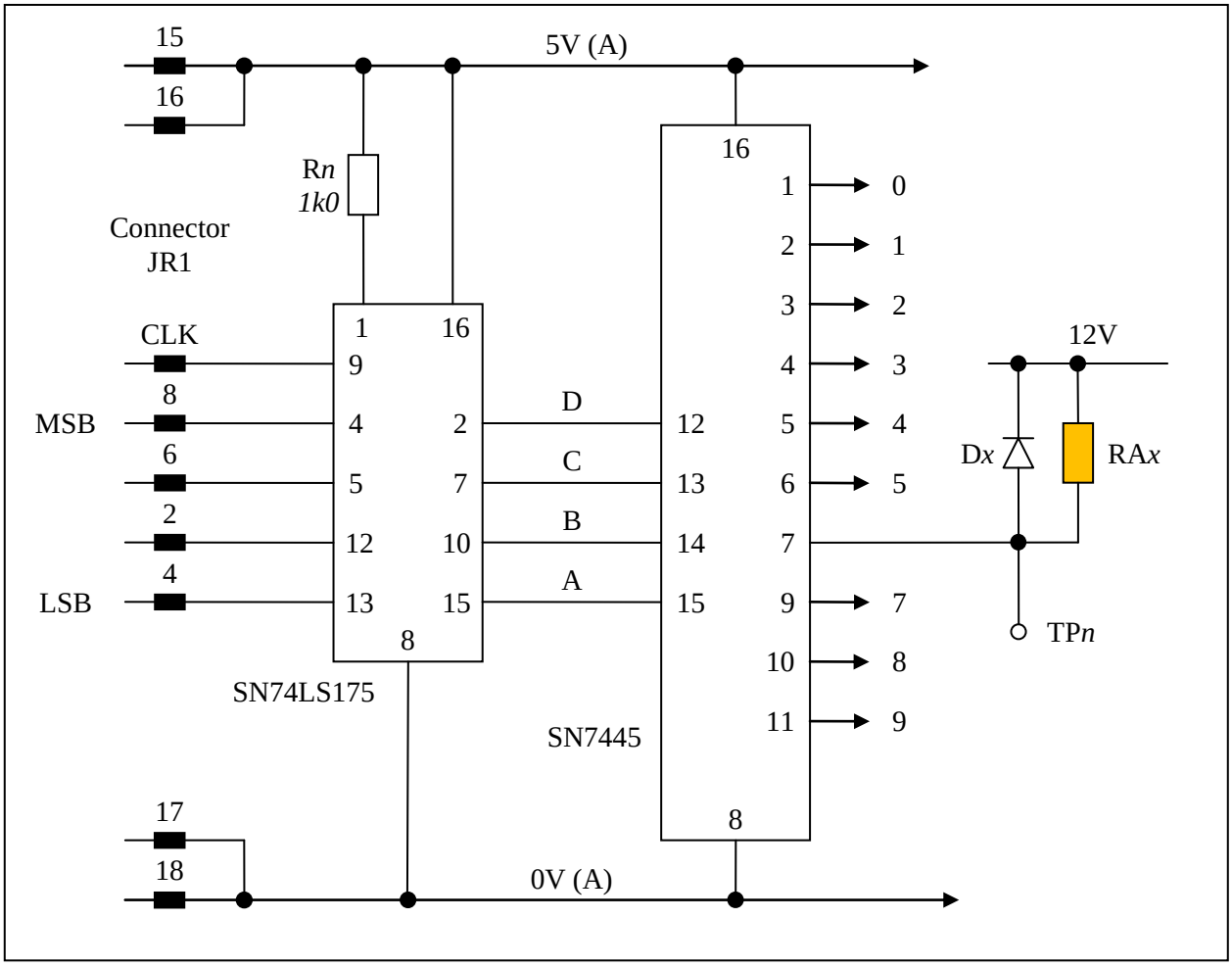


Fig. 6.2.1.1 Relay coil decoder/driver circuit

Decade	1	2	3	4
Register	IC3 &IC4	IC7	IC8	IC10
Decoder/driver	IC1 & IC2	IC5	IC6	IC9
Relay coils	RA1 to RA13	RA14 to RA23	RA24 to RA33	RA34 to RA43
Diodes	D1 to D13	D14 to D23	D24 to D33	D34 to D43
Test point	TP1 to TP13	TP14 to TP23	TP24 to TP33	TP34 to TP43
CLK control (JR1)	Pins 13 & 14	12	11	10
Pull-up resistor	R1	R2	R2	R3

For more detail on the interface see section 6.4.

1. Part 3, monograph 4: "Three-stage RTs".
2. Part 3, monograph 1: "Inductive voltage dividers and ratio transformers – the basics".

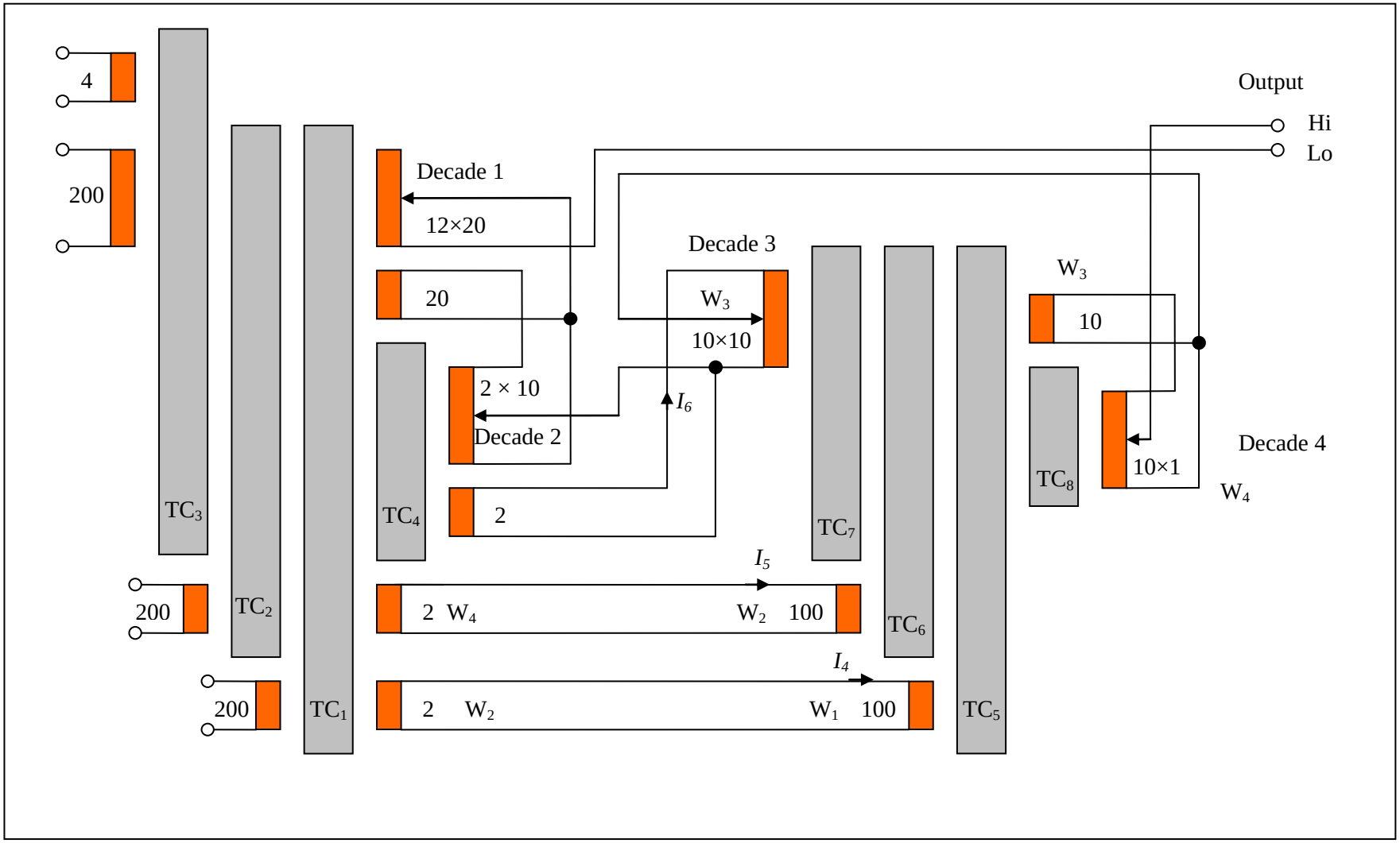


Fig. 6.2.1 Decades 1 to 4 (outline design)

6.2.2 MDAC (decades 5 to 7)

There are two versions of this circuit. See figs. 6.2.2.3 and 6.2.2.4. Both employ two-stage transformers at the input and output. The input to the MDAC is taken from the followers via a two-stage transformer with active drive from the output side [1]. The main windings consist of 200 turns (BNNL [2]). An extra 2 turns provides the reference voltage for the ratio tweek. Note the hierarchy of 0V star points: -

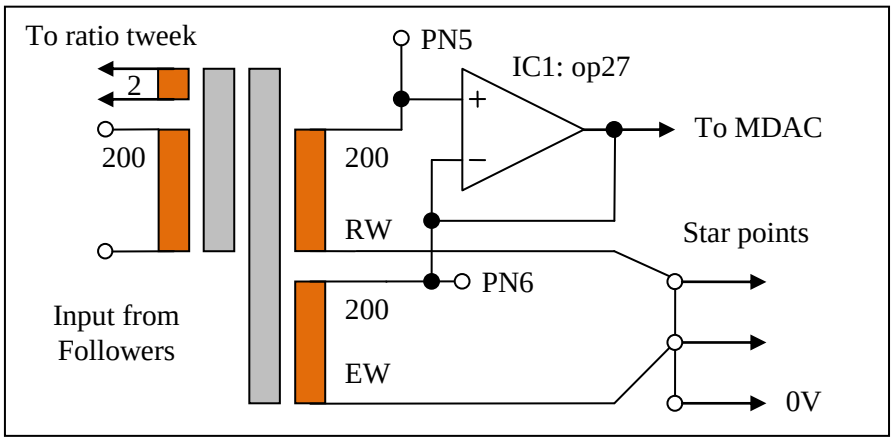


Fig. 6.2.2.1 MDAC input stage

The output of the MDAC is then stepped down with two more two-stage transformers, each reducing the output by precisely 100:1.

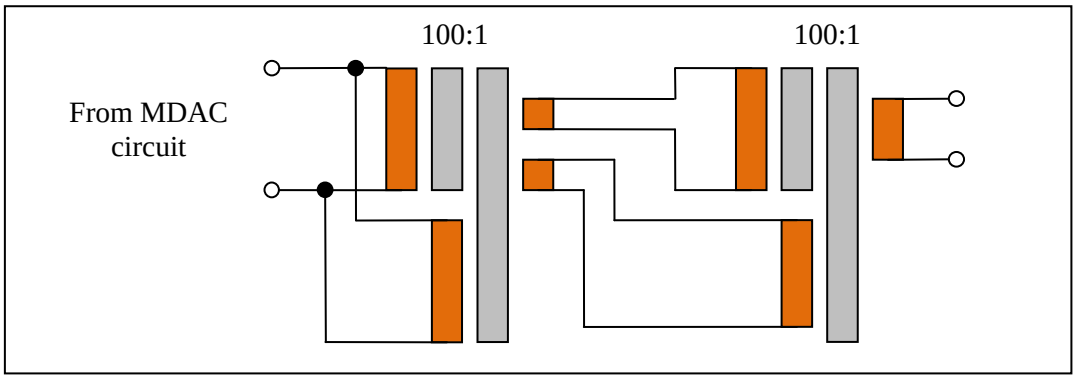


Fig. 6.2.2.2 Step-down stage

The reduced output is added in series with the output of the ratio transformer (decades 1 – 4).

1. Part 3, monograph 3: “Two-stage IVDs and RTs”.
2. Part 3, monograph 1: “Inductive voltage dividers and ratio transformers – the basics”.

The earliest version of the MDAC PCB module (Nov 1983) employs AC coupling to block the DC component of the MDAC output with a low DC offset op-amp to drive the (low resistance) primary windings of the first step-down transformer: -

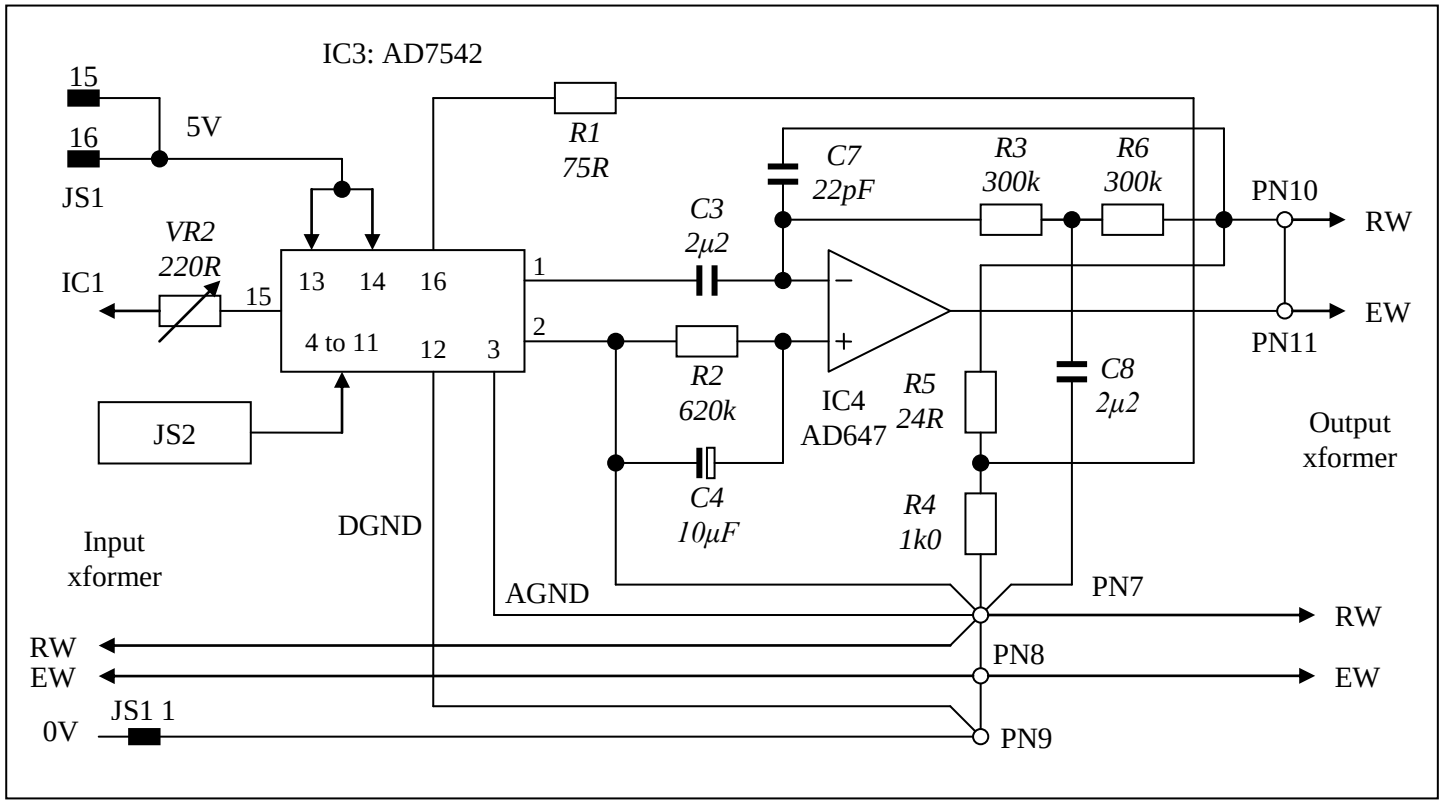


Fig. 6.2.2.3 MDAC circuit module (early version)

Note the order of connections to the energising and ratio windings (EW and RW). The energising windings carry most of the current.

The offset trimmer for IC4 (not shown) is *VR3*.

For more detail on the MDAC interface see section 6.4.

A later version of the MDAC PCB module (July 1984) employs a three-stage high-pass filter (a JDY special [1]) to block DC followed by a low DC offset op-amp to drive the primary windings of the first step-down transformer: -

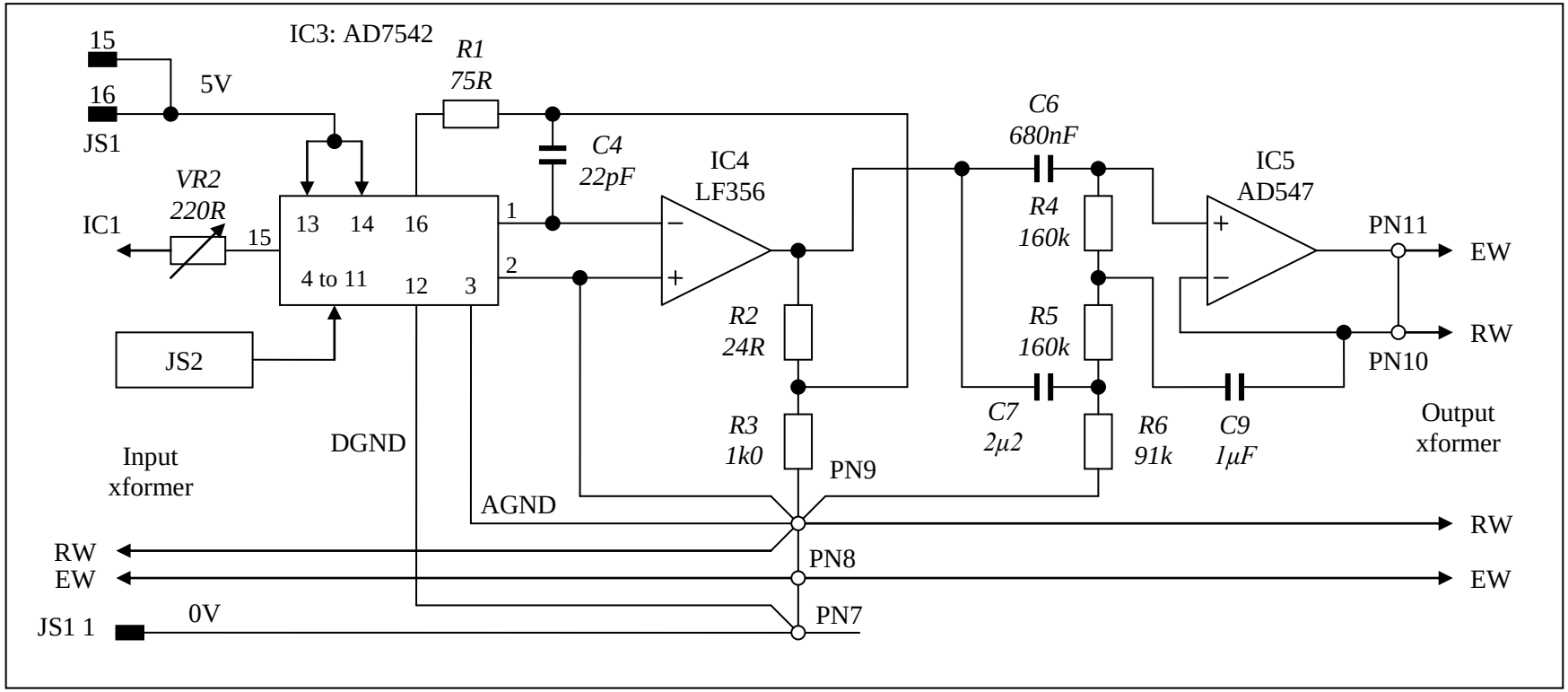


Fig. 6.2.2.4 MDAC circuit module (later version)

Note the order of connections to the energising and ratio windings (EW and RW). The energising windings carry most of the current.

The offset trimmer for IC5 (not shown) is *VR3*.

For more detail on the MDAC interface see section 6.4.

1. Part 2, monograph 2: “Three-stage filters”. See section 2.

Data, address and control lines come from the microcontroller PCB (slot 2 of the card frame) via the interface PCB (slot 3) and connector JS2. Both versions of the MDAC PCB also include an address decoder (IC2: 74LS138): -

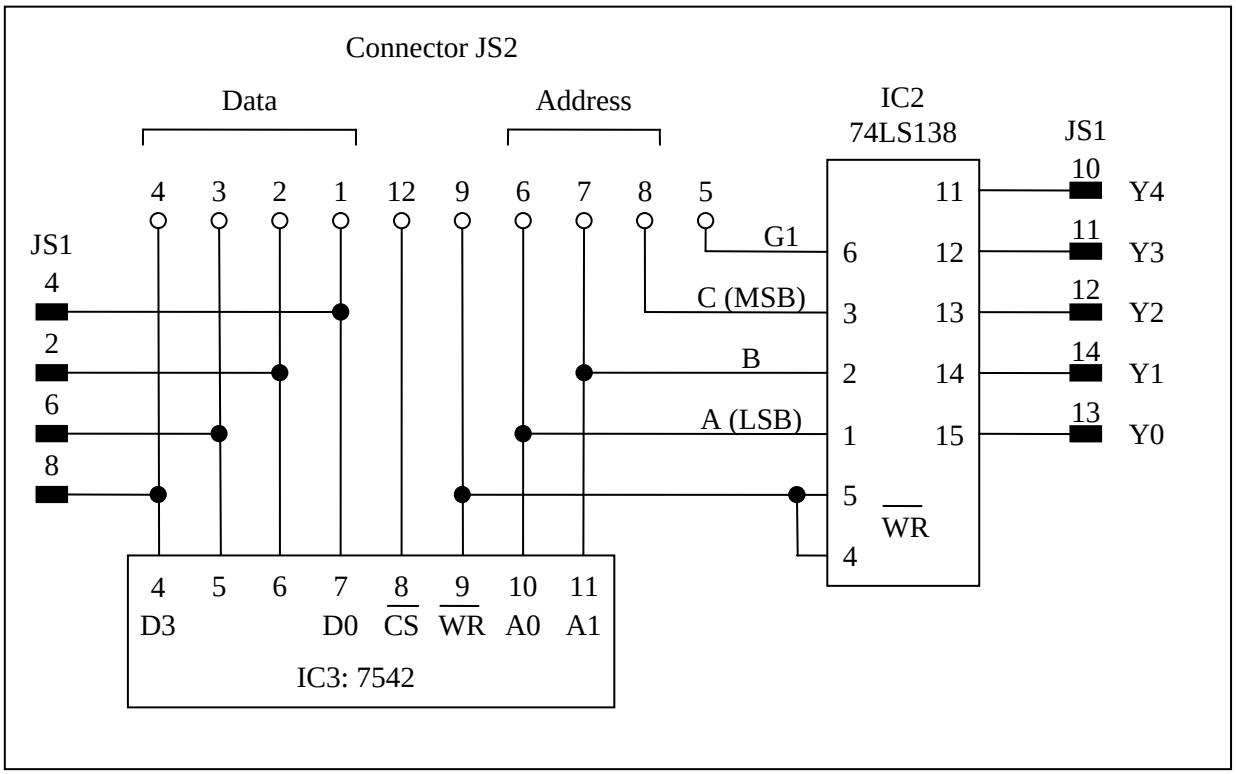


Fig. 6.2.2.5 MDAC interface and address decoder

For details of the (opto-coupled) interface see section 6.4.

The MDAC protocol requires valid data, address and chip select (0) before the write pulse (active low): -

A1	A0	CS	WR	CLR	Operation
x	x	x	x	0	Reset
x	x	1	x	1	Not selected
0	0	0	0	1	Load low 4 bits
0	1	0	0	1	Load middle 4 bits
1	0	0	0	1	Load high 4 bits
1	1	0	0	1	Load 12 bits

The write pulse is level triggered (i.e. data is latched on the rising edge). The reset pin is hard wired to 5V.

Which control line is used to select the MDAC? Addresses 000, 001, 010 and 011 are used by both the MDAC and the decoder chip so it can't be the bridge ratio channel selector. The outputs of the decoder (Y0 to Y5) are used as write pulses (active low) for 4-bit latches, probably in the same order as digits 1 to 5. See fig. 6.2.1.1.

The decoder control G1 is active high and is probably connected to the bridge ratio channel selector. See fig. 6.4.4.

The power supplies enter (and exit?) via connectors JS1, JS3 and JS4: -

JS1						JS3			JS4			
15	16	17	18	19	20	1	3	4	1	3	4	5
5V	5V	0V	0V	12V	12V	0V	-15V	+15V	0V	5V	0V	12V

ASL F18 circuits

Also on the MDAC PCB module is a pair of relay coils – a single and a double reed for a DPDT switch, for the unity ratio check, and a SPDT switch for the zero ratio check: -

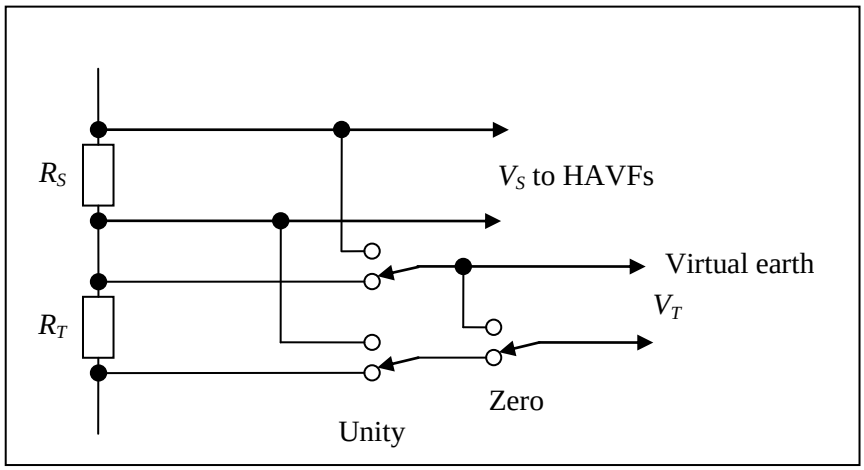


Fig. 6.2.2.6 Zero and unity ratio check relays

Each relay coil has a screen which is connected to 0V.

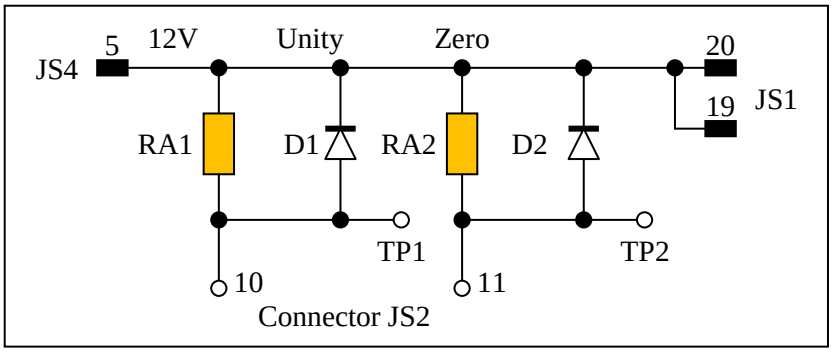


Fig. 6.2.2.7 relay coil connections

For more detail on the relay interface see section 6.4.

The connections to the reeds are hard wired to PTFE insulated pins: -

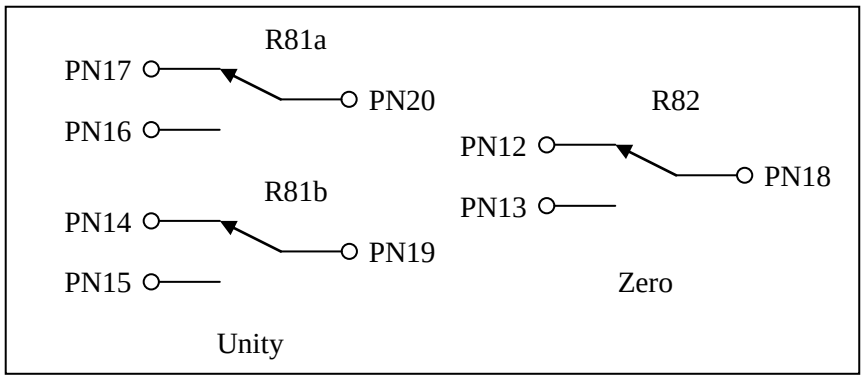


Fig. 6.2.2.8 Relay pin allocation

6.3 Negative and simulated large capacitors

Part of the divider system but on a separate PCB module is a pair of negative capacitors [1] and a simulated large capacitor [2]. The negative capacitors employ positive feedback with a real (polystyrene) capacitor and an LCR low-pass filter with two-stage response within the loop (for stability) [3]: -

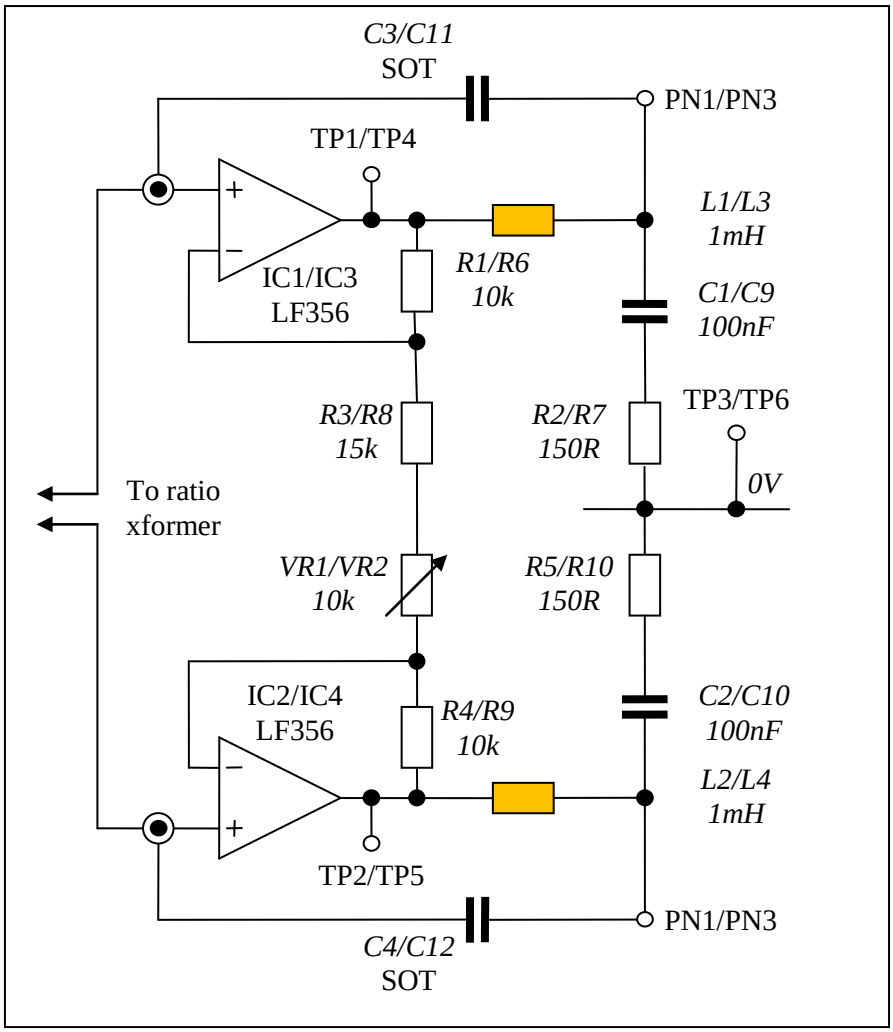


Fig. 6.3.1 Negative capacitors

1. Part 6, monograph 2: “A simulated negative capacitor circuit”.
2. Part 6, monograph 1: “A simulated large capacitor circuit”.
3. Part 2, monograph 1: “Two-stage filters”. See section 6.

The simulated large capacitor, equivalent to 22,000µF, is equally ingenious: -

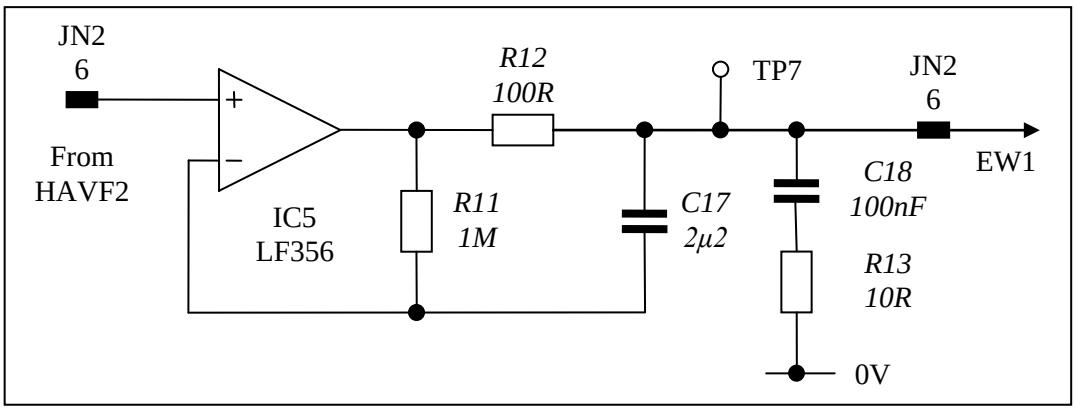


Fig. 6.3.2 Simulated large capacitor

The offset trimmer for IC5 (not shown) is *VR3*.

Strictly speaking the equivalent circuit is a large capacitor in parallel with R_{12}. Viz: -

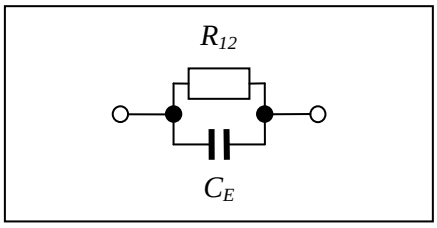


Fig. 6.3.3 Equivalent circuit

Where the equivalent capacitance is: $$C_E = \left(1 + \frac{R_{11}}{R_{12}}\right) C_{17}$$

This PCB module also includes the "Wolfendale" input impedance tweek circuit: -

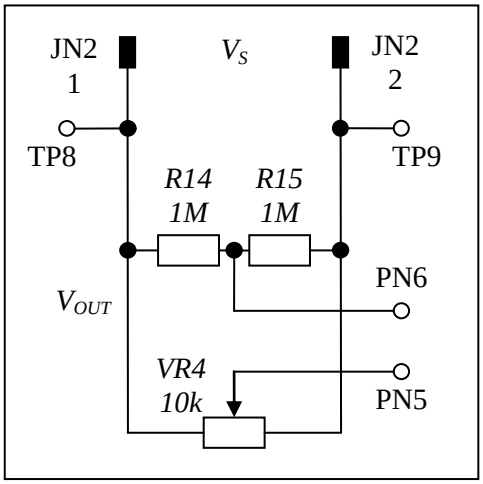
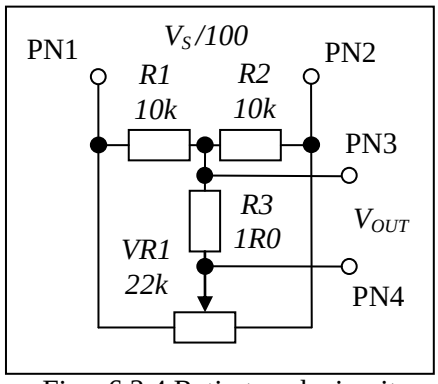


Fig. 6.3.4 The Wolfendale tweek

The two connectors are JN1 and JN2: -

JN1			JN2									
1	2	3	1	2	3	4	5	6	7	8	9	10
+15V	0V	-15V	HAVF1	HAVF2			C_E OUT	C_E IN		+15V	0V	-15V

This PCB module also includes the ratio tweek circuit: -



Figs. 6.3.4 Ratio tweek circuit

The ratio tweek takes its (isolated) input from a secondary of a two-stage transformer (see fig. 2.2.1). It is accurately one hundredth (10^{-2}) of the reference voltage. The output is added in series with the ratio winding primary with a further attenuation in the range $\pm 10^{-4}$. The total range of slope adjustment is, therefore, ±1ppm.

The control is non-linear. If one assumes that the trimmer can be set with a resolution of 1% the 1:1 ratio can set to within ±5ppb (at the centre) and ±30ppb (at either end).

6.4 Interface circuits

See 6_part 2.