7. Adjustments and final checks

7.1 Basic checks (normal configuration)

Before embarking on final checks and adjustments please consult the user manual and section 1 (Introduction and overview). Useful clues can be gleaned, regarding any malfunction or anomalies, using the normal configuration.

Connect two fixed resistors for R_S and R_T, preferably of the same high stability (low temperature coefficient) types and value (100Ω). A decade resistance box is desirable for variable R_S or R_T.

The connections should be of the two-terminal pair types [1] (sometimes referred to as "four wire" resistors). The resistance of the connecting wires is made irrelevant with separate current carrying and voltage sensing pairs. Viz: -

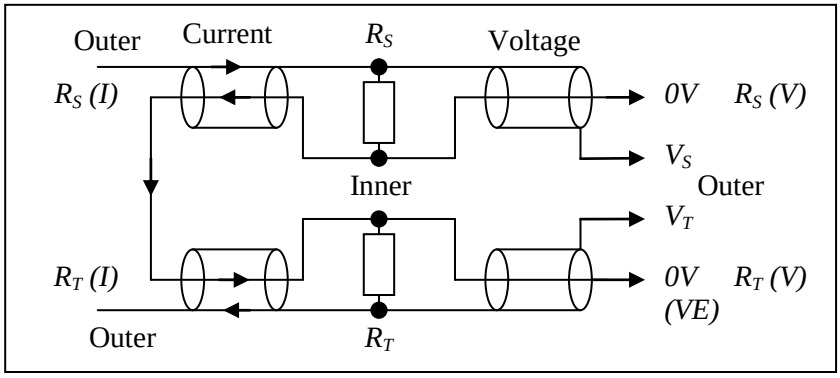

Fig. 7.1.1 Configuration for basic checks

R_S *(I)* refers to the current carrying coax cable for the standard resistor; R_T *(V)* to the voltage sensing cable for the unkown resistor (thermometer) etc.

Set the controls as follows (buttons from left to right): -

Source R.	In-phase gain		Quad gain	Carrier	Freq.	Check	Meter	Bandwidth	Mode	Rotary switches
	Buttons	Pot								
100Ω	$\times 10^4$	5.00	×10	1mA	High	Normal	Normal	0.5Hz	Manual	1.0000000

The voltages V_S and V_T are then easily checked with an oscilloscope (100mV RMS at 75Hz) on the outer conductors [2] of the coax cables (see fig. 1.2.1). The earth terminal on the front panel is a convenient 0V reference point. V_T should be the inverse of V_S (180deg phase shift).

Check the inner conductors for virtual earth (*VE* = 0V±1mV).

Try a variety of current settings and values of R_S to check that the bridge constant current source and active guard is working, subject to maximum V_S of 700mV $\left(V_S = I_B R_S\right)$.

Try a manual null balance (using the rotary switches) while observing the out-of-balance on the meter and the DC output (rear panel SKT1). With 1mA bridge current, R_S = 100Ω, sensitivity fine control setting at 5 and coarse setting $\times 10^4$ the out-of balance should change by full scale on the meter and 10V DC for 10ppm change in ratio (third digit from the right). Try setting the gain to $\times 10^5$: full scale for 1ppm change in ratio.

Proceed to check that all the user controls are in accordance with the user manual and instrument specification.

1. Part 1, monograph 1: "High accuracy resistors". See section 3.
2. The terms "outer" and "inner" not only apply to the coax cables but also to the outer and inner parts of the bridge circuit. The inner part is sensitive to interference, hence the need for shielding.

7.2 External zero ratio check

A very accurate zero ratio check can be implemented by connecting the potential lead of R_T as a zero-Ohm junction [1]. This is the method employed by the F18 internally: -

Source Resistance	In-phase gain		Quad gain	Carrier	Freq.	Check	Meter	Bandwidth	Mode	Rotary switches
	Buttons	Pot								
100Ω	$\times 10^4$	5.00	×10	1mA	High	Normal	Normal	0.5Hz	Manual	0.0000000

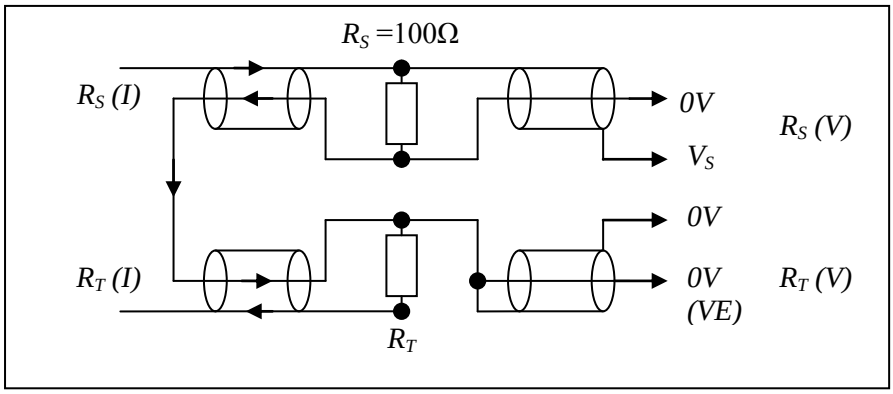

Fig. 7.2.1 Configuration for external zero check

The bridge should balance with ratio setting of precisely 0.0000000 (±0.1ppm). Increasing the ratio setting provides a suitable test signal for the null detector circuitry.

7.3 External unity ratio check

A very accurate unity check can be implemented by connecting the potential lead of R_T to R_S. This is the method employed by the F18 internally: -

Source Resistance	In-phase gain		Quad gain	Carrier	Freq.	Check	Meter	Bandwidth	Mode	Rotary switches
	Buttons	Pot								
100Ω	$\times 10^4$	5.00	×10	1mA	High	Normal	Normal	0.5Hz	Manual	1.0000000

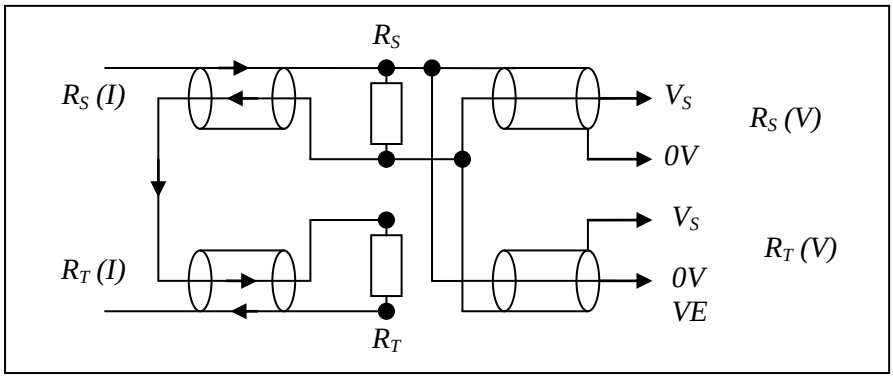

Fig. 7.3.1 Configuration for external unity check

Note that the virtual earth moves to the outer conductors of the reference resistor.

The bridge should balance at a ratio of precisely 1.0000000 (±0.1ppm).

N.B. This is the ideal configuration for adjusting the ratio tweek and lower decade scaling. See section 7.6.8.

1. Part 1, monograph 1: “High accuracy resistors”. See section 3.4.

7.4 External signal generator configuration

It is possible to "troubleshoot" for more subtle faults with a test signal from an external signal generator (sig. gen.). One terminal of the signal generator must be local 0V (earth).

With many signal generators it is a simple case of using a BNC to BNC cable (to the R_S *(V)* input).
The current carrying coax cables are connected as normal but the R_T (V) inner and outer are both connected to R_T (I) inner (the virtual earth point): -

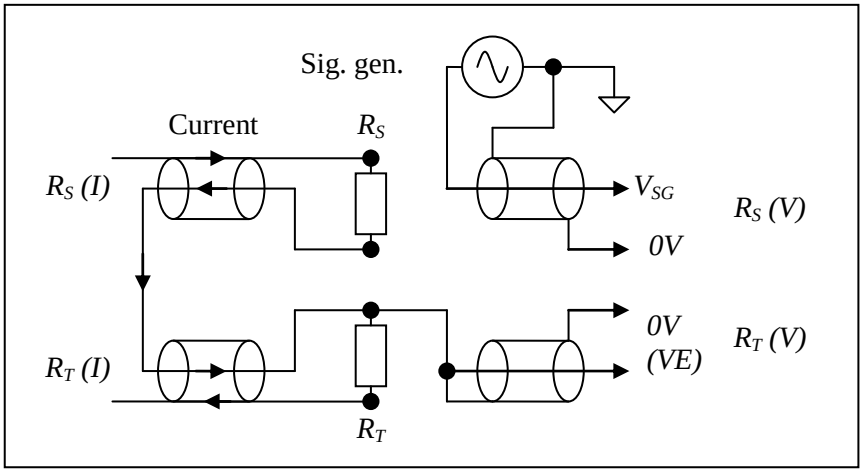

Fig. 7.4.1 Configuration for external sig. gen. tests

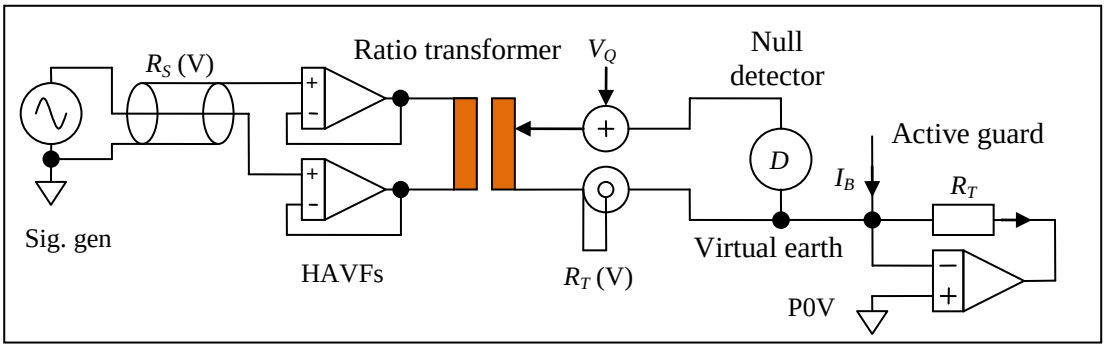

Fig. 7.4.2 Equivalent circuit

Use a 1kHz square wave (100mV pk-pk) to test the dynamic response of the followers (a very characteristic overshoot and a peak in the frequency response).

To test the frequency response of the null detector filters select a sinewave of 100mV pk-pk. Check the signal across *R19* (proportional to the current through the ratio transformer primary [1]) to make sure that the sig. gen is not producing a DC component.

Increase the manual ratio setting from zero to provide a test signal for the null detector circuitry. The output of the filter and amplifier stages (amplitude and phase shift) will vary with frequency: notches at 50Hz and 150Hz and a band-pass (zero phase shift) at 25Hz or 75Hz.

The quadrature servo should not be a problem but, if in doubt, simply unplug the quad servo analogue multiplier (IC10) [2].

1. Section 4: "High accuracy voltage followers". See fig 4.1.
2. Section 5: "Part 2_Null detector PCB2". See section 5.3.3.

7.5 Zero V_S and V_T checks

This test configuration is particularly useful for adjusting the DC offset trimmers – both V_S and V_T are connected to the virtual earth: -

Source Resistance	In-phase gain		Quad gain	Carrier	Freq.	Check	Meter	Bandwidth	Mode	Rotary switches
	Buttons	Pot								
100Ω	$\times 10^4$	5.00	×10	1mA	High	Normal	Normal	0.5Hz	Manual	0.0000000

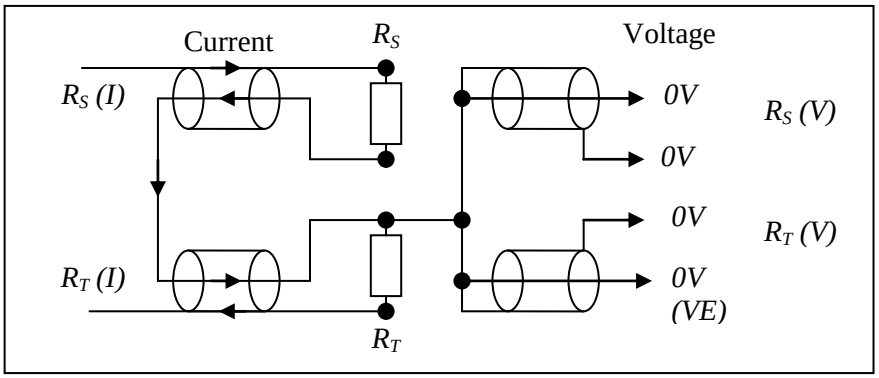

Fig. 7.5.1 Zero V_S and V_T configuration

The virtual earth can be considered the 0V AC reference point for the bridge (0V±10nV at 75Hz relative to the primary 0V reference point (P0V) – the non-inverting input of the guard amp. See fig. 7.6.1.1). Unfortunately it is not possible to connect this to earth (e.g. via a 'scope probe). The best location for a 'scope probe earth is usually a wire connected to the earth terminal on the front panel. For critical 0V DC adjustments (virtual earth and voltage followers) a more local 0V reference point is recommended.

7.6 Adjustments

The recommended order for adjustment and final checks is as follows: -

	Section	Description
1	7.6.1	V to I and guard amplifier PCB
2	7.6.2	Carrier generator PCB (slot 4).
3	7.6.3	High accuracy voltage follower PCB.
4	7.6.4	Pre-amplifier module.
5	7.6.5	Amplifier and filter PCB (slot 6) DC offsets
6	7.6.6	Amplifier and filter PCB tuning.
7	7.6.7	Null detector PCB2 (slot 5)
8	7.6.8	MDAC module
9	7.6.9	Negative and simulated capacitors
10	7.7	Final checks

Rotate trimmers backward and forward a few times to establish a clean resistive surface and a fresh contact with the wiper. Observe the signal with an oscilloscope to ensure that the voltage changes smoothly. Persist but, if necessary, replace the trimmer if it remains "scratchy".

The following equipment is recommended: -
Dual channel oscilloscope (down to 5mV/div or better)
DMM (0.01% accuracy/0.1mV resolution) including AC RMS voltage and current.
A selection of probes and test cables for "hands free" testing and troubleshooting
General purpose signal generator,
Double euro-card extender with compatible connectors (type?).
Good quality (temperature controlled) soldering iron and a selection of tips
Hand tools: snipe nose pliers, side cutters, wire strippers, solder sucker, magnifying glass, trimmer tool, selection of screwdriver types.

A differential amplifier with variable bandwidth may prove to be useful – observe voltages without creating an earth loop.

The F series bridges have been criticised for the large number of trimpots. These are mostly to correct for the input offset voltage of the op-amps. John David Yewen (JDY), our analogue guru, justified this on the grounds that the LF356 is a very good op-amp (for the price - excellent AC, DC and low noise characteristics) and, unlike many other types, maintains a low DC offset over temperature especially with the offset trimmed.

It is fairly obvious, in most cases, which trimmer is for DC offset. For example, *VR1*: -

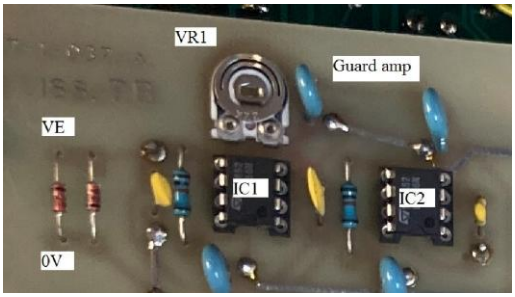

Fig. 7.6.1 The offset trimpot is usually nearest the chip

Picture from F18 preferable.

7.6.1 V to I and guard amplifier PCB.

These adjustments are best done in basic checks mode (section 7.1) with $R_S = R_T = 100\Omega$ and $I_B = 1\text{mA}$.

Pic required

Fig. 7.6.1.1 Guard amp on V to I and guard amp PCB

Set the bridge current to zero by connecting TP2 to TP3 and check the latter for 0V AC relative to pin3 of IC2. This is the output of the MDAC for fine amplitude control [1]. It is then possible to set the following DC levels: -

Adjust *VR2* for 0V ±1mV on TP4 (output of amplifier IC3).

Adjust *VR3* for 0V ±1mV on TP7 (output of V to I output stage IC3).

One of the most critical DC offsets is the virtual earth created by the guard amplifier. It is important that this is adjusted to 0V ±0.1mV relative to the primary 0V (P0V) reference point at the bottom of *R22*.

Virtual earth (VE): adjust *VR4* for 0V ±0.1mV at TP8 relative to 0V at the bottom of *R22* [2].

Check that the DC level at TP12 is also 0V ±0.1mV (output of guard amplifier).

Remove the link between TP2 and TP3 and check that the current is set to 1mA (RMS). If the reference resistor is precisely 100Ω the output TP7 should be precisely 100mV (RMS). Adjust VR1 (MDAC fine gain adjustment) to ensure that it is. You may wish to revisit this after adjusting the fine amplitude control in the next section.

1. Section 3: “Part 2_V to I and guard amp”. See fig. 3.7.1.
2. Ditto: See section 3.9.

7.6.2 Carrier generator PCB (slot 4 of the card frame)

This module consists of the phase-lock loops, filters and amplitude control with a number of (non-critical) DC offsets [1].

Adjustments are best done in basic checks mode (section 7.1) with $R_S = R_T = 100\Omega$ and $I_B = 1\text{mA}$.

pic required

Fig. 7.6.2.1 Carrier generator PCB

Remove IC3 from its socket (if supplied) and connect TP2 to 0V (pin 6 to pin 3 of the socket).

Adjust *VR2* for 0V ±1mV DC at TP3 (output of IC5: low-pass filter LPF1). See fig. 3.2.3.

Adjust *VR3* for 0V ±1mV DC at TP4 (output of IC7: low-pass filter LPF2). See fig. 3.2.3.

Adjust *VR4* for 0V ±1mV DC at TP5 (output IC9: of phase inverter stage). See fig. 3.3.1.

Adjust *VR5* for 0V ±1mV DC at TP6 (output of IC10: inverter stage). See fig. 3.3.1.

Adjust *VR6* for 0V ±1mV DC at TP7 (output of IC11: half wave rectifier). See fig. 3.4.1.

It is not clear why IC12 has an offset trimmer – its an integrator.

Unplug IC12 and connect TP9 to 0V (integrator output).

Adjust *VR10* for 0V ±1mV at TP10 (output of IC13: inverter stage). See fig. 3.2.2.

Adjust *VR12* for the threshold at TP17 (comparator output just changing state). See fig. 3.5.2.

Remove the 0V links and replace IC3 and IC12.

Adjust *VR11* for 50/50 duty cycle 50Hz square wave at TP11 (output of filter/comparator). See fig. 3.1.2.

Adjust *VR1* for a symmetrical square wave (equal positive and negative levels) at TP2.

Adjust *VR7* for precisely 8V pk-pk at the main output TP6. If necessary revisit the MDAC fine gain adjustment (section 7.6.1).

1. Section 3: “Part 1_Carrier generator”.

7.6.3 High accuracy voltage follower PCB.

These adjustments are best done in zero V_S and V_T configuration (section 7.5).

The current (AC and DC) flowing through the ratio transformer primaries can be monitored by connecting a scope probe directly across *R19*. Test point TP10 is local 0V and TP5 is the other end of *R19* [1].

pic required

Fig. 7.6.3.1 High accuracy voltage followers

Check that the inputs to both followers are 0V ±0.1mV relative to primary 0V.

Adjust *VR1* for 0V ±0.1mV at PN5 (output of HAVF1 and "0V" of its floating PSU) relative to TP10.

Adjust *VR2* for 0V ±0.1mV at PN10 (output of HAVF2 and "0V" of its floating PSU) relative to TP10.

Tweak *VR1* for a DC component across *R19* of 0V±1mV.

1.

7.6.4 Pre-amplifier PCB

This is best done with Zero V_S and V_T checks (section 7.5) and maximum gain (pre-amp gain is ×1000).

$$R_S = R_T = 100\Omega$$

Source Resistance	In-phase gain		Quad gain	Carrier	Freq.	Check	Meter	Bandwidth	Mode	Rotary switches
	Buttons	Pot								
100Ω	$\times 10^7$	5.00	×10	1mA	High	Normal	Normal	0.5Hz	Manual	0.0000000

pic required

Fig. 7.6.4.1 Pre-amp PCB

Adjust *VR1* for 0V ±100mV on pin 6 (output of pre-amp) relative to 0V on PN5. See fig. 5.1.3.

7.6.5 Amplifier and filter PCB (slot 6) DC offsets

This is also best done with Zero V_S and V_T checks (section 7.5) and maximum gain (pre-amp gain is ×1000).

$$R_S = R_T = 100\Omega$$

Source Resistance	In-phase gain		Quad gain	Carrier	Freq.	Check	Meter	Bandwidth	Mode	Rotary switches
	Buttons	Pot								
100Ω	$\times 10^7$	5.00	×10	1mA	Both*	Normal	Normal	0.5Hz	Manual	0.0000000

***Check that all the DC offsets remain low when the frequency of operation is switched to low.**

pic required

Fig. 7.6.5.1 Amplifier and filter PCB

Adjust *VR3* for 0V ±1mV on TP1 (output of BPF1) relative to 0V on the bottom of *R7*. See fig. 5.2.1.1.

Adjust *VR4* for 0V ±1mV on TP2 (output of SGS1) relative to 0V on the bottom of *R15*. See fig. 5.2.2.1.

Adjust *VR7* for 0V ±1mV on TP3 (output of BPF2) relative to 0V on the bottom of *R7*. See fig. 5.2.2.1.

Adjust *VR12* for 0V ±1mV on TP6 (output of summing junction/amplifier) relative to 0V on the bottom of R33. See fig. 5.2.4.3.

Adjust *VR17* for 0V ±1mV on TP9 (output of summing junction/amplifier) relative to 0V on the bottom of R*45*. See fig. 5.2.5.3.

Adjust *VR18* for 0V ±1mV on TP10 (output of SGS2) relative to 0V on the bottom of *R51*. See fig. 5.2.6.1.

Adjust *VR19* for 0V ±1mV on TP12 (output of MDAC) relative to 0V on the bottom of *R55*. See fig. 5.2.7.1.

Adjust *VR23* for 0V ±1mV on TP13 (output of BPF3) relative to 0V on the bottom of *R51*. See fig. 5.2.6.1.

7.6.6 Amplifier/filter tuning

This is best done with the external signal generator configuration (section 7.4).

Set the signal generator frequency to precisely 25, 50, 75 or 150Hz for tuning the band-pass filters as required.

Select the appropriate operating frequency ("High" is 75Hz and "Low" is 50Hz) and invert one 'scope channel to detect precisely 180 degrees phase shift as required.

Adjust the signal generator gain and/or the null detector gain to achieve a suitable signal level.

There is a small amount of interaction between the summing junction controls (not virtual earths) so the adjustments may need repeating to achieve a good null at 50Hz and 150Hz.

pic required

Fig. 7.6.6.1 Amplifier and filter PCB

Adjust *VR1* and *VR2* for zero phase shift at 25Hz and 75Hz respectively from input (sig. gen.) to TP1 (output of BPF1). See fig. 5.2.1.1.

Adjust *VR5* and *VR6* for zero phase shift at 25Hz and 75Hz respectively from TP2 to TP3 (input and output of BPF2). See fig. 5.2.2.1.

Adjust *VR8* for zero phase shift at 150Hz from TP3 to TP4 (input and output of a BPF). See Fig. 5.2.4.1.

Adjust *VR9* for zero phase shift at 50Hz from TP3 to TP5 (input and output of a BPF). See Fig. 5.2.4.1.

Adjust *VR10* and *VR11* for nulls at 150Hz and 50Hz respectively at TP6 (output of summing junction/amplifier). See fig. 5.2.4.1. Repeat the adjustments until a null is achieved for both frequencies.

Adjust *VR13* for zero phase shift at 150Hz from TP6 to TP7 (input and output of a BPF). See Fig. 5.2.5.1.

Adjust *VR9* for zero phase shift at 50Hz from TP3 to TP5 (input and output of a BPF). See Fig. 5.2.5.2.

Adjust *VR15* and *VR16* for nulls at 150Hz and 50Hz respectively at TP9 (output of summing junction/amplifier). See fig. 5.2.5.3. Repeat the adjustments until a null is achieved for both frequencies.

Adjust *VR21* and *VR22* for zero phase shift at 25Hz and 75Hz respectively from TP12 to TP13 (output of BPF3). See fig. 5.2.8.1.

Final tuning: -

The notch filters introduce a small phase shift (at 25Hz and 75Hz) so that it is necessary to retune all three band-pass filters for a total of zero phase shift from V_S to the final output. Return to basic checks configuration (section 7.1) and adjust each BPF to reduce the phase error by one third at TP13.

The final tweek is to ensure that the full wave rectified signal at the output of the in-phase synchronous rectifier is a precisely rectified sinewave: -

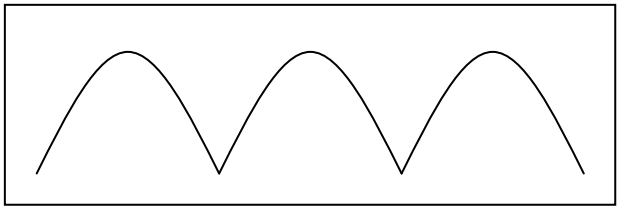

Fig. 7.6.6.2 precisely rectified sinewave

This is best done in internal (or external – section 7.3) unity ratio check mode: -

$$R_S = R_T = 100\Omega$$

Connect both resistors with the same length of cable - to minimise quadrature imbalance.

Source Resistance	In-phase gain		Quad gain	Carrier	Freq.	Check	Meter	Bandwidth	Mode	Rotary switches
	Buttons	Pot								
100Ω	various	5.00	×10	1mA	Both	Unity	Normal	0.5Hz	Manual	1.0000000

Try the full range of gain (starting with the minimum) and adjust the ratio to provide a suitable in-phase out-of-balance signal. At the highest gain setting you may have a problem with noise.

7.6.7 Null detector PCB2

These adjustments are best done in zero V_S and V_T configuration (section 7.5) with in-phase gain set to minimum. The input (output of the amplifier/filter PCB) should have negligible AC content and DC offset of less than 1mV.

pic required

Fig. 7.6.7.1 Null detector PCB2

In-phase synchronous rectifier: -

Adjust *VR5* for 0V ±1mV on TP8 (output of inverter INV1) relative to 0V on pin 3 of IC12. See fig.5.3.1.1.

Adjust *VR6* for 0V ±1mV on TP9 (output of synch. rect.) relative to 0V on pin 3 of IC14. See fig.5.3.2.1.

Adjust *VR9* for 0V ±1mV on TP10 (output of 25Hz BPF) relative to 0V on pin 3 of IC15. See fig.5.3.5.1.

Adjust *VR10* for 0V ±1mV on TP12 (output of 10Hz LPF) relative to 0V on pin 3 of IC16. See fig.5.3.5.2.

Adjust *VR11* for 0V ±1mV on TP11 (output of 0.5Hz LPF) relative to 0V on pin 3 of IC15. See fig.5.3.5.1.

Reference voltage differential amplifier: -

Adjust *VR1* for 0V ±1mV on TP2 (output of diff. amp.) relative to 0V on the bottom of *R19*. See fig.5.3.8.2.

Adjust *VR2* for 0V ±1mV on TP3 (output of inverter INV2) relative to 0V on the bottom of *R19*. See fig.5.3.9.1.

Adjust *VR3* for 0V ±1mV on TP4 (output of synch. rect.) relative to 0V on the bottom of *R19*. See fig.5.3.10.1.

Adjust *VR4* for 0V ±1mV on IC9 pin2 (virtual earth of integrator) relative to 0V on pin3. See fig.5.3.2.2.

To tune the 25Hz notch filter remove IC14 and connect a signal generator to TP9 and 0V on IC14 pin3: -

Adjust *VR7* and *VR8* to obtain a null (25Hz) at TP12. Replace IC14.

7.6.8 MDAC module

These DC offsets are critical as the op-amps drive the (low resistance) primary windings of transformers.

pic required

Fig. 7.6.8.1 MDAC module (see section 6.2.2)

Adjust *VR1* for 0V ±0.1mV on PN6 (output of IC1) relative to 0V on star point PN7. See fig. 6.2.2.1.

Adjust *VR3* for 0V ±0.1mV on PN10 relative to 0V on PN7 or PN9 (both versions). See figs. 6.2.2.3 and 6.2.2.4.

Check that there is negligible DC difference between PN7 and PN9.

Decades 5, 6, and 7 scaling: -

This is best done in external unity ratio check configuration (section 7.2): -

$$R_S = R_T = 100\Omega$$

Source Resistance	In-phase gain		Quad gain	Carrier	Freq.	Check	Meter	Bandwidth	Mode	Rotary switches
	Buttons	Pot								
100Ω	$\times 10^6$	5.00	×10	2mA	High	Unity	Normal	0.5Hz	Manual	0 to 1

The higher carrier current provides twice the normal sensitivity.

First is the unity ratio tweek: -

Adjust *VR1* on the ratio tweek PCB for precisely zero error on the meter with the ratio set to 1.0000000.

Then the correct scaling: -

Adjust the fine gain (potentiometer) for precisely full scale (on the meter for +0.5ppm of ratio change (from 1.0000000 to 1.0000005).

Adjust *VR2* for two units of change on the meter for the transition 1.0000000 to 0.9999999.

7.6.9 Negative and simulated capacitors

The negative capacitors neutralise the interwinding capacitances: -
a). Capacitance in parallel with the primary winding (NC1) and
b). Capacitance between the primary ratio winding and the main secondary ratio winding (NC2).

pic required

Fig. 7.6.9.1 negative capacitors

The first is equivalent to extra cable capacitance in parallel with the reference resistor (RS) and results in a quadrature imbalance. The adjustment is best done in basic checks configuration (section 7.1) with equal lengths of cable for R_S and R_T (minimum quadrature imbalance). Select maximum quadrature gain (minimum range). Select the meter to indicate quadrature imbalance. Viz: -

Source Resistance	In-phase gain		Quad gain	Carrier	Freq.	Check	Meter	Bandwidth	Mode	Rotary switches
	Buttons	Pot								
100Ω	$\times 10^5$	≈5.00	$\times 10^2$	1mA	High	Normal	Quad	0.5Hz	Manual	For balance

Adjust *VR1* (NC1) for zero quadrature on the meter.

The second affects the "common mode" rejection and is best tested in zero V_S and V_T mode with a twist – switch both R_S *(V)* connections between virtual earth and V_S on the reference resistor: -

$$R_S = R_T = 100\Omega$$

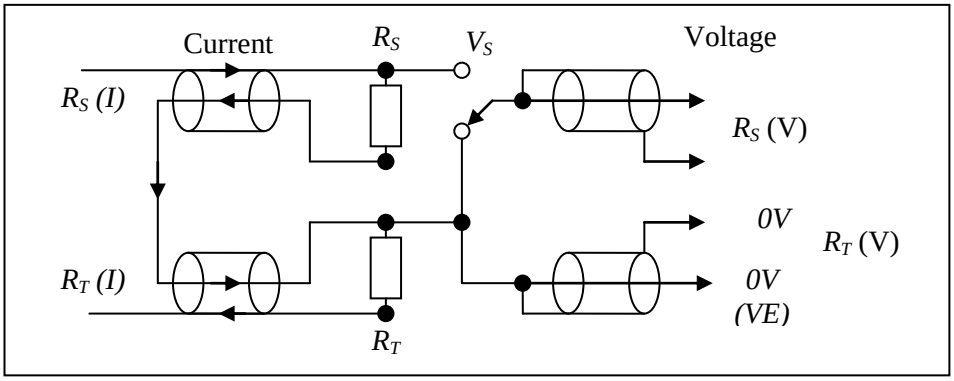

Fig. 7.6.9.2 Switching the common mode

Source Resistance	In-phase gain		Quad gain	Carrier	Freq.	Check	Meter	Bandwidth	Mode	Rotary switches
	Buttons	Pot								
100Ω	$\times 10^5$	≈5.00	$\times 10^2$	1mA	High	Normal	Quad	0.5Hz	Manual	0.0000000

The meter should read zero when both R_S (V) inputs are connected to virtual earth (VE).

Adjust *VR2* (NC2) for zero quadrature on the meter when R_S (V) are both connected to V_S.

It may be worth trying to connect R_S (V) to V_T (R_T (I) outer).

Simulated capacitor DC offset: -

The simulated capacitor stabilises the active drive. To adjust the DC offset select the zero V_S and V_T configuration (section 7.5).

Adjust *VR3* for 0V ±1mV between pins 2 and 3 of IC5. Use a battery powered DMM as pin 3 is the bridge virtual earth - from the guard amplifier (neither input is PSU 0V). See fig. 6.3.2.

7.7 Final checks

Work in progress. Feedback please.

See section 1 for overview diagrams