3. Carrier generator

3.1 Phase-lock loop PLL1

The bridge current source starts with a phase-lock loop to produce a 25 or 75Hz clock (CLK1) which is frequency and phase locked to the local 50Hz supply. The outline is repeated here for convenience: -

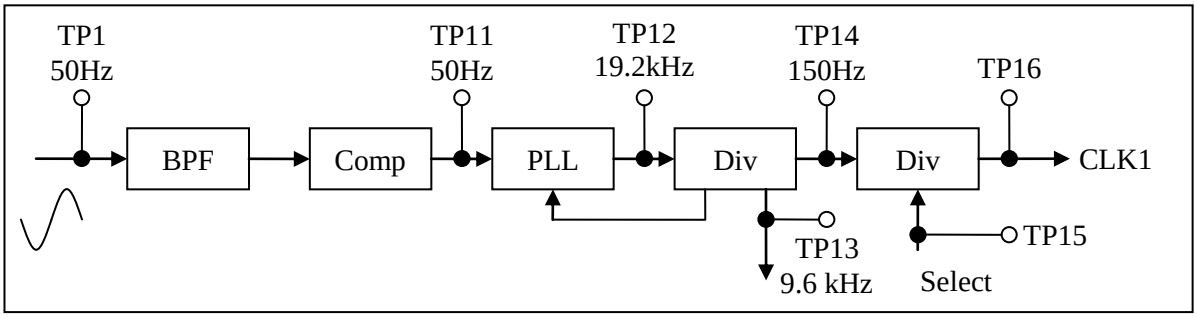

Fig. 3.1.1 Phase-lock loop PLL1

The first two stages are a simple (passive) band-pass filter (BPF) and comparator stage (Comp) to produce a 50Hz logic level compatible input to the next stage. The input offset trimmer for IC14 (not shown) is *VR11*: -

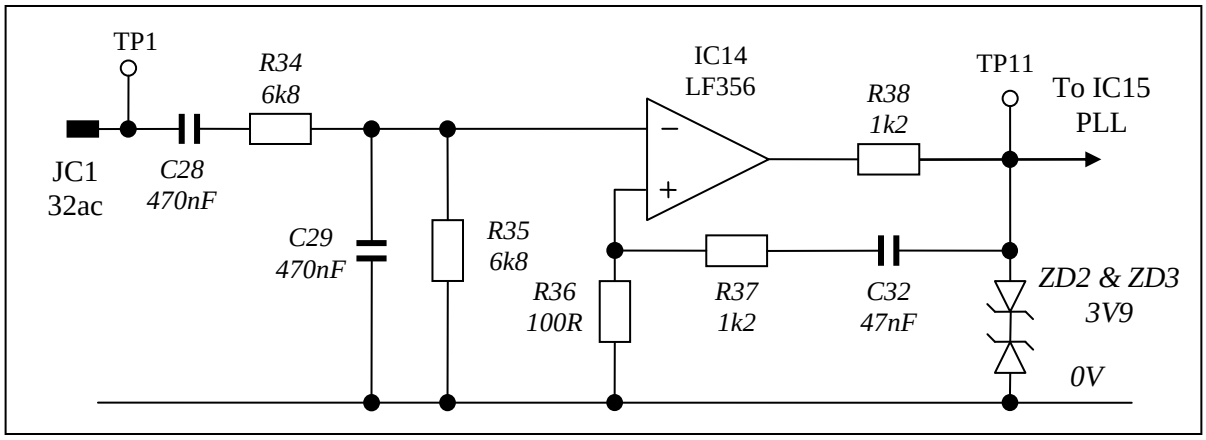

Fig. 3.1.2 Band-pass filter and comparator

The voltage controlled oscillator (VCO) and phase comparator (PC2) are within the CMOS chip (CD4046): -

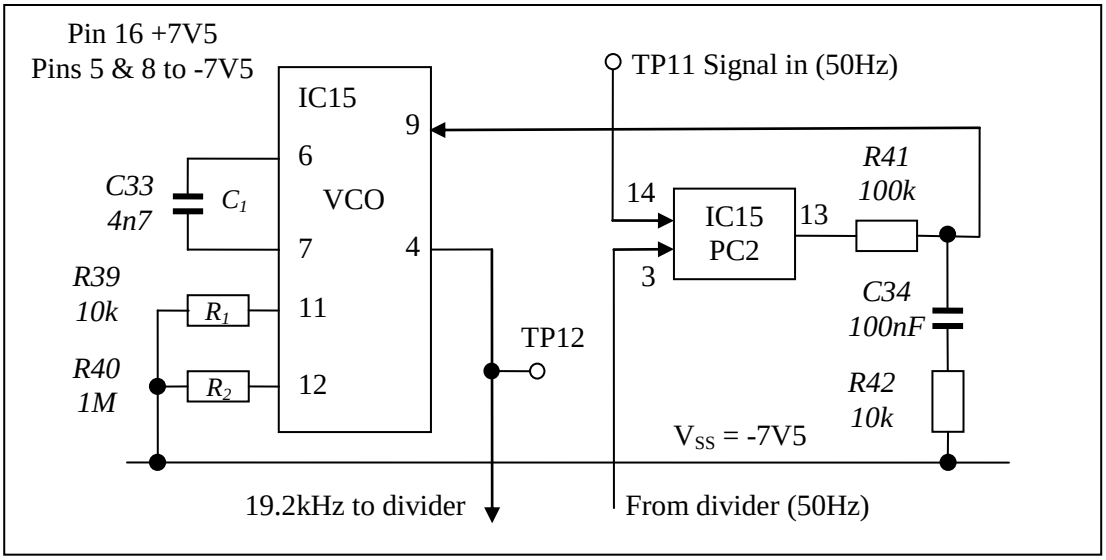

Fig. 3.1.3 Voltage controlled oscillator and phase comparator

According to the data sheet the output (frequency) of the voltage controlled oscillator (VCO: pin 4)) consists of a variable plus a fixed (minimum) component, in Hz: -

$$f = \left(\frac{V_{IN} - V_{SS}}{V_{DD} - V_{SS}} \right) \frac{k_1}{R_1 C_1} + \frac{k_2}{R_2 C_1}$$

Where V_{DD} and V_{SS} are the positive and negative power supplies: pins 16 and 8 respectively (±7.5V logic).

V_{IN} is the VCO input (pin 9).

The constants, k_1 and k_2, depend on the supply voltage (V_{DD}-V_{SS}) but are of the order 2.35 ($V_{DD} - V_{SS}$ = 15V).

The minimum frequency is approximately 500Hz (k_2 = 2.35) and much lower than the variable component (V_{IN} = 0V) of approximately 22kHz. It would seem, however, that the VCO is designed to run at 19.2kHz. It is not clear why the minimum component is so small.

The divider stages consist of a seven stage binary divider and two programmable divide by N chips: -

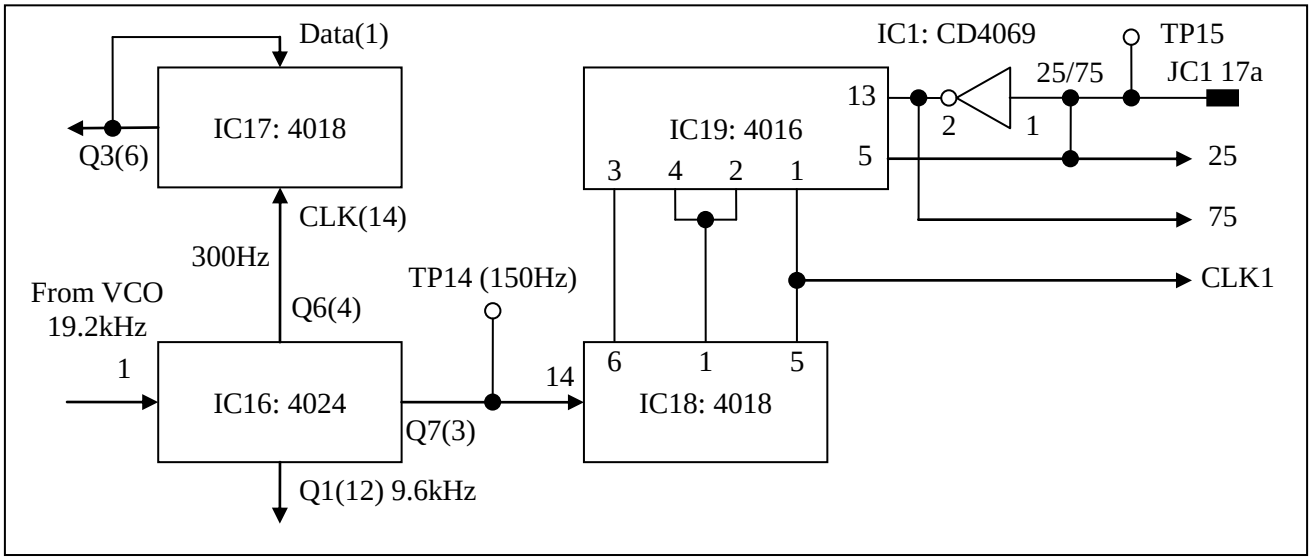

Fig. 3.1.4 PLL1 divider stages

The 19.2kHz output of the VCO is divided by 2 to produce a 9.6kHz clock for the A/D converter (µcontroller PCB), presumably to synchronise it to the carrier. See section 3.6. It is then divided by 5 more stages to produce 300Hz. For details on the interface to the µcontroller see section 3.12.

IC17 (CD4018) then divides the 300Hz signal by 6 to produce 50Hz which is fed back to the phase comparator. See fig. 3.1.3.

The seventh stage of the binary counter produces 150Hz which is then divided by 2 or 6 by the second divide by N stage (IC18: CD4018) to produce CLK1 (25 or 75Hz), depending on the control input (25/75).

Selection is by quad analogue switch (IC19: CD4016) which connects either pin 6 (notQ3 of IC18) or pin 5 (notQ1 of IC18) back to pin 1 (data input).

The in/out of the unused switches (pins 8, 9, 10 & 11) are connected to 0V. The unused control inputs are connected to V_{SS} (-7V5). Similarly for the other chips: -

	IC15	IC16	IC17	IC18	IC19
To V_{DD} (+7V5)	16	14	16	14	14
To V_{SS} (-7V5)	5 & 8	2 & 7	7, 8 10 & 15	8, 10 & 15	6, 7 & 12

3.2 Modulator and filter stages

The clocks signal CLK1 (25 or 75Hz) drives a DC to AC modulator/filter to produce a sine wave at the chosen frequency. The outline schematic is reproduced here for convenience: -

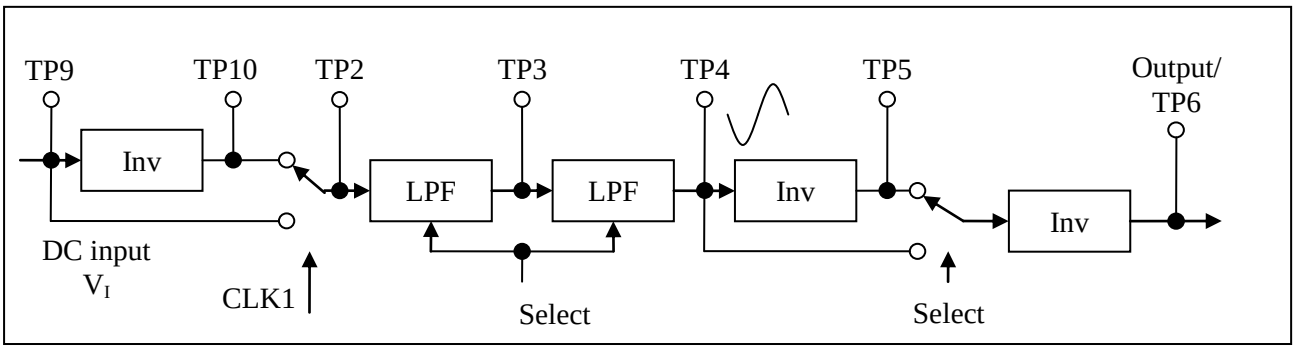

Fig. 3.2.1 Modulator and filter stages

For details on the frequency and invert control signal interfaces see section 3.12.

The DC signal, V_I, from the amplitude control circuit (integrator output) is converted to a symmetrical square wave (equal positive and negative) at CLK1 frequency: -

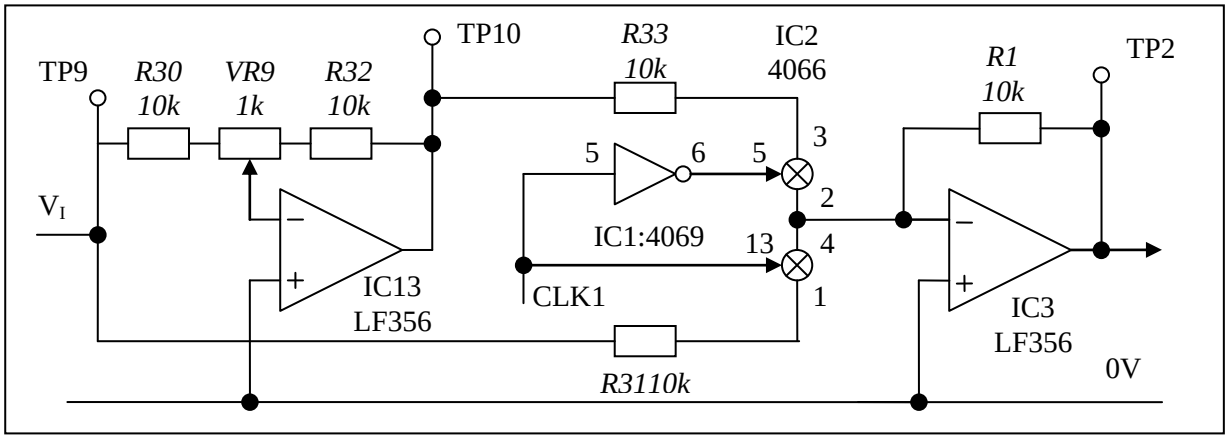

Fig. 3.2.2 Modulator stage

The offset trimmers (not shown) are IC13: *VR10* and IC3: *VR1*.

The first low-pass filter employs an analogue switch (IC4: CD4066) to select one of two feedback networks. A logic 1 (+7V5) on the relevant control line selects the natural frequency: -

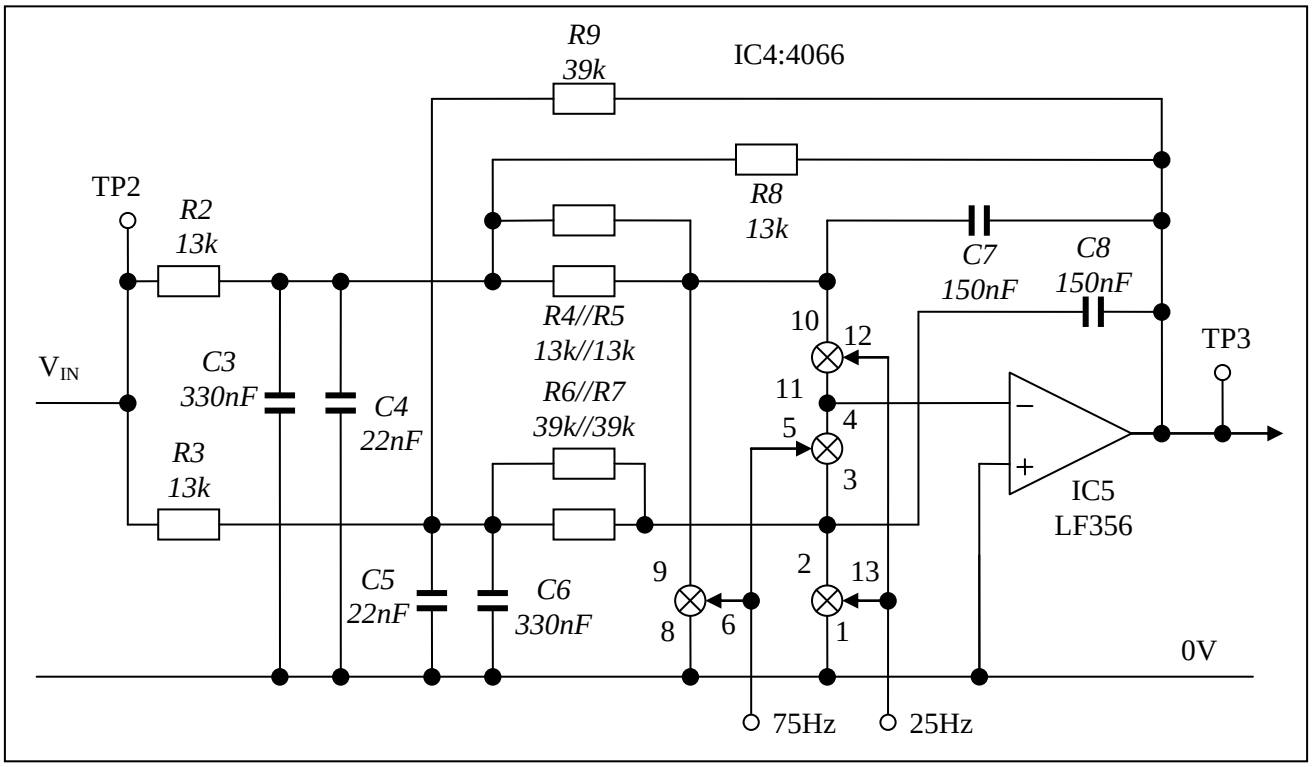

Fig. 3.2.3 Low-pass filter LPF1

The offset trimmer for IC5 (not shown) is *VR2*.

The 25/75Hz control signal are produced in fig. 3.1.4. Similarly for the second low-pass filter: -

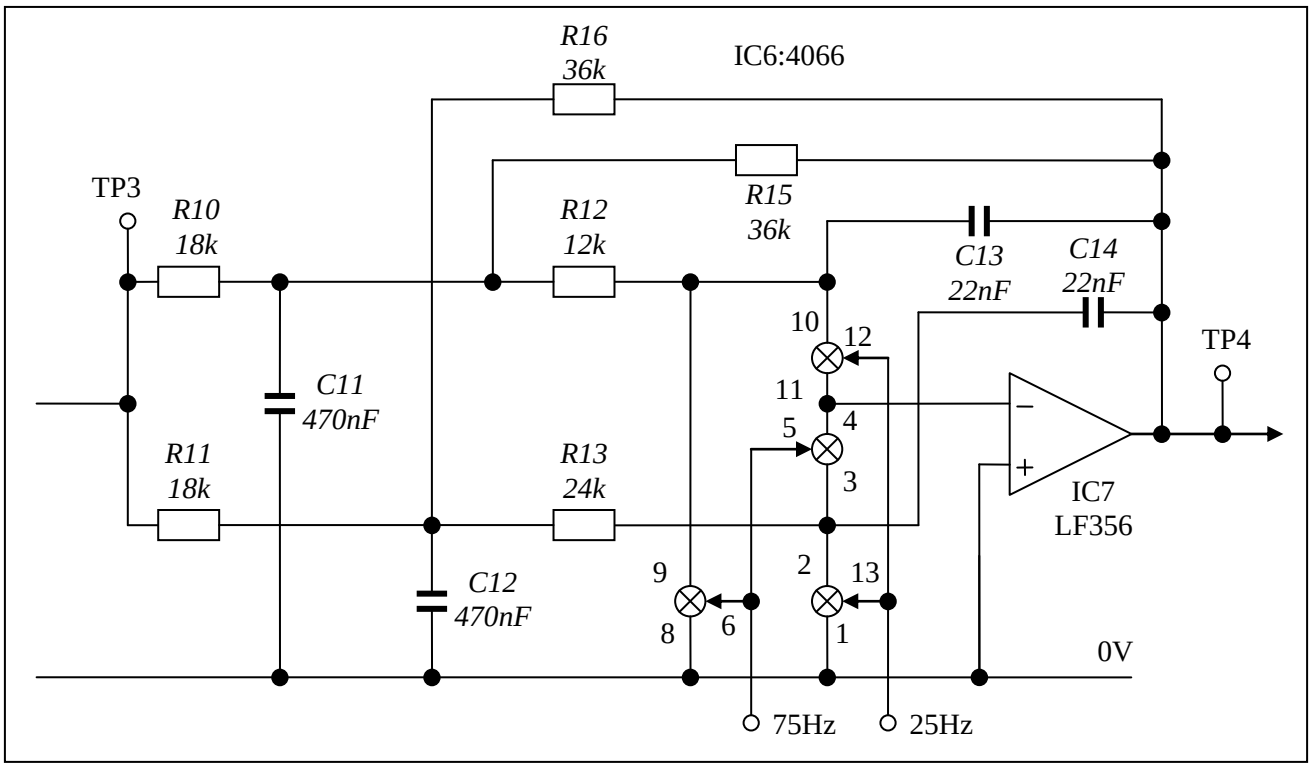

Fig. 3.2.4 Low-pass filter LPF2

Why are LPF1 and LPF2 different?

3.3 Phase reversal circuit

Whereas it is highly unlikely the presence of power supply sub-harmonics could affect accuracy, especially when operating at 25Hz. Fortunately the inclusion of a phase reversal circuit makes it possible to detect and correct for such interference: -

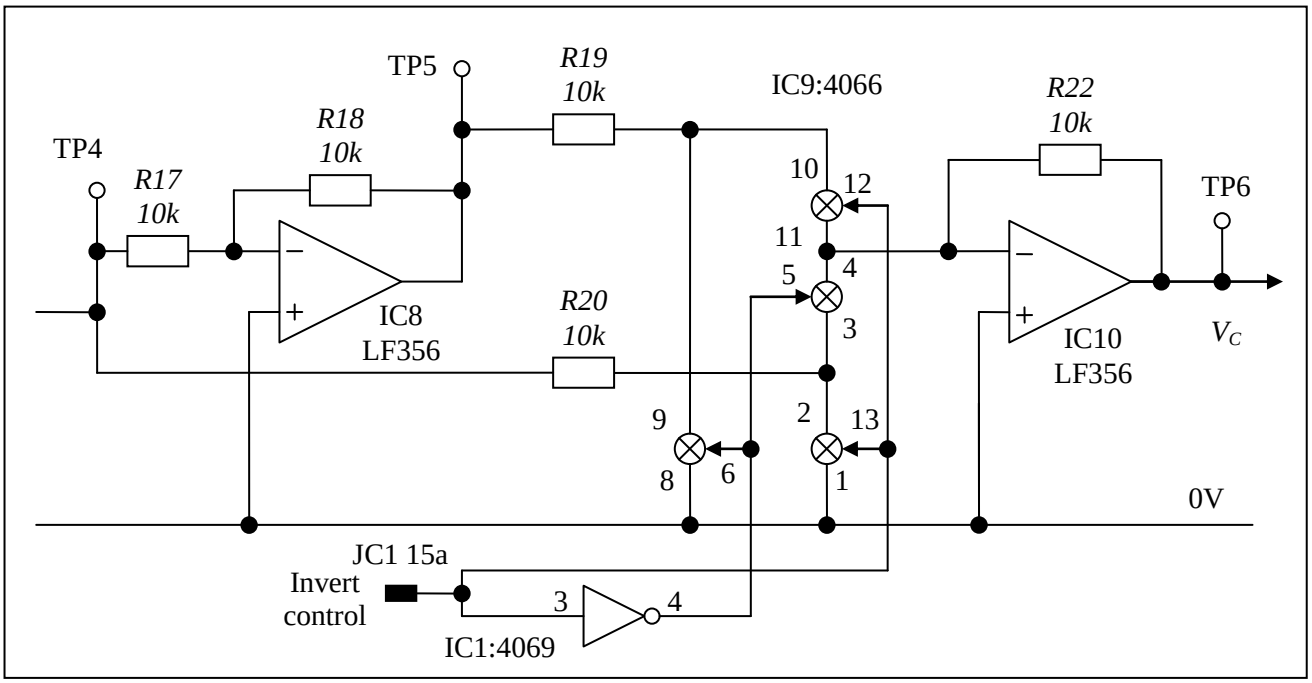

Fig. 3.3.1 Selectable phase inverter

The offset trimmers (not shown) are IC8:*VR4* and IC10:*VR5*.

For details on the invert control interface see section 3.12.

3.4 Amplitude control circuit

The amplitude control circuit consists of a half wave rectifier and an integrator: -

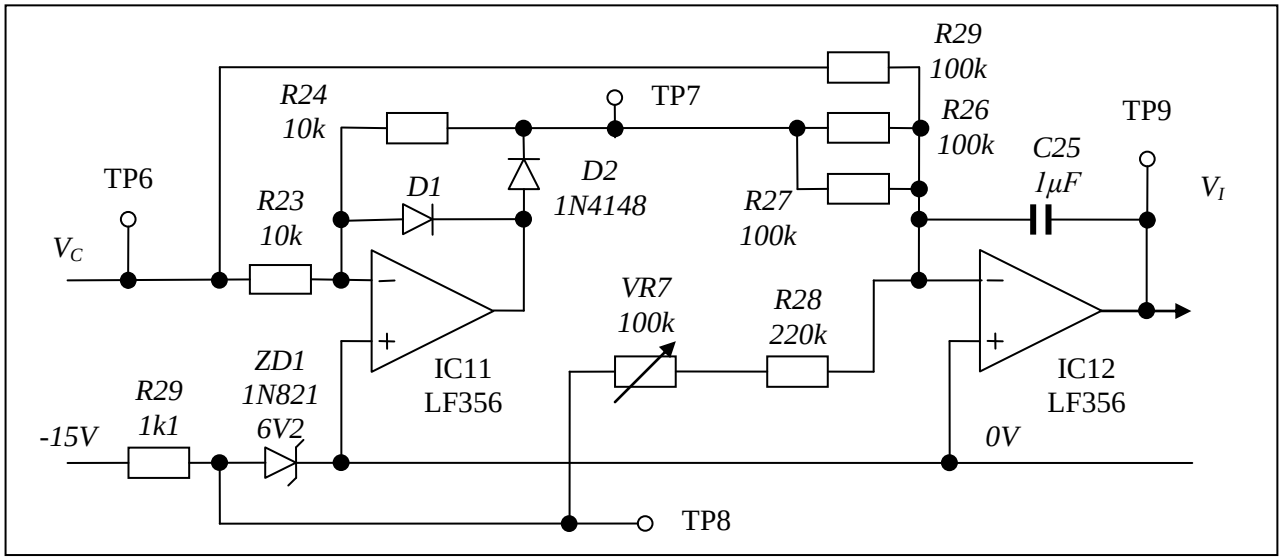

Fig. 3.4.1 Amplitude control circuit

The offset trimmers (not shown) are IC11:*VR6* and IC12:*VR8*.

For the positive half cycle the input voltage, V_C, results in a current (via *R29* = 100k) into the integrator summing junction (virtual earth). Zero current flows from the half wave rectifier (*R24*, *R26* and *R27* connect two virtual earths).

For the negative half cycle the positive output of the half wave rectifier results in twice the current compared to the direct input and the net current is thus the same as for the positive half cycle. The peak (full wave rectified) AC current into the summing junction is, therefore: -

$$I_{PK} = \frac{V_C(pk-pk)}{2R_{29}}$$

For a full wave rectified sinewave the average current is $2/\pi$ times the peak. The integrator stabilises when the total current into the summing junction is zero so that the average AC current into the summing junction is equal to the DC reference current: -

$$I_{AVE} = \frac{V_C}{\pi R_{29}} = \frac{V_{REF}}{R_{REF}} = \frac{6.2V}{270k} \quad \Rightarrow \quad V_C = 7.2V$$

This assumes that the trimmer is in the middle of its range (*VR7* = 50k). In practice the trimmer is adjusted for precisely 8V (pk-pk) at test point TP6.

The DC offset trimpot for the half wave rectifier IC11 is *VR6*. Adjust *VR6* for an accurate 0V level of the waveform at test point TP7: -

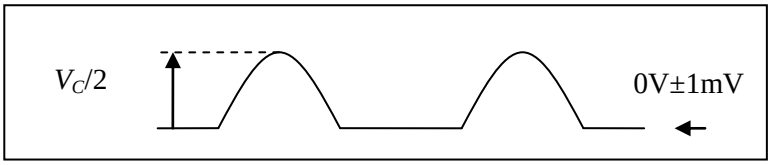

Fig. 3.4.2 Correct DC level

3.5 Phase reference phase-lock loop (PLL2)

A second phase-lock loop is used to generate the phase reference signals for both in-phase and quadrature synchronous rectifiers. The outline schematic is repeated here for convenience: -

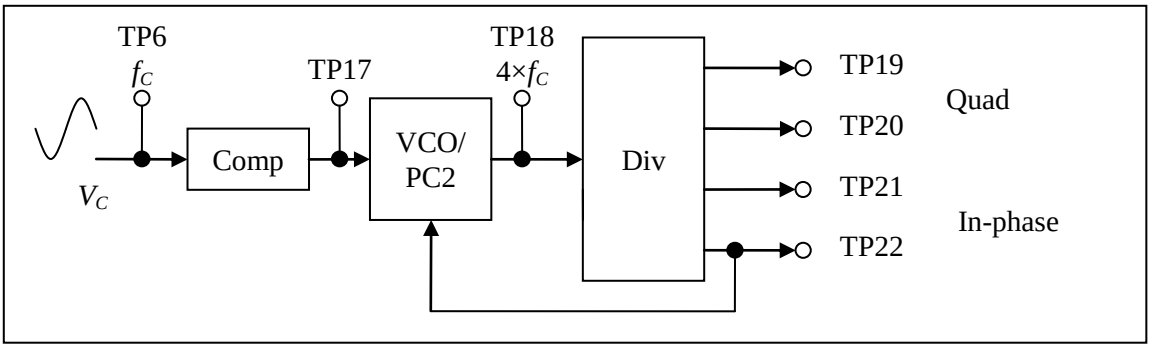

Fig. 3.5.1 Outline schematic of PLL2

The comparator (COMP) converts the sine wave signal, V_C, to a logic level compatible signal (±7V5) for input to the phase comparator: -

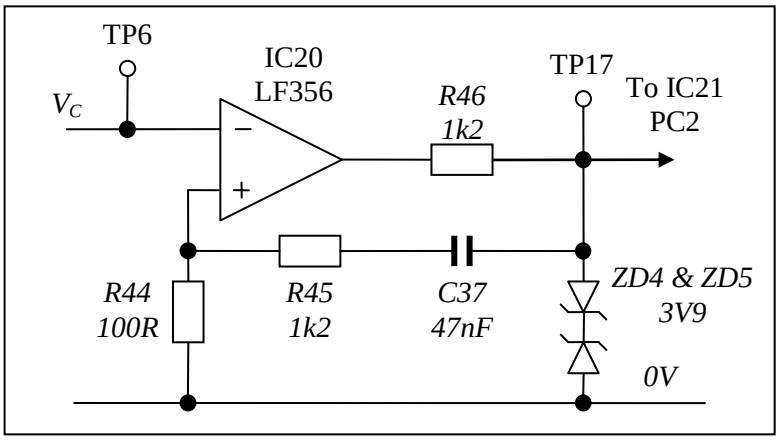

Fig. 3.5.2 Comparator circuit

The voltage controlled oscillator and phase comparator are within the CMOS chip CD4046: -

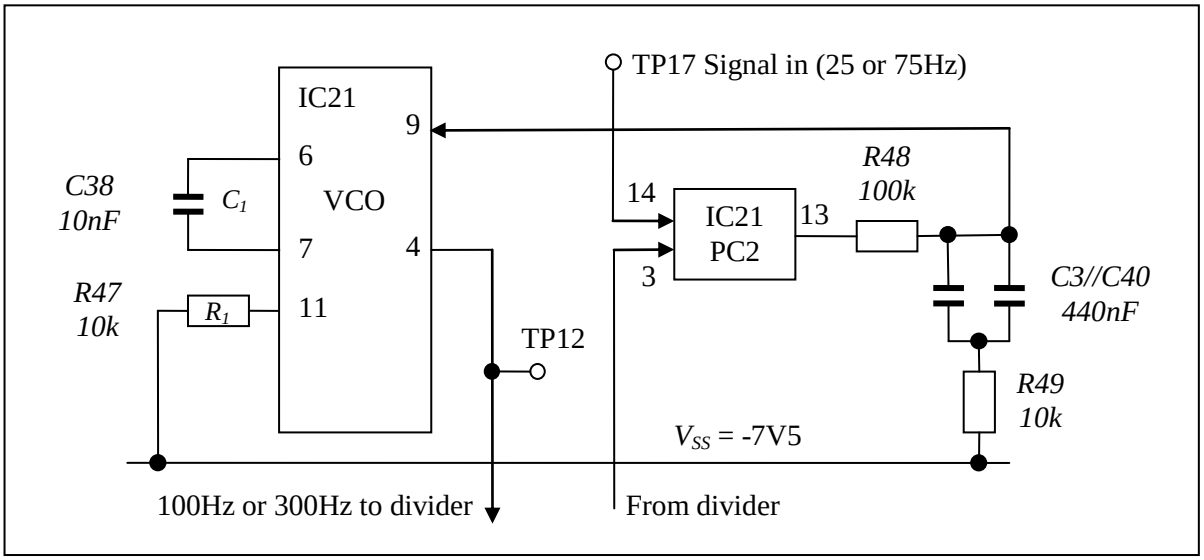

Fig. 3.5.3 Voltage controlled oscillator and phase comparator circuit

With 0V input the VCO is designed to operate at approximately 12kHz. Why so high when the maximum required is around 300Hz?

The divider stage employs a pair of D-type flip-flops (IC22: 4013): -

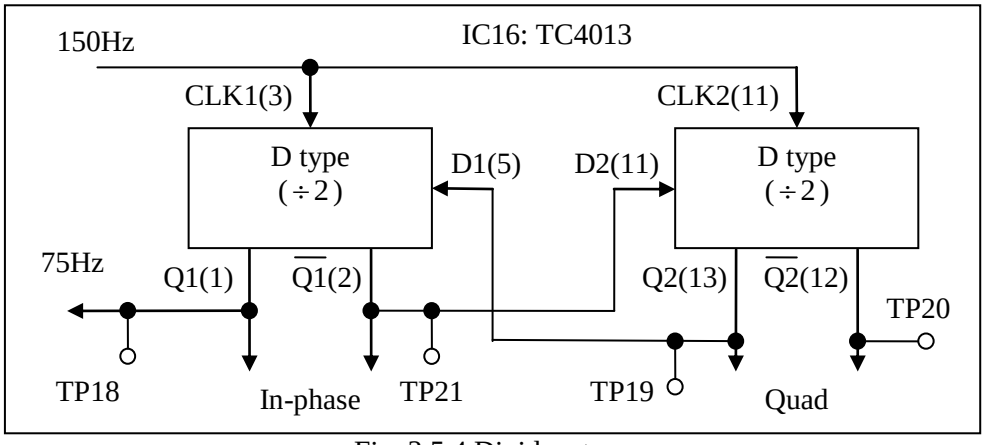

Fig. 3.5.4 Divider stage