ASL F18 circuits

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The collection of monographs “High Accuracy Electronics” can be found at: -

https://drive.google.com/folderview?id=1TbomXeoBble-IVADaOOmyyLH9le-3wAt

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Contents

1. Introduction and overview

1.1 Bridge configuration

The ASL F18 employs a pair of high accuracy voltage followers (HAVFs) [1] to drive the energising windings of a three-stage ratio transformer [2] in a novel bridge configuration: -

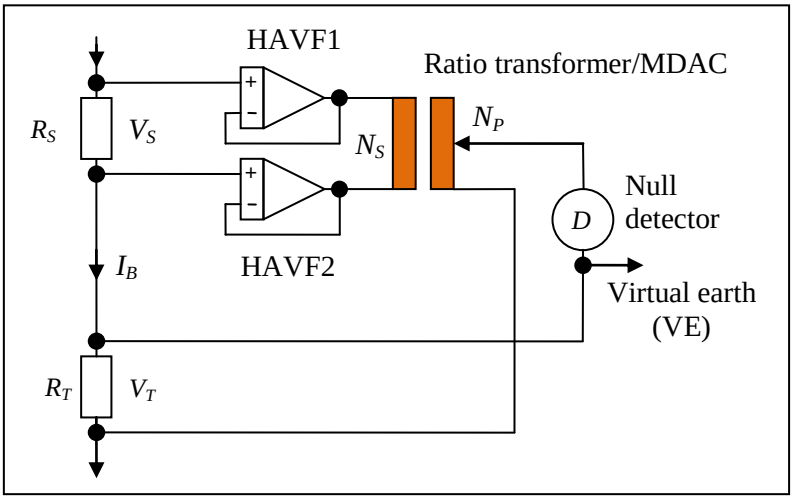

Fig. 1.1.1 The F18 bridge configuration

The HAVFs and ratio transformer are depicted here in the conventional way for simplicity. The actual circuits are rather more subtle. For a thorough understanding it is recommended that the reader study the relevant monographs.

The most sensitive part of the bridge circuit is maintained at local 0V ("virtual earth") by the active guard circuit - a high gain block [3].

The full range of ratio is 0.0000000 to 1.2999999. The first five digits are implemented with two stages of ratio transformer. The lower three digits are implemented with an MDAC plus a two-stage step-down (10000:1) transformer.

The in-phase component of the bridge output (input to the null detector) is: -

$$V_D = \frac{N_S}{N_P} V_S + V_T = \frac{N_S}{N_P} I_B R_S - I_B R_T$$

At null balance $(V_D = 0)$ the resistance ratio is the transformer turns ratio: $\frac{R_T}{R_S} = \frac{N_S}{N_P}$

The null detector [4] also detects any quadrature imbalance which is automatically reduced to zero by the action of a quadrature servo in both manual and automatic (in-phase) balance modes.

The bridge operating frequency is selectable 25Hz or 75Hz (60Hz or 90Hz for the USA version) phase locked to the local power supply. Whereas it is very unlikely that any sub-harmonics are present the relative phase is reversible so that such interference can be detected.

For more detail see [5].

1. Part 4, monograph 2: "High accuracy voltage followers".
2. Part 3, monograph 4: "Three-stage RTs".
3. Part 4, monograph 1: "High gain blocks".
4. Part 5, monograph 1: "Null detectors – the basics".
5. Part 3, monograph 7: "An F18 type ratio transformer bridge".

1.2 The active guard circuit

Another innovative feature of the F18 is the use of a high gain block (HGB, two-stage, type 1 [1]) to create a "virtual earth" point (VE) for the bridge. The HGB, standard resistor and thermometer are configured as an inverting amplifier. The action of feedback ensures that the inverting input of the HGB is maintained at the primary 0V (P0V) very accurately, setting the bridge potentials relative to local earth. This is much more practicable than a "Wagner balance" [2]: -

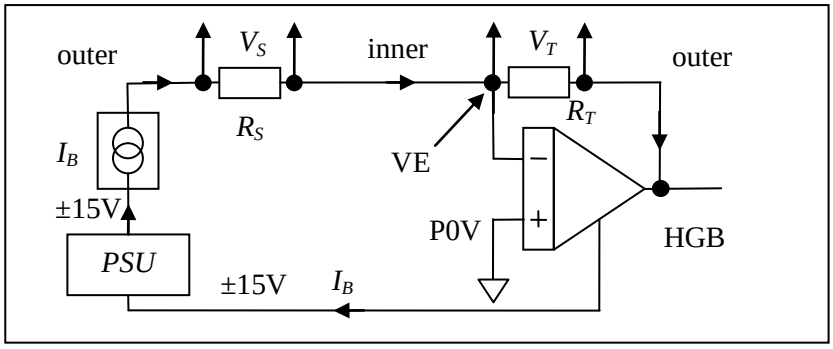

Fig. 1.2.1 The active guard circuit

A useful way to remember the coax cable connections for normal operation is "outer conductors to the outer part of the bridge". The inner connections (between R_S and R_T) are sensitive to interference and are shielded by the outer conductors.

Note that the current returns to the source via the power supply. The area of the loop (and stray flux) thus created is minimised by a combination of twisted pairs and go/return pairs if PCB tracks.

1.3 The quadrature servo

The F18 has a separate quadrature synchronous rectifier (Quad SR) and automatic null balance (a.k.a. "quadrature servo") implemented with an analogue multiplier and a low phase error (ferrite) transformer. The output is added in series with the output of the ratio transformer/MDAC . For in-depth theory see [3 and 4].

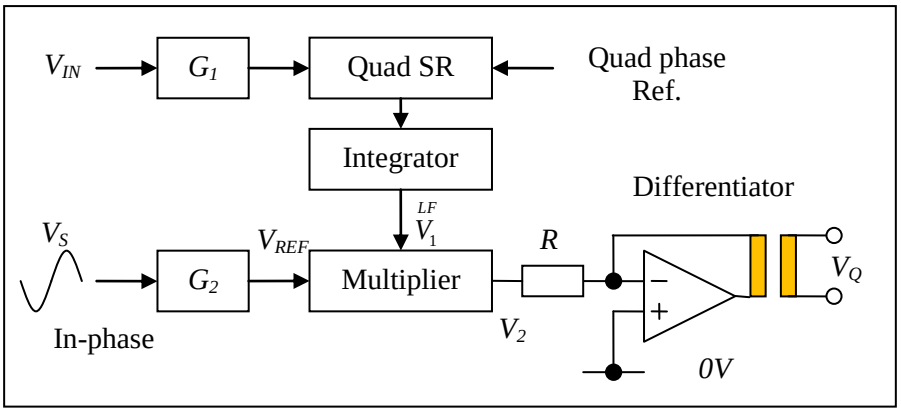

Fig. 1.3.1 Quadrature servo

With null balance for both in-phase and quadrature components the phase accuracy, of the amplifier/filter stages before the synchronous rectifiers, is far less important so that a high degree of filtering is possible (band-pass for 25 or 75Hz and notch filters for supply harmonics).

1. Part 4, monograph 1: "High gain blocks".
2. Part 3, monograph 7: "An F18 type ratio transformer bridge". See section 3.
3. Part 5, monograph 1: "Null detectors-the basics". See section 6.2.
4. Part 1, monograph 6: "Low phase error capacitors and inductors". See section 3.

1.4 Bridge current source

The bridge current generator circuits are on a PCB in slot 4 of the card frame.

The clock signal, CLK1 at 25 or 75Hz, is generated with a phase-lock loop (PLL). The output of a power transformer (18V RMS at 50Hz) is first passed through a (passive) band-pass filter (BPF) and then comparator (Comp) to produce a 50Hz logic signal (±7.5V). The first divider (Div) then provides feedback to generate a 150Hz logic signal. A second divider then generates CLK1 (divide by 2 or 6): -

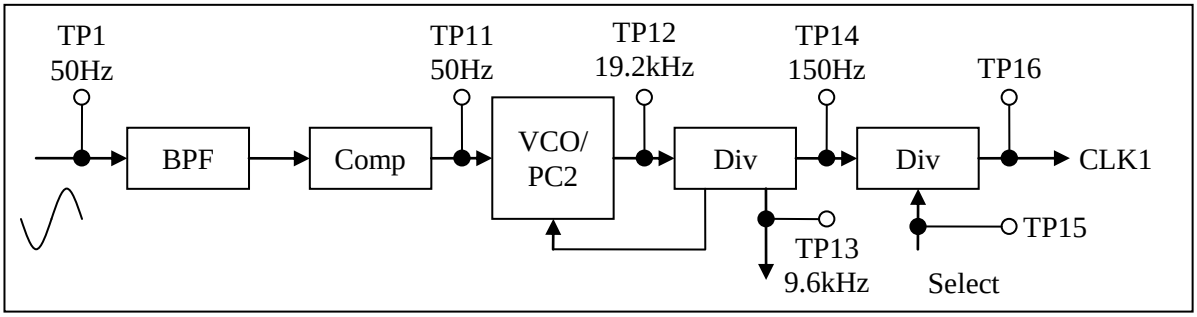

Fig. 1.4.1 Phase-lock loop (PLL1)

The clock signal CLK1 drives a DC to AC modulator/filter to produce a sine wave at the chosen frequency: -

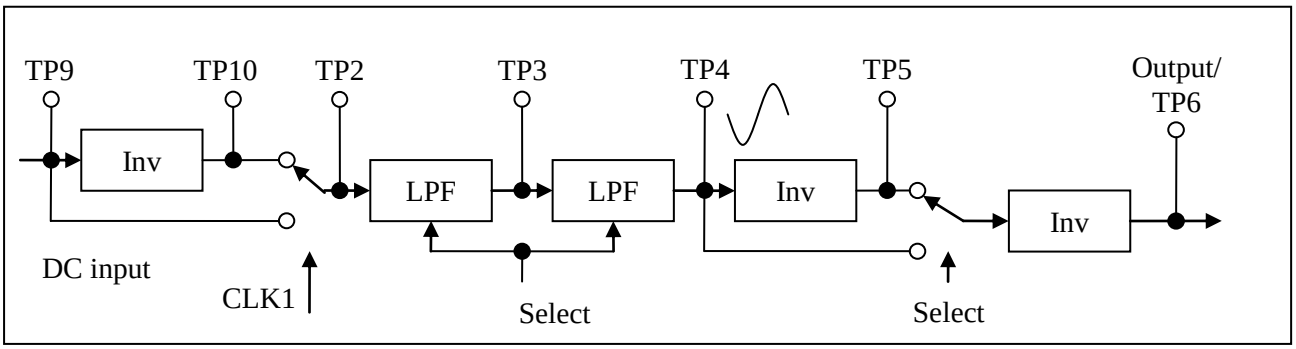

Fig. 1.4.2 Modulator/filter section

The modulator is a single pole two-way analogue switch, driven by CLK1, and produces a symmetrical square wave from the DC input (from an integrator: TP9) and its inverse (TP10). The square wave is then converted to a low distortion sinewave with two second order (Butterworth) low-pass filters (LPF). The natural frequency (-3dB gain) is selectable so that the total phase shift is a fairly precise 180 deg. The phase integrity, relative to the power supply, is thus maintained so that the final stage (inverted or not) can be used to detect the presence of sub-harmonic interference.

The amplitude is controlled by comparison with a reference diode (ZD1: -6.2V) and integrator/feedback loop: -

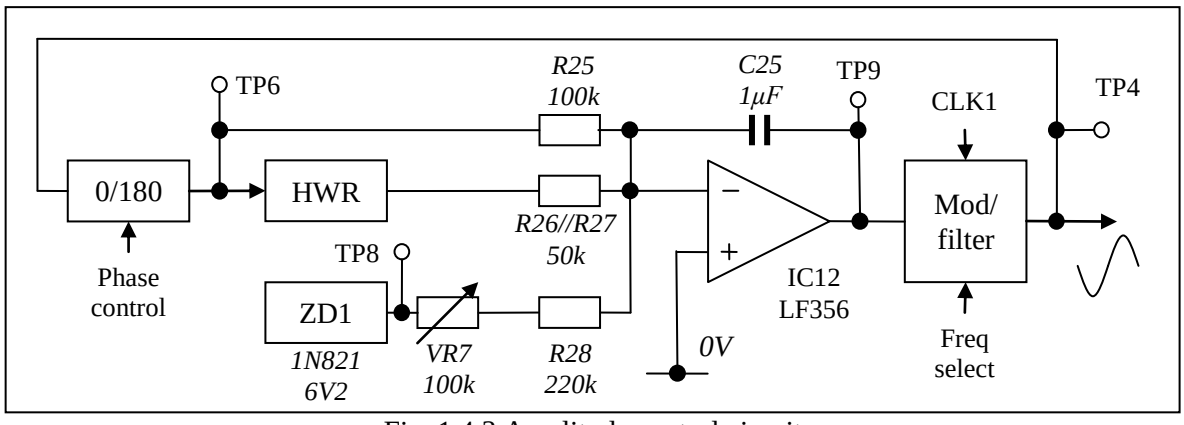

Fig. 1.4.3 Amplitude control circuit

The half wave rectified current (via HWR and *R26* in parallel with *R27*) plus the AC current via *R25* supplies, on average, the full wave rectified current into the virtual earth node of the integrator stage (IC12). An equal but opposite current is provided by the adjustable resistance from the (negative) reference voltage.

The DC output of the integrator, together with a 25/75Hz clock and frequency selector logic inputs, result in an amplitude controlled sine wave at the output (TP4 at ≈3V RMS).

The main oscillator is followed by an MDAC, two-stage high-pass filter (HPF), amplifier (Amp) and a voltage to current converter (V to I). The 1, 2, 5mA and $\times\sqrt{2}$ options are selected by the 12 bit code to the MDAC.

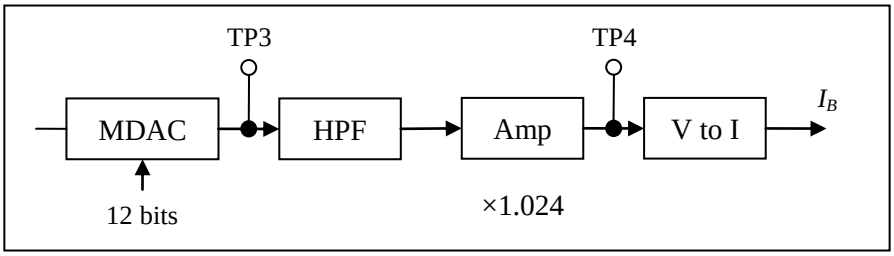

Fig. 1.4.4 Bridge current output stages

The voltage to current converter stage is a "Howland current pump" [1 and 2] based on a power op-amp with positive and negative feedback [1, 2]. Glass encapsulated relays select the ×0.1, ×1 and ×10 options: -

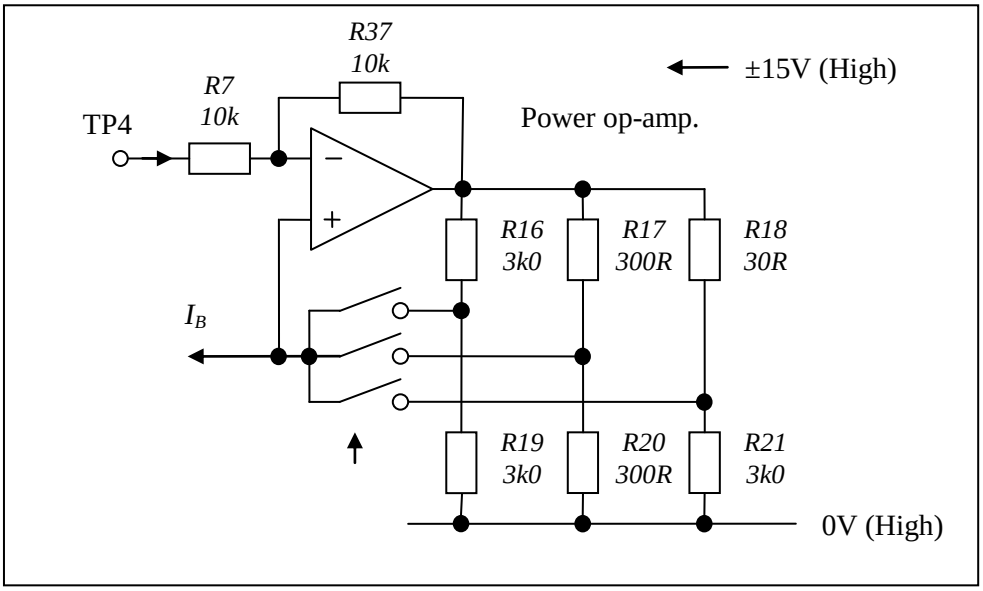

Fig. 1.4.5 Voltage to current output stage

Most of the current source circuitry is supplied by a low current ±15V supply. The final (power) stage of the V to I converter, however, is supplied by a separate high current supply which also supplies the guard amplifier.

The bridge current loop area (and stray flux) is minimised by careful routing of the conductors – a combination of twisted pairs and go/return pairs of PCB tracks (see fig. 1.2.1).

1. Sheingold D. H.: "Impedance & Admittance Transformations using Operational Amplifiers". The Lightning Empiricist, Vol. 12, No. 1. (Jan 1964).
2. Part 4, monograph 4: "The Isotech MicroK Bridge". See section 3.

A second phase-lock loop is used to generate the in-phase and quadrature phase reference logic signals: -

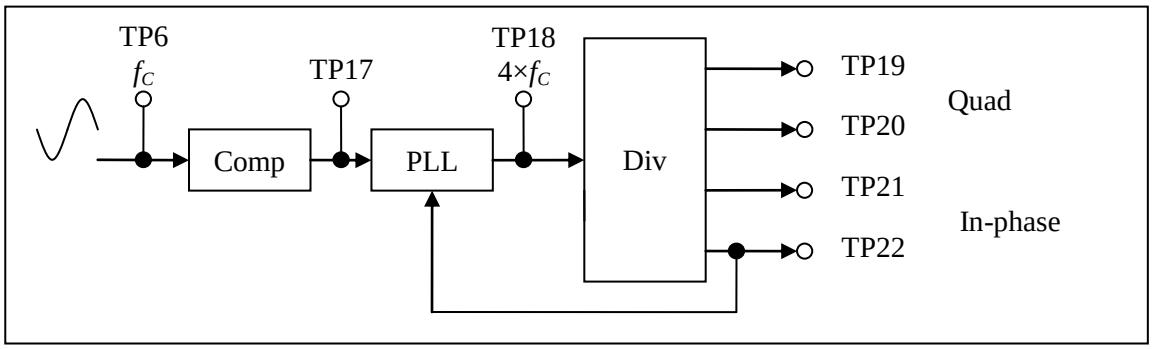

Fig. 1.4.6 In-phase and quadrature phase reference generator

The comparator (Comp) first converts the carrier signal to logic levels (±7.5V). The phase-lock loop then produces 4 times the input frequency. This is then divided by 4 to produce both in-phase and quadrature phase reference signals.

1.5 External reference resistor

To take advantage of the accuracy of the F18 the reference resistor the reference resistor needs to be very stable – typically a "Wilkins" AC/DC transfer standard (in an oil bath for temperature control): -

Fig. 1.5.1 A Wilkins type reference resistor

The reference resistor can be in the range 1Ω to 300Ω, depending on the resistance range of the resistance thermometer.

1.6 Internal zero and unity ratio checks

The F18 has provision for high accuracy zero and unity ratio checks: -

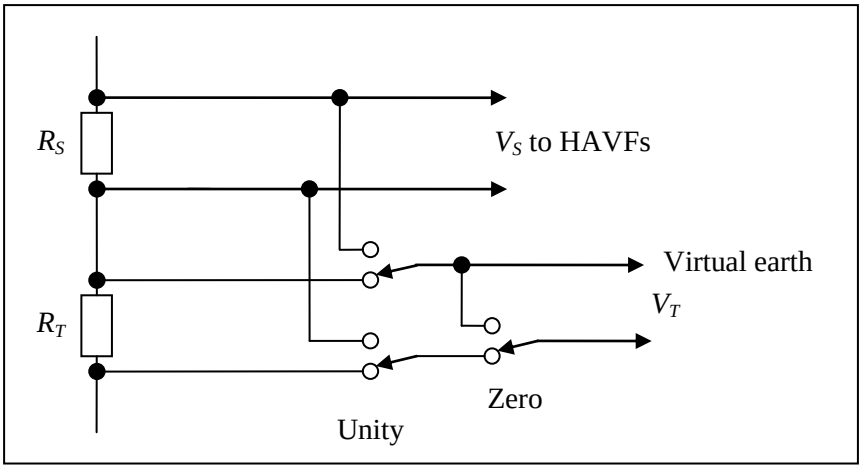

Fig. 1.6.1 Zero and unity ratio checks

Zero check: The bridge should balance at a ratio of precisely 0.0000000 (±0.1ppm).

Unity check: The bridge should balance at a ratio of precisely 1.0000000 (±0.1ppm).

The ratio tweek PCB has a trimmer (picture required) for adjusting the meter to read zero in internal or external unity ratio check configuration.

For adjustments and final checks see section 7.

1.7 The null detector

The null detector consists of three modules:

a). A low noise pre-amplifier with transformer for noise matching in a mumetal box for screening.
b). An amplifier/filter PCB in slot 6 of the card frame.
c). Phase sensitive detectors and quadrature servo in slot 5 of the card frame.

The card frame slots are numbered from right to left, as seen from the top and front. Please check.

1.7.1 Low noise pre-amplifier

The noise matching transformer [1] has three settings: 1, 10 and 100Ω: -

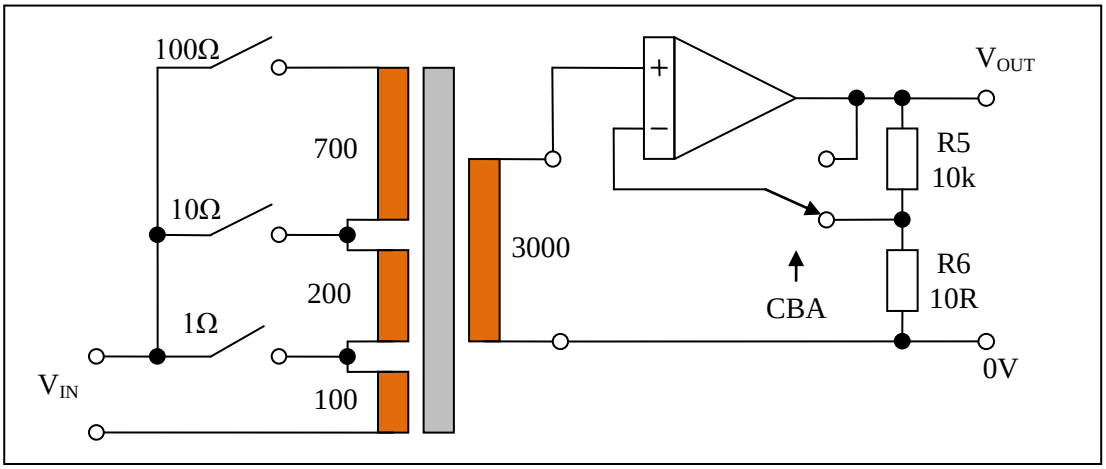

Fig. 1.7.1.1 Low noise pre-amp

The high gain block is a single stage composite amplifier with a matched pair of BJTs (long-tail pair) front-end, operated at 0.1mA each, for an input noise resistance of approximately 1kΩ [2].

The relay selects gain of ×1 or ×1001 according to a three bit gain control: -

Gain control code [3]						
C (MSB)	B	A (LSB)	Pre-amp	SGS1	SGS2	Total
0	0	0	×1	×1	×1	×1
0	0	1	×1	×10	×1	×10
0	1	0	×1	$\times 10^2$	×1	$\times 10^2$
0	1	1	$\times 10^3$	×1	×1	$\times 10^3$
1	0	0	$\times 10^3$	×10	×1	$\times 10^4$
1	0	1	$\times 10^3$	$\times 10^2$	×1	$\times 10^5$
1	1	0	$\times 10^3$	$\times 10^2$	×10	$\times 10^6$
1	1	1	$\times 10^3$	$\times 10^2$	$\times 10^2$	$\times 10^7$

Fig. 1.7.1.2 Gain setting truth table [4]

1. Part 3, monograph 5: “Noise matching transformers”. See section 2.
2. Part 5, monograph 2: “Low noise BJT pre-amps”. See section 4.3.
3. The bit labels A, B and C are consistent with the Fairchild CD4051 data sheet.
4. Gain relative to the lowest setting and not including the fine gain control (see next section).

1.7.2 Amplifier/filter PCB

The amplifier/filter PCB card (slot 6) consists of: -

a). Band-pass filter (BPF1: 25Hz or 75Hz selectable).
b). Switched gain stage (SGS1: ×1, ×10 and ×100).
c). Band-pass filter (BPF2: 25Hz or 75Hz selectable).
d). Notch filters (NF1: 50Hz and 150Hz).
e). Notch filters (NF2: 50Hz and 150Hz).
f). Switched gain stage (SGS2: ×1, ×10 and ×100).
h). MDAC fine gain control (12 bit).
i). Band-pass filter (BPF3: 25Hz or 75Hz selectable).

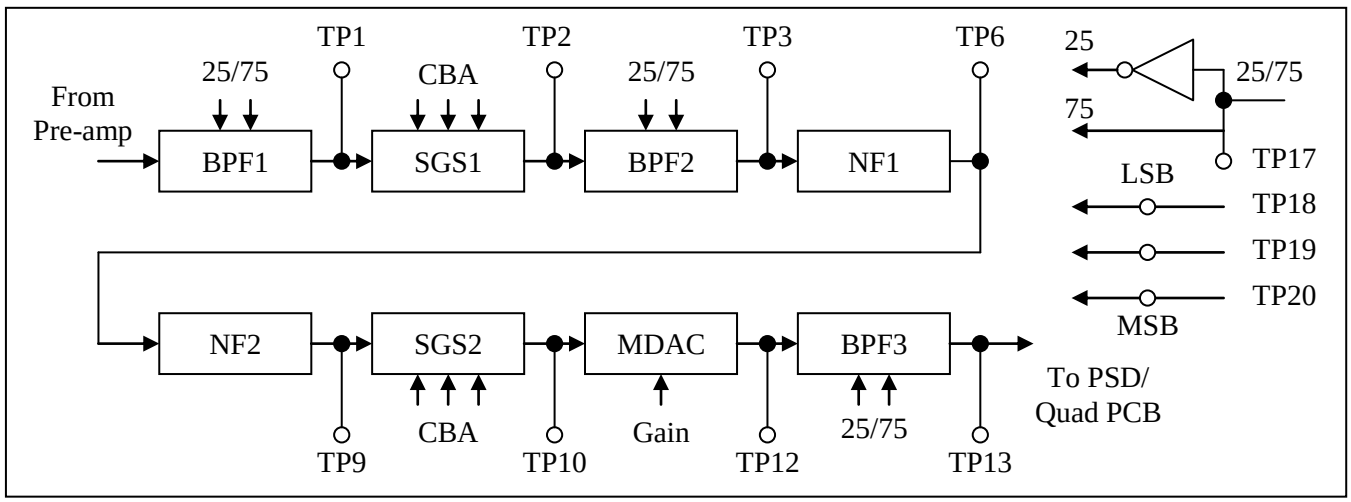

Fig. 1.7.2.1 Amplifier/filter PCB

The control lines come from the interface PCB (card frame slot 3): -

a). Band-pass filters (BPF1 and BPF2): Logic 1 input selects 75Hz.
b). Switched gain stages: The three control lines are CBA (see fig. 1.7.1.2).
c). MDAC fine gain control: 12 binary bits delivered 4 bits at a time with 2 address lines, chip select and write control. The gain is variable: up to ×10.

1.7.3 Phase sensitive detectors and quad servo PCB

The PSD/quad servo PCB card (slot 5) consists of: -

a). An inverter (Inv1).
b). In-phase synchronous rectifier (PSD1).
c). Two low-pass filters (LPF1 and LPF2) for the in-phase out-of-balance (including 25Hz notch).
d). Quadrature synchronous rectifier/integrator (PSD2/Int).
e). Analogue multiplier (Mult).
f). Mutual inductor stage (MI).
h). Switched gain stage (SGS) for the reference voltage.
i). Reference voltage synchronous rectifier/low-pass filter (PSD3/LPF) with a second inverter (Inv2).
j). Residual signal full wave rectifier and low-pass filter (FWR).
k). Residual and quadrature overload indicator/drivers (ROID and QOID).
l). Meter selector (analogue switch).

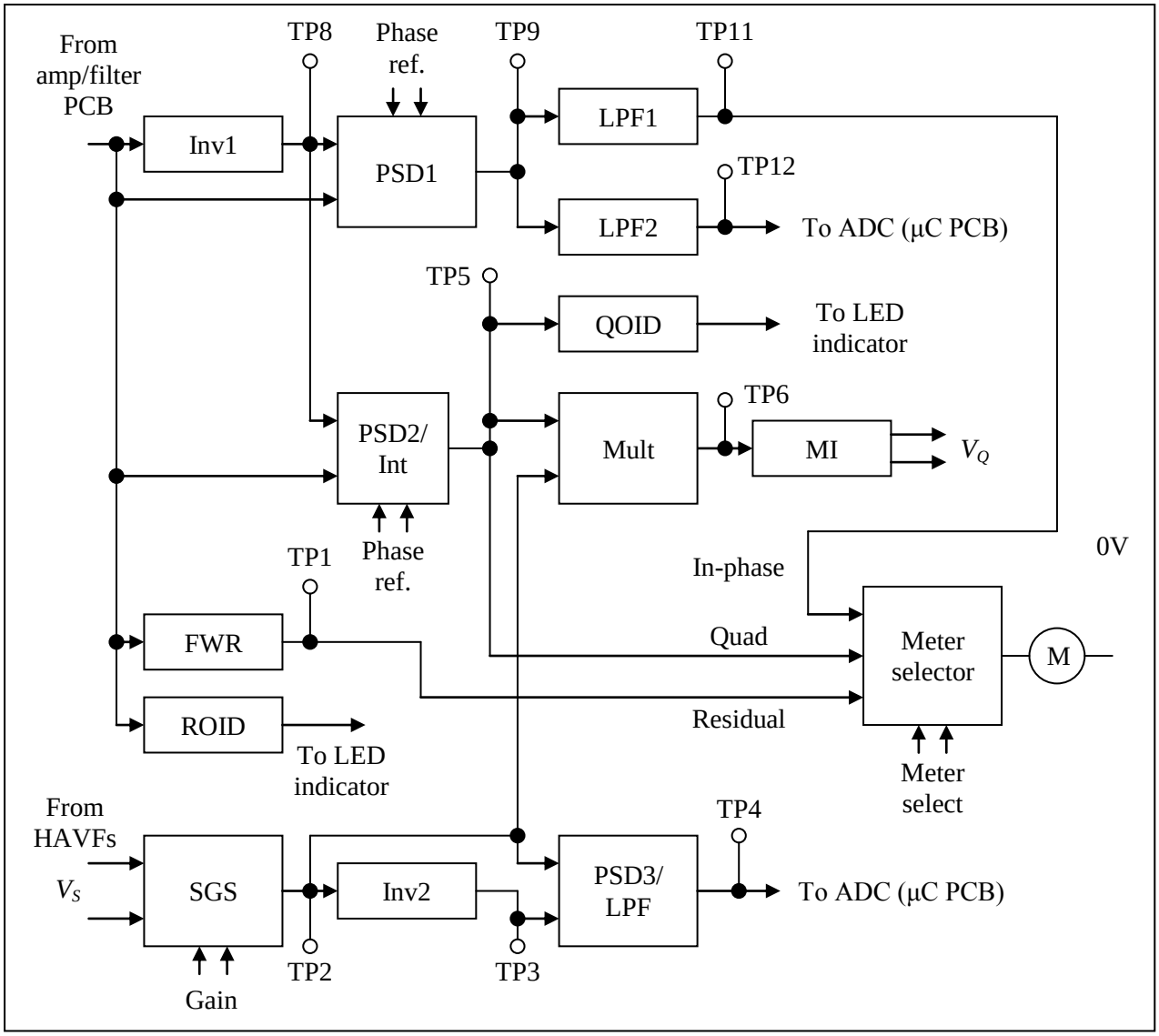

Fig. 1.7.3.1 Phase sensitive detector and quad servo PCB