5.3 The null detector PCB2

The synchronous rectifiers, quadrature servo and other circuits occupy a second double-eurocard PCB in slot 5 of the card frame. The connectors are JQ1 and JQ2. For an overview see section 1.7.3.

5.3.1 Inverter stage INV1

The synchronous rectifiers and residual rectifier stages share an inverter stage: -

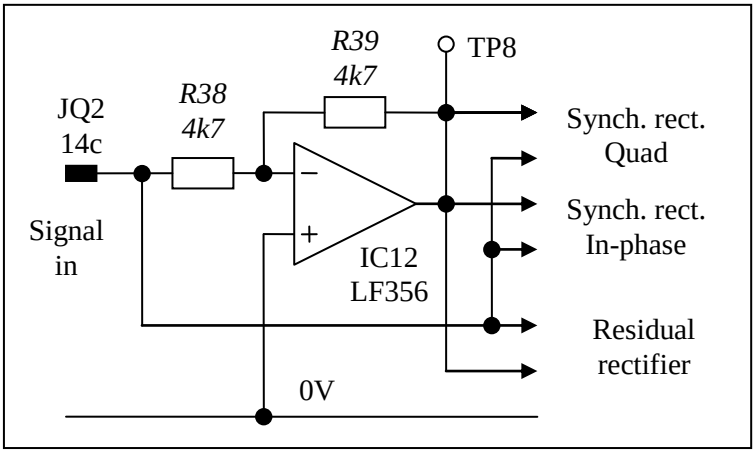

Fig. 5.3.1.1 Inverter stage INV1

The offset trimmer for IC12 (not shown) is *VR5*.

5.3.2 The synchronous rectifiers

The out-of-balance (AC) signal and its inverse are the inputs to the in-phase synchronous rectifier: -

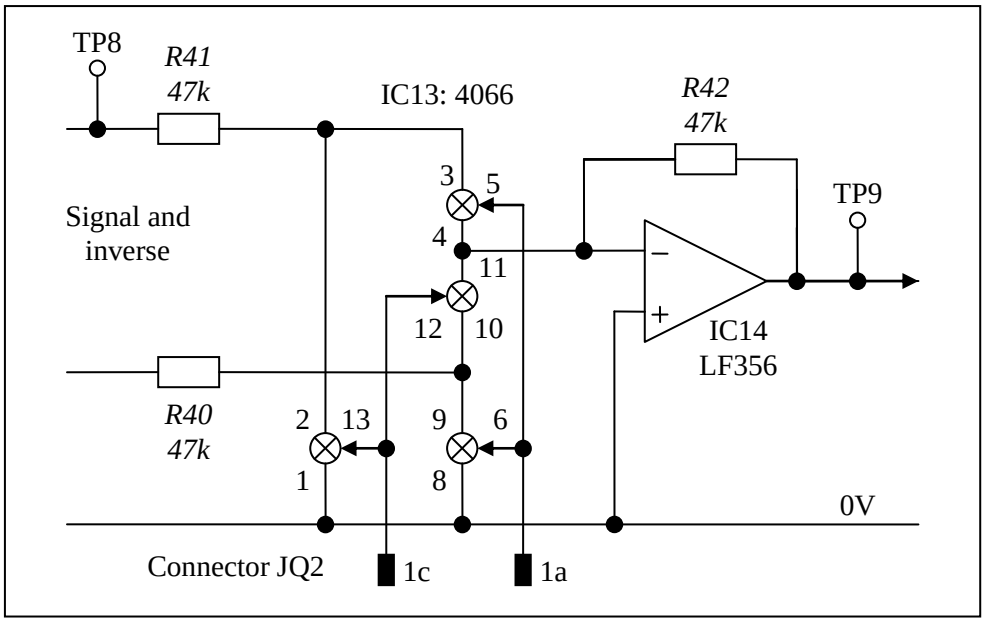

Fig. 5.3.2.1 In-phase synchronous rectifier

The offset trimmer for IC12 (not shown) is *VR5*.

TP9 is a key test point: the full-wave rectified out-of-balance signal. See section 7.

The quadrature synchronous rectifier integrates the quadrature out-of-balance: -

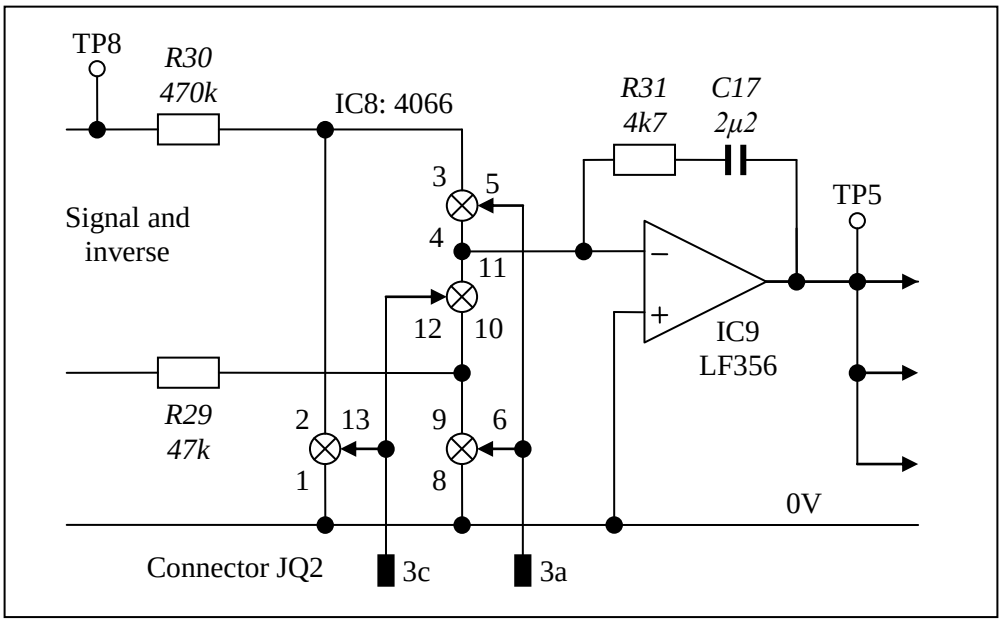

Fig. 5.3.2.2 Quadrature synchronous rectifier

The offset trimmer for IC9 (not shown) is *VR4*. It is unnecessary – it's an integrator.

One of the outputs goes to the analogue multiplier (IC10: AD534JH); the second to the quadrature overload detector circuit (see fig. 5.3.11.2) and the third to the meter selector circuit (see fig. 5.3.7.1).

5.3.3 The multiplier

The inputs are: -
a). AC from the differential switched gain stage reference amplifier (see figs. 5.3.8.1 and 5.3.8.2) and
b). DC from the integrator (see fig. 5.3.2.2): -

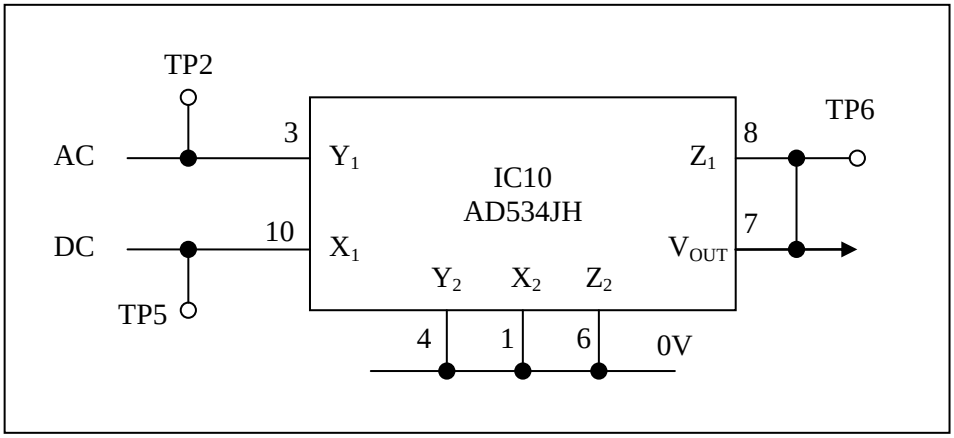

Fig. 5.3.3.1 Multiplier circuit

Power supply is +15V (pin 14), -15V (pin 3) and 0V (pin 10).

5.3.4 The mutual inductor

A low phase error (ferrite) transformer is used to ensure accurate conversion of in-phase AC voltage to quadrature (a phase shift of precisely 90deg) [1]: -

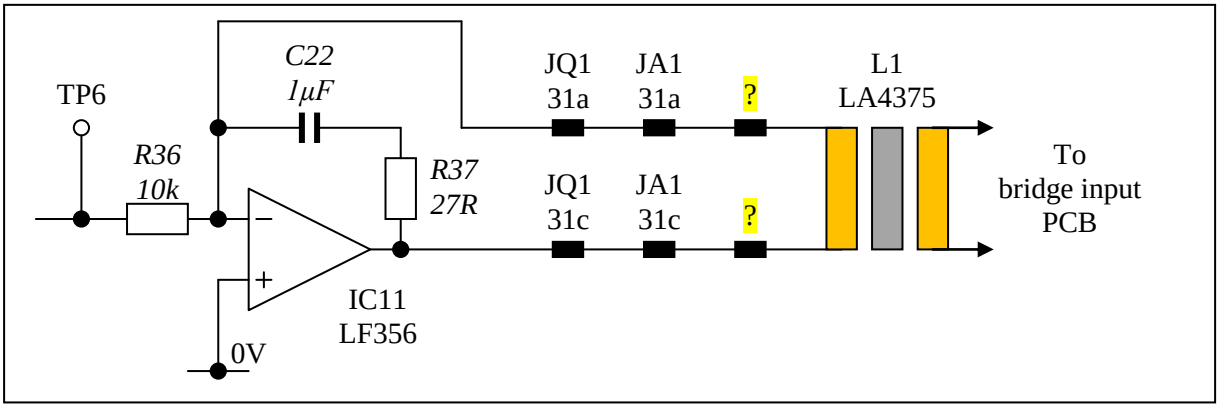

Fig. 5.3.4.1 Quadrature phase shifter

The output is added in series with the output of the main ratio transformer on the side of the null detector pre-amp which is not the virtual earth. Pls check.

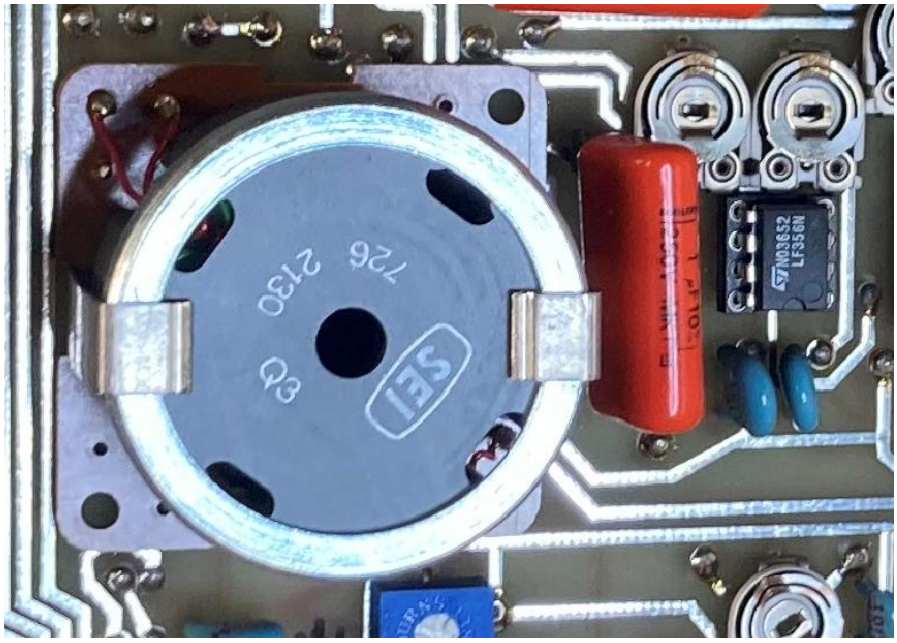

Fig. 5.3.4.2 A ferrite pot core

It appears that the connections to the mutal inductor (via JQ1 31a and 31c) first go through the amplifier/filter PCB (null detector PCB1: JA1 31a and 31c). There is probably another connector on PCB1.

1. Part 1, monograph 6: “Low phase error capacitors and inductors”. See section 3.

5.3.5 Low-pass filters

This PCB module also has two low-pass filters. They share a 25Hz band-pass filter to create a notch at 25Hz (the main ripple component): -

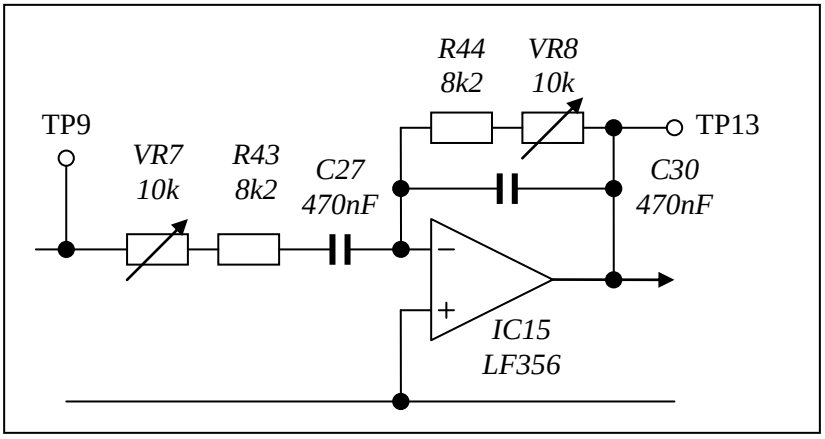

Fig. 5.3.5.1 Band-pass filter (25Hz)

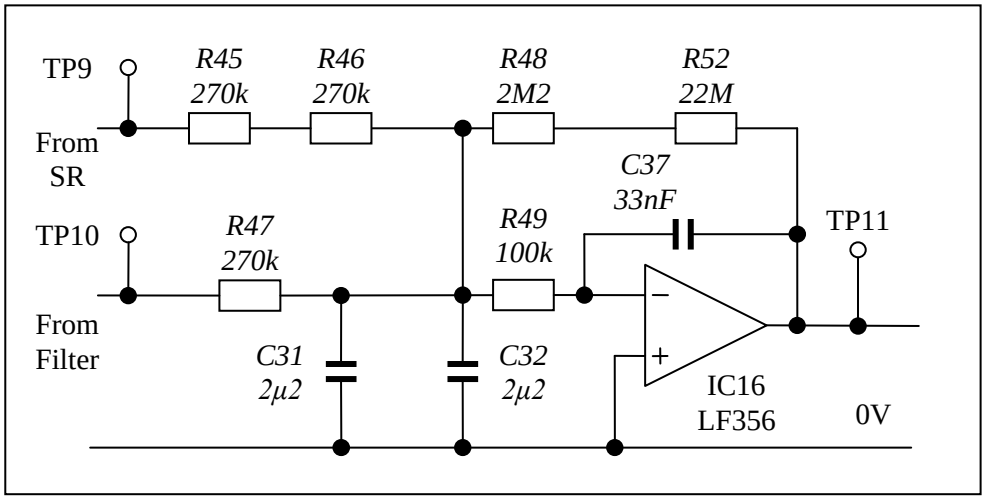

Fig. 5.3.5.2 Low-pass filter 1 (0.3Hz to the meter)

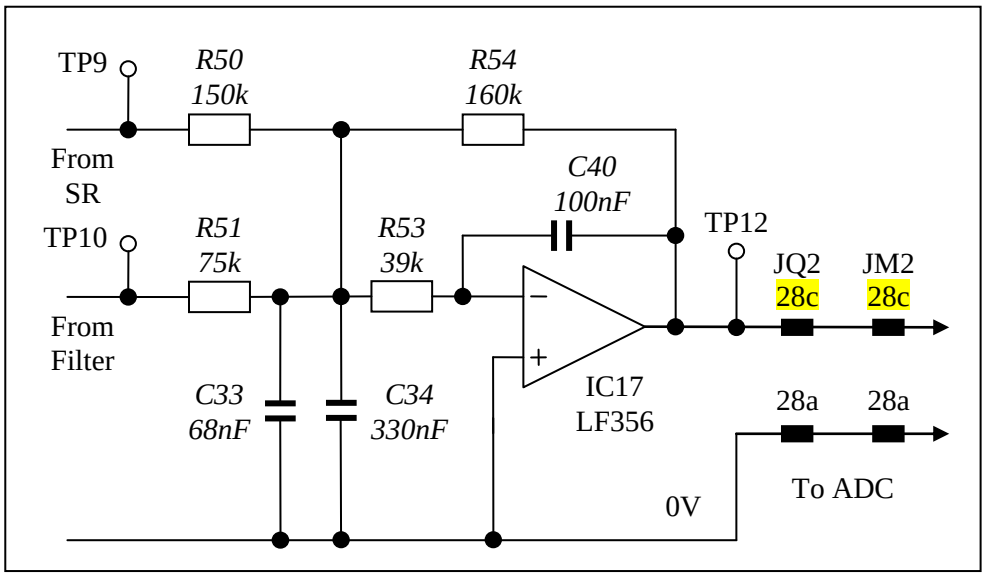

Fig. 5.3.5.3 Low-pass filter 2 (10Hz to A/D converter)

The offset trimmers for IC15, IC16 and IC17 (not shown) are *VR9, VR11* and *VR10* respectively.

5.3.6 Residual rectifier

Any AC signal (e.g. noise and interference) after the filter and amplification stages is rectified, smoothed and passed to the meter selector. The inverter stage is repeated for convenience: -

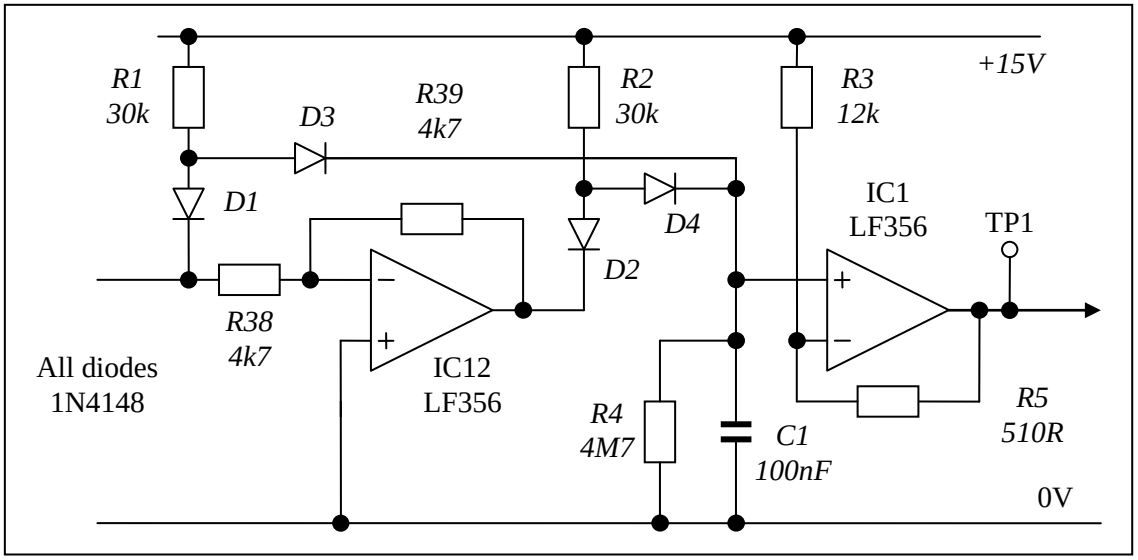

Fig. 5.3.6.1 Residual rectifier

5.3.7 Meter selector

Analogue switch (IC18: CD4053) selects the signal to be displayed on the moving coil meter: -

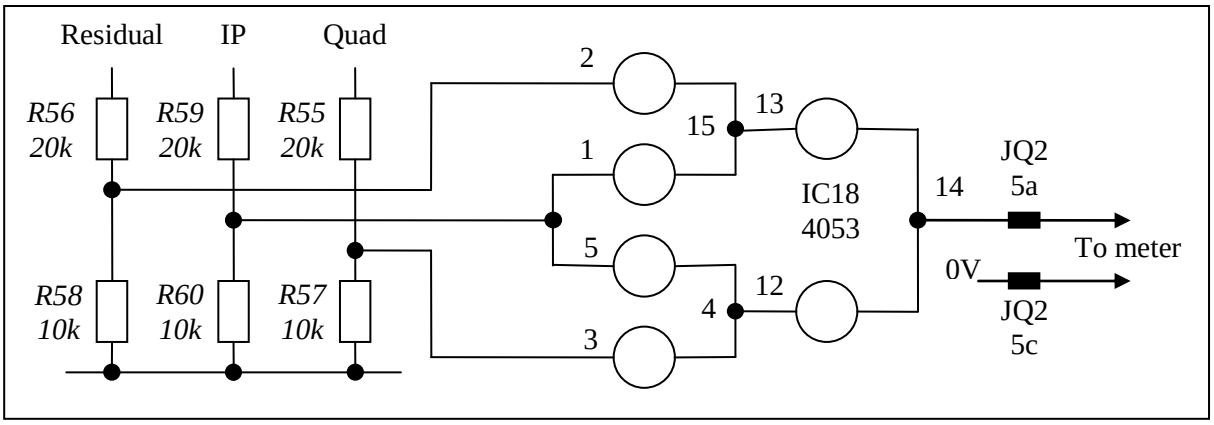

Fig. 5.3.7.1 Meter selector

Control inputs B and C (pins 10 and 9) are hard wired together with a pull-up resistor (*R62, 100k*) to 7V5.

Control input A (pin 11) also has a pull-up resistor (*R61, 100k*).

The truth table is as follows: -

C & B (pins 9 &10)	A (pin 11)	Mode
0	0	In-phase
0	1	Residual
1	0	Quad
1	1	In-phase

For more detail on the interface from the microcontroller PCB see section 5.4.

5.3.8 Differential switched gain stage

The reference voltage, at the outputs of the high accuracy voltage followers (HAVF1 and HAVF2), is amplified (×5.1, ×51 or ×510) depending on the gain selected: -

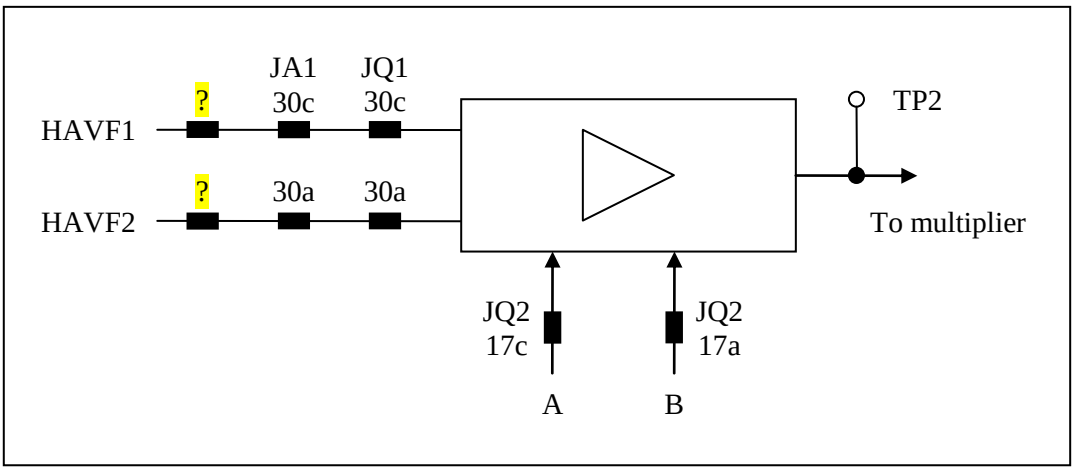

Fig. 5.3.8.1 Differential switched gain stage

The offset trimmer for IC3 (not shown) is *VR1*.

The input arrives via the amplifier/filter PCB (connector JA1). It must have another connector for connections to the followers.

Control inputs A and B (pins 10 and 9) have pull-up resistors (*R66* and *R67*, *10k*) to 7V5.

The truth table is as follows: -

B (pin 9)	A (pin 10)	Gain
0	0	×5.1
0	1	×5.1
1	0	×51
1	1	×510

For more detail on the interface from the microcontroller PCB see section 5.4.

For more theory on this circuit see the relevant monograph [1].

1. Part 4, monograph 3: “High accuracy amplifiers, integrators and differentiators”. See section 6.3.

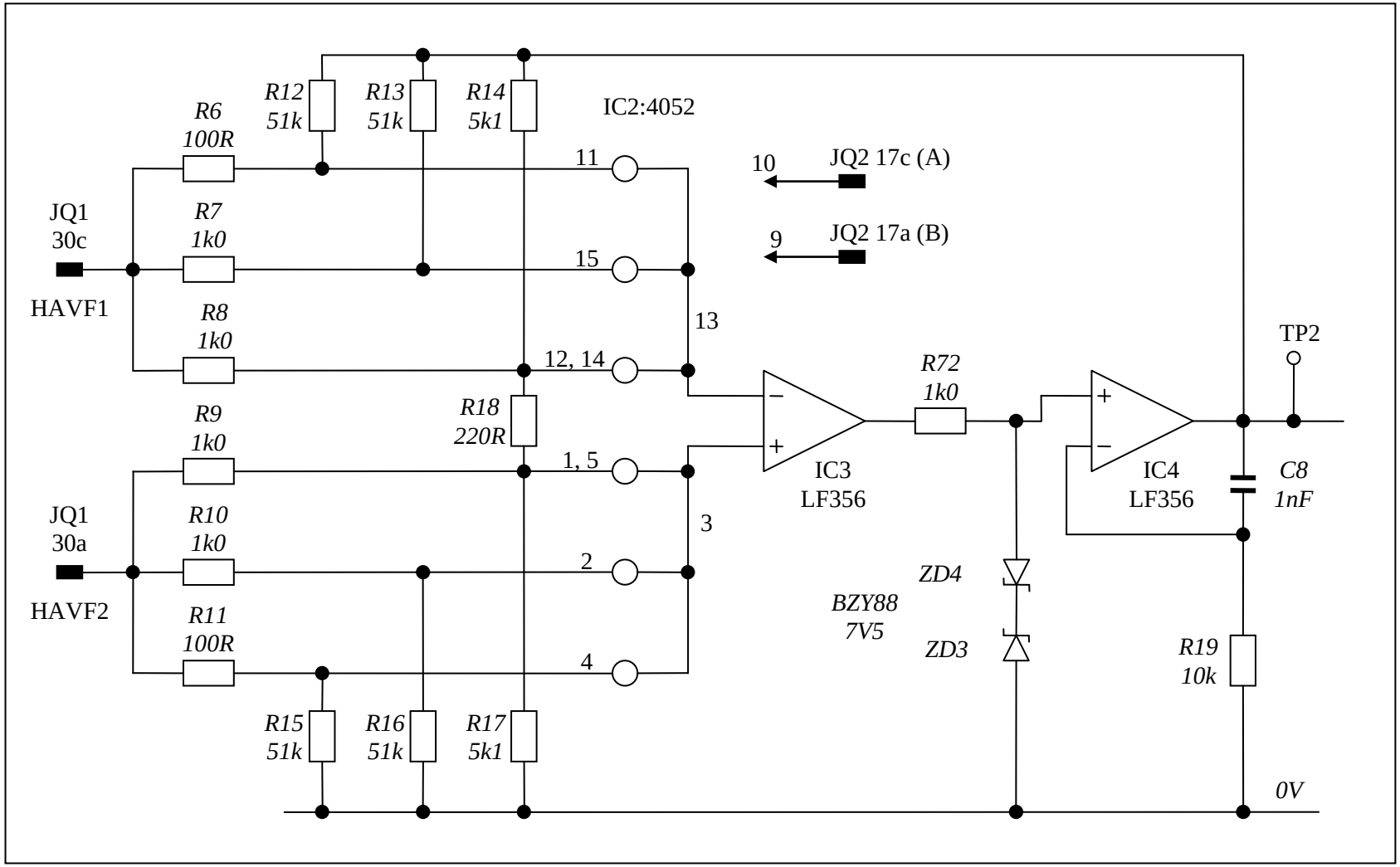

Fig. 5.3.8.2 Differential switched gain stage

The offset trimmer for IC3 (not shown) is *VR1*.

5.3.9 Inverter 2

A second inverter provides the input to the next stage - a synchronous rectifier/low-pass filter combination: -

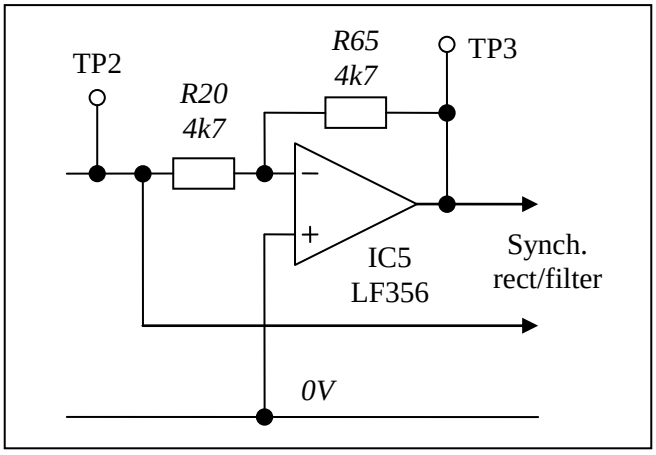

Fig. 5.3.9.1 Inverter INV2

The offset trimmer for IC5 (not shown) is *VR2*.

5.3.10 Synchronous rectifier/low-pass filter

The amplified reference voltage is rectified (in-phase) and smoothed before being sent to the ADC on the microcontroller PCB: -

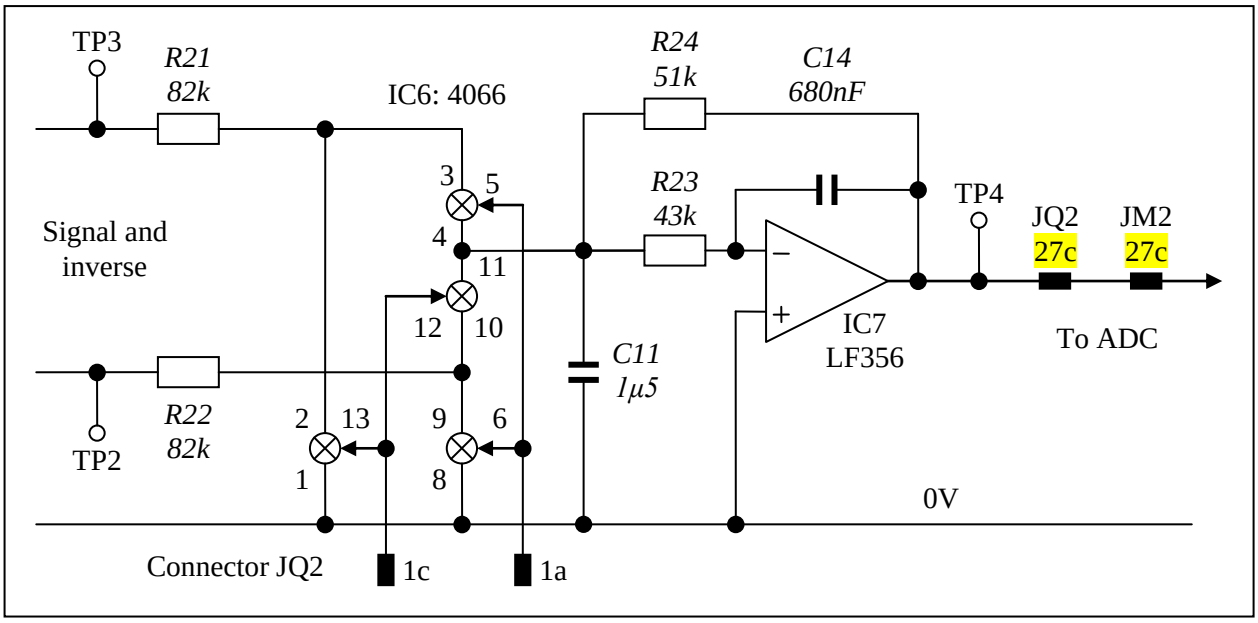

Fig. 5.3.10.1 Synchronous rectifier/low-pass filter

The offset trimmer for IC7 (not shown) is *VR3*.

5.3.11 Overload detectors

This PCB also has two overload detector circuits. The first is for residual (noise and interference) after the amplification and filtering stages (PCB1) but before the synchronous rectifiers: -

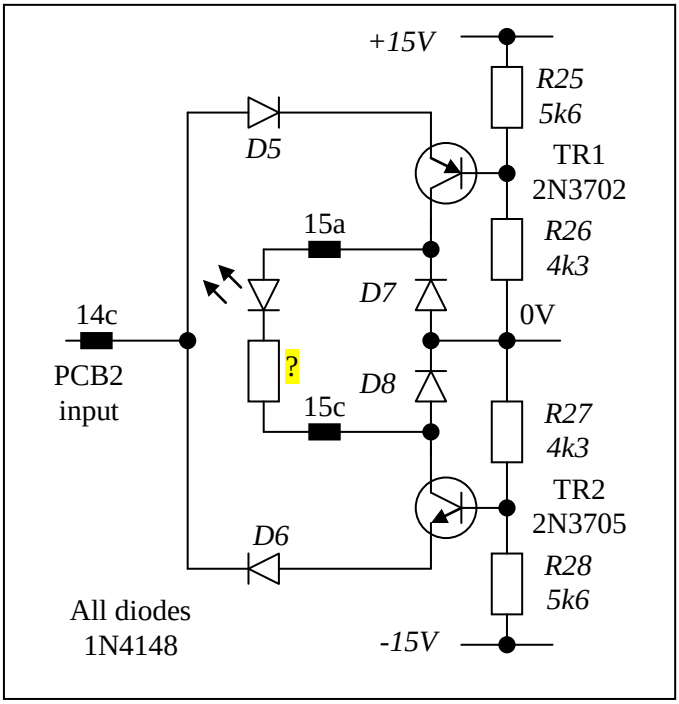

Fig. 5.3.11.1 Residual overload detector circuit

The overload condition is when the input voltage exceeds (approx.) ±8V. The outputs are via connector JQ2.

The second monitors the (DC) output of the integrator (TP5): -

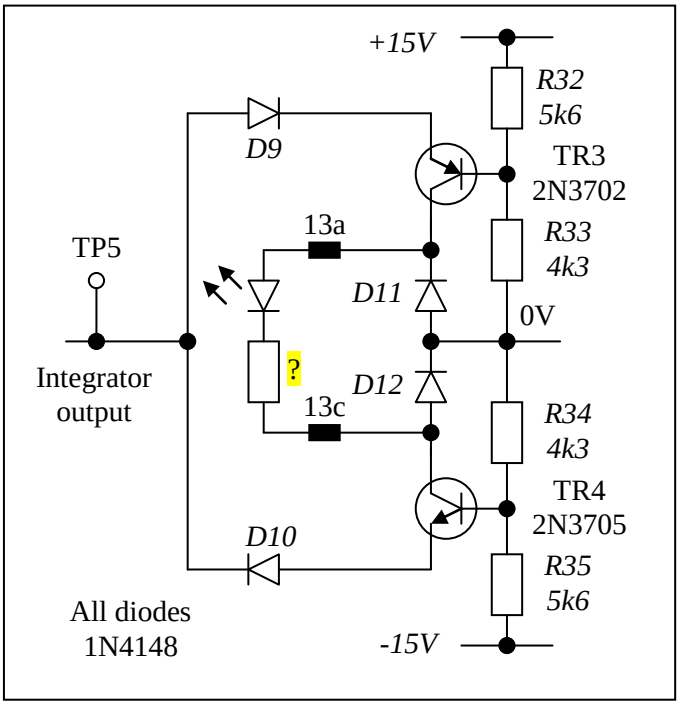

Fig. 5.3.11.2 Quadrature overload detector circuits

For more detail on the (opto-coupled) interface to the microcontroller PCB see section 5.4. There appears to be no resistor in series with the photodiode.

5.4 Interface circuits

The meter select control signals are produced by the microcontroller PCB (slot 2 of the card frame, connectors JM1 and JM2) and reach the synchronous rectifier/quad servo PCB (slot 5, connectors JQ1 and JQ2) via the interface PCB (slot 3, connectors JI1 and JI2): -

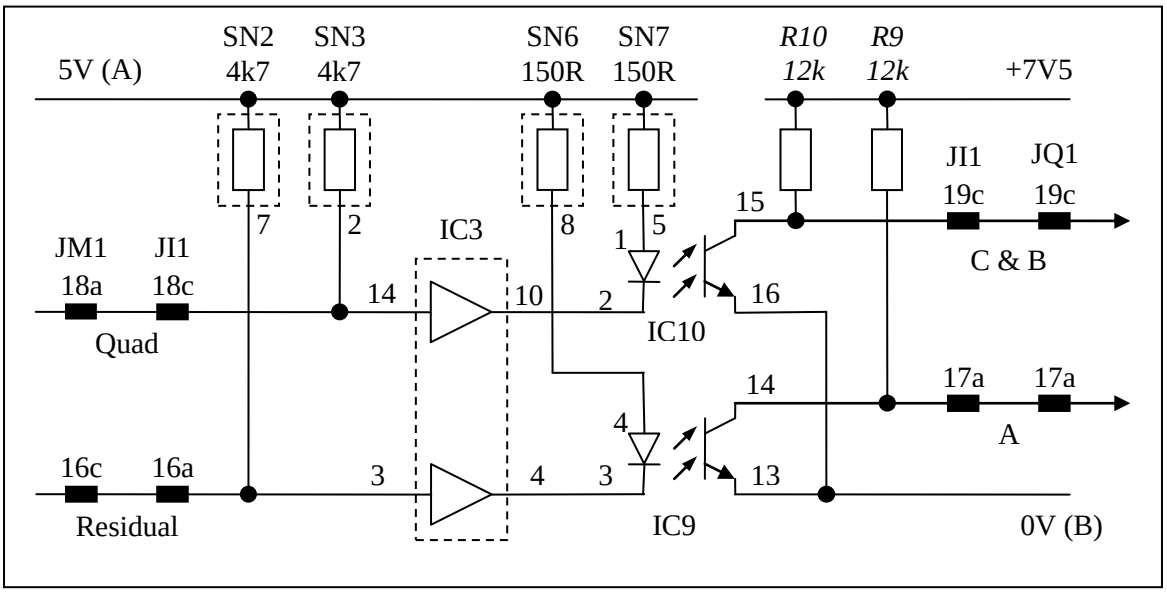

Fig. 5.4.1 Meter select interface

See section 5.3.7. The truth table is repeated for convenience: -

C & B (pins 9 &10)	A (pin 11)	Mode
0	0	In-phase
0	1	Residual
1	0	Quad
1	1	In-phase

Similarly for the reference voltage differential amplifier gain selection. See section 5.3.8: -

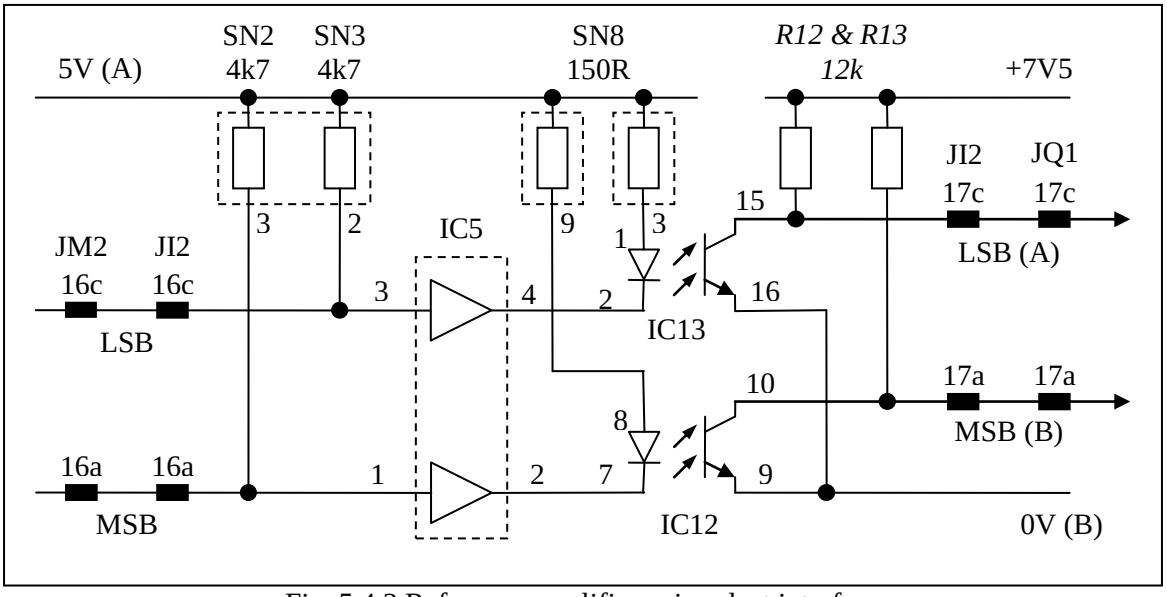

Fig. 5.4.2 Reference amplifier gain select interface

The interface from the overload detectors (see section 5.3.11) to the microcontroller PCB is as follows: -

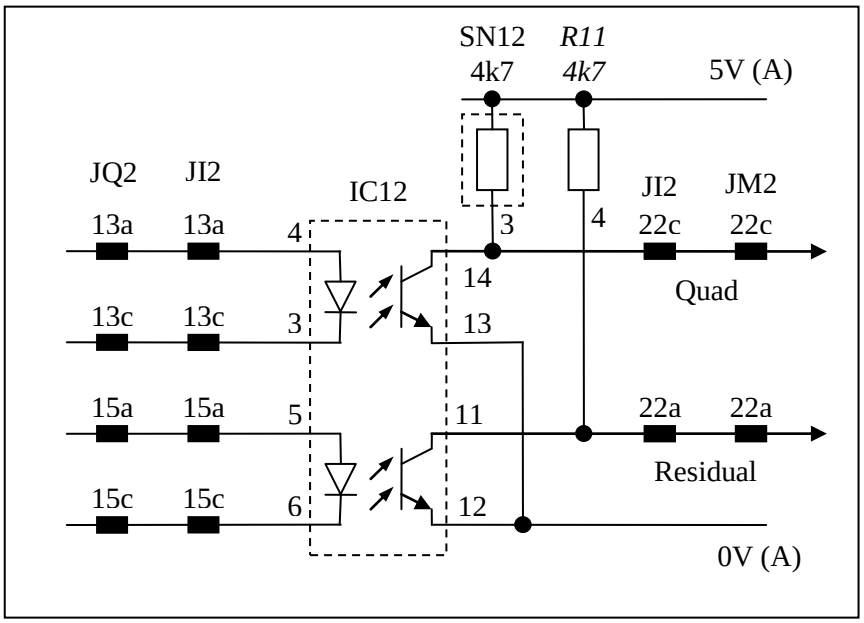

Fig. 5.4.3 Overload detector interface

There appears to be no resistor in series with the photodiode.

The ouptuts from null detector PCB2 can be traced through the analogue switch selector (IC11: DG508) to the input of the analogue to digital converter. For some reason the 0V local to the bridge out-of-balaance (V_{OOB}) and the 0V local to the rectified reference voltage (V_{REF}) are also connected to analogue channels: -

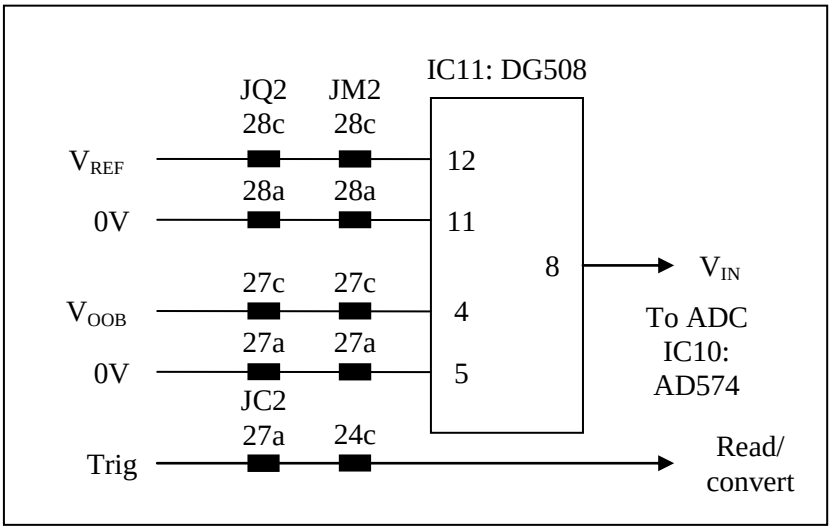

Fig. 5.4.4 Interface between the null detector and ADC.

The connector pin allocation above was taken from the micro circuit diagram. It differs on the backplane diagram.

The control lines can also be traced to the input/output ports on the microcontroller PCB (slot 2).

The meter select lines originate from IC8 (8255) port C: -

Control	Port	Pin	JM1	JI1 (input)	JI1 (output)	JQ1 (input)
Quad	C0	14	18a	18c	19c	19c
Residual	C1	15	16c	16a	17a	17a

The reference amplifier gain select lines originate from IC9 (8255) port C: -

Control	Port	Pin	JM2	JI2 (input)	JI2 (output)	JQ2 (input)
MSB	C7	10	16a	16a	17a	17a
Residual	C6	11	16c	16c	17c	17c

The overload signals arrive at IC9 (8255) port B: -

Overload	JQ2 (output)	JI2 (input)	JI2 (output)	JM2 (input)	Port	Pin
Quad	13a & 13c	13a &13c	22c	22c	B7	22
Residual	15a & 15c	15a & 15c	22a	22a	B5	23