# Check the 0-TC point in your FETs.

## Experiments show that theoretical values of bias current for 0-TC are not accurate.

A zero-temperature-coefficient (0-TC) point that is inherently present in junction- and MOS-FETs is the devices' ideal operating point because no changes due to temperature take place there.

The theoretical explanation of this phenomenon is already well documented.[1, 2, 3, 4, 5] Experience shows, however, that theoretical expressions cannot be relied on for detailed circuit design. In fact, to use the 0-TC point in practical circuits, a designer must determine it for every FET type, and, quite often, for each FET of the same type.

The purpose of this article, then, is to describe the 0-TC measuring techniques, to present test data for several commercially available FETs, and to review briefly applications where the 0-TC point can be used advantageously.

### Theoretical model may give imprecise results

The temperature variation of drain current in J-FETs is largely due to two opposing factors. The first is the change in width of the thermally generated depletion layer at the gate-channel junction. The second is the majority-carrier mobility between the source and drain.

In the references cited above it is shown that the first factor tends to increase the drain current at a rate equivalent to a change of 2.2 mV/°C at the gate. The second factor tends to decrease the gate current at a rate of approximately 0.7%/°C.

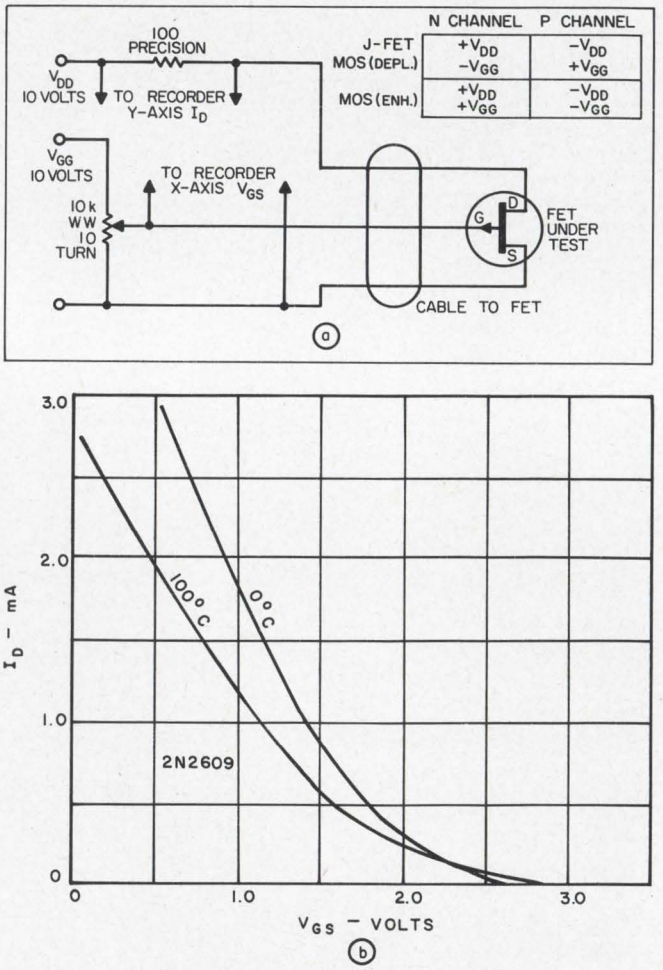
These two factors combined result in the following equations:[1]

$$I_{DZ}=0.4\,I_{DSS}/V_p^2=\textit{drain current for zero TC} \quad (1)$$

$$V_{GSZ}=V_p-0.63=\textit{gate-source voltage for zero TC} \quad (2)$$

These equations, having been developed from a theoretical model, often do not give correct results in practice. The semiconductor doping and diffusion account for most of the differences between the actual and theoretical results. Of the two foregoing equations, the first is the more meaningful because the result, $I_{DZ}$, is independent of the drain-to-source voltage. $V_{GSZ}$, on the other hand, is dependent on the drain-to-source voltage, a variable known only in the final circuit configuration.

From practical considerations, therefore, the best way to establish the 0-TC point is experimentally. $I_{DZ}$, being a unique value, should be determined first. A second test should then be performed to determine $V_{GSZ}$ at $I_{DZ}$ and the proper drain-to-source voltage. The 0-TC point can be determined easily by making a plot of $V_{GS}$ vs $I_D$ for various temperatures, using the circuit shown in Fig. 1a. The equipment needed is an X-Y recorder, two




1. **0-TC point of a FET** can be quickly determined using a simple test setup (a). A sample curve (b) has been obtained for the 2N2609 FET.

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low-voltage dc supplies, and an environmental oven. A ten-turn potentiometer is used to control the gate-to-source voltage so that a smooth curve is produced on the X-Y recorder. A sample $V_{GS}$-vs-$I_D$ plot of a p-channel FET is shown in Fig. 1b. In lieu of using an oven, a simpler and possibly quicker method would be the use of ice water and boiling water. This method would produce both an accurate temperature reference and a very good heat sink.

It is frequently impractical to bias the FET at exactly $I_{DZ}$. In order to determine the temperature drift errors at other drain currents, a plot similar to that of Fig. 2 can be used. It was developed by determining graphically the drift at various drain currents with the $V_{GS}$-vs-$I_D$ plot of Fig. 1b. It can be seen that for moderate drift requirements (less than 1 mV/°C) the J-FET is well behaved over a wide range of currents.

A large spread in $I_{DZ}$ values often occurs from one sample to the next of a particular type of J-FET. This is a result of the many device conditions that affect $I_{DZ}$. When production requirements necessitate a specific $I_{DZ}$, the J-FETs can usually be specially ordered from a manufacturer.

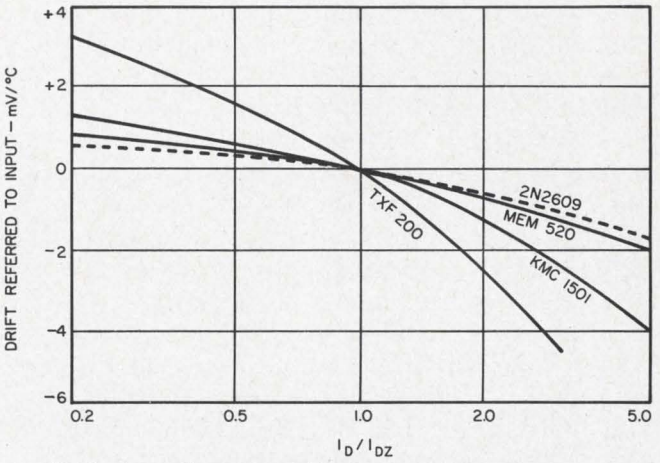
### MOS-FET characteristics are hard to determine

The temperature dependence of MOS-FET characteristics is much more difficult to define than that of J-FETs'. For this reason, an easily handled mathematical model has not as yet been developed. One of the most difficult factors to control in MOS-FET fabrication is the interface structure between the silicon drain-source channel and the silicon dioxide gate insulator. Large changes in the surface properties of the transistor are to be expected as a result of variations in cooling rate, in atmospheric purity, and in general cleanliness during the formation of the gate insulator.

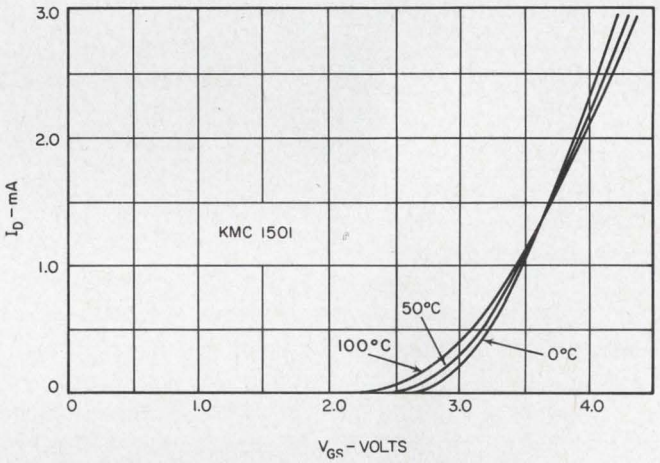
A theoretical explanation of the temperature-dependent properties can, however, be made.[2] It can be theorized that there is a particular drain current for which a 0-TC exists. But in practice, this drain current, $I_{DZ}$, is impossible to predict and requires experimental determination.

The same method outlined for J-FETs can be used to determine the 0-TC point of MOS-FETs experimentally. Fig. 3 shows the results of a temperature-dependent $V_{GS}$-vs-$I_D$ plot for a p-channel enhancement-mode MOS-FET. For a closer analysis of the 0-TC point, it is advantageous to use zero suppression in the X-Y recorder. This quickly demonstrates nonlinearities (Fig. 4).

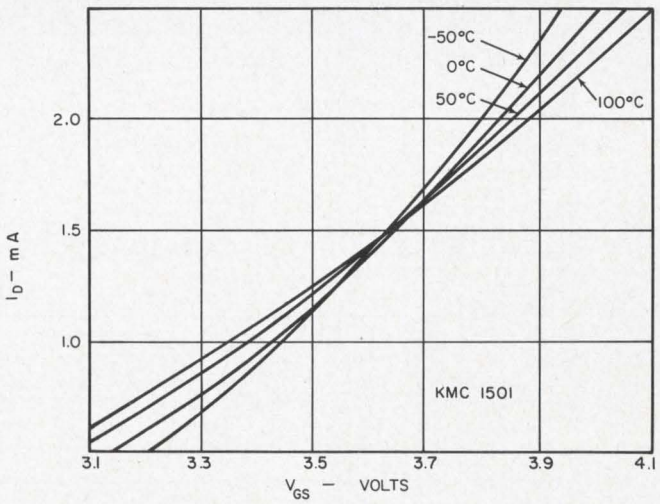
One problem seldom admitted, yet sometimes encountered, is sodium ion drift.[3] This can complicate the search for a 0-TC point because the gate voltage may not be a true indication of drain current. The ion drift rate is very temperature-




2. **Maximum allowable drift** for condition when a FET must be biased at an $I_D$ different from $I_{DZ}$ can be determined from the data of Fig. 1b. Devices of four manufacturers were used for this photo.




3. **MOS-FETs also possess a 0-TC point,** as can be seen from the plot above. Yet it is more difficult to predict and may vary from unit to unit. The existing theoretical models are not accurate.




4. **A blown-up view of the 0-TC** shown in Fig. 3, obtained through zero suppression in the X-Y recorder, demonstrates the nonlinearities in the $V_{GS}$-vs-$I_D$ plot. Note the large variations in $I_D$.

dependent. At 100°C the mobility of sodium ions through the silicon dioxide gate insulator is many times greater than at room temperature. The magnitude of the drift is vividly portrayed in Fig. 5, a plot of the drain current versus time. This defect is present in varying degrees in all MOS-FETs presently manufactured and depends on the purity of the manufacturing conditions. The problem can be alleviated by first making the $V_{GS}$-vs-$I_D$ plot at the highest temperature after the drift has gone to its limit under biased conditions; then, while maintaining the gate bias voltage, cooling the device down for its lower-temperature runs. The result will be a true indication of $I_{DZ}$ alone, if a significant drift is present.

Most MOS-FETs that were tested possessed a 0-TC point. Several units checked are listed below with their approximate $I_{DZ}$:

| | | |
|---|---|---|
| Sprague | TXF200 | 50 μA |
| Fairchild | FI100 | 100 μA |
| General | MEM520 | 0.5 mA |
| Instrument | MEM551 | 0.5 mA |
| KMC | 1501 | 1.5 mA |
| TRW | 2N4308 | 2.5 mA |
| Siliconix | 2N3631 | 4.0 mA |

Because of variations in the manufacturing conditions, however, these approximate values must not be relied on as constant.

MOS-FETs, as a rule, will not perform as well as J-FETs under wide ranges of temperature because of the complex temperature compensation present at the 0-TC point. Of the types tested, the General Instrument MEM520, MEM 551 and the KMC 1501 exhibited the most stable 0-TC point over a temperature range of 0°C to 100°C.

## Where to use FETs

J-FETs offer the widest latitude in design because of the diversity of the types available. Since the transconductance, $g_m$, of a FET is proportional to the drain current, high gain in conventional circuitry requires the J-FET's $I_{DZ}$ to be near its $I_{DSS}$. From Eq. 2, $V_p$ must be about 0.63 volt if $I_{DZ}$ is to equal $I_{DSS}$. Devices such as the Union Carbide 2N3687 and 2N3698 satisfy this requirement. Equation 1 shows that low $I_{DZ}$ operation can be obtained from J-FETs that have a $V_p$ of 4 to 6 volts. However, the stage gain will suffer unless techniques like that shown in Fig. 6 are used. In this application, a constant-current load at $I_{DZ}$ is used to give the highest possible stage gain. A temperature-compensated power supply regulator combination (*Q1* and *CR1*) and *R1* comprise the current source. The composite stage gain can easily exceed several thousand.

The use of MOS-FETs in dc amplifiers, because of the difficulties involved, is usually limited to high-input-impedance applications. The small number of different types available often limits the circuit design. Some of the problems that have to be considered are:

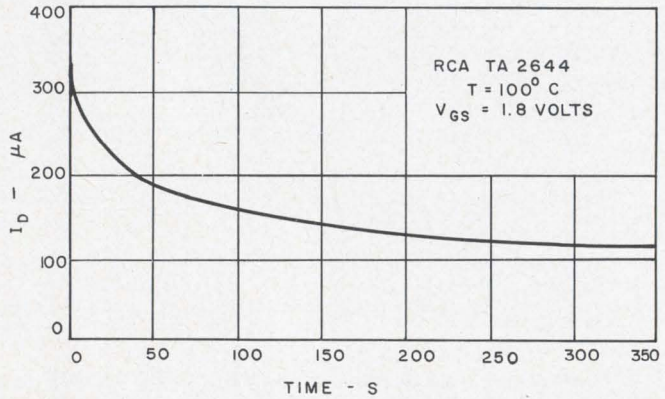
- The unpredictability of the 0-TC point.
- The 0-TC point variability with the temperature range.
- Gate voltage drift due to ion migration.

It is therefore necessary to design the circuit around the device once the MOS-FET's limitations have been thoroughly investigated.

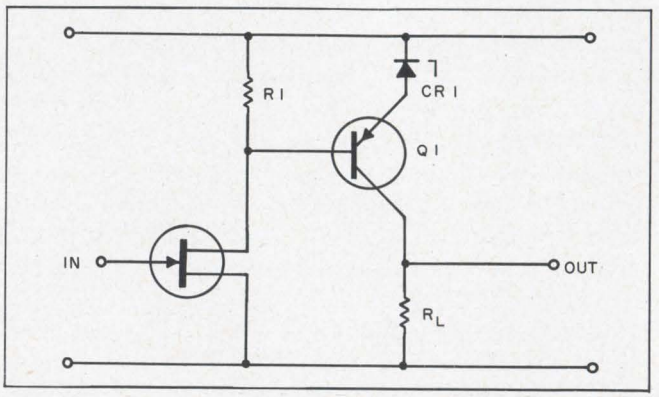
Large-swing open-loop dc amplifiers should be avoided. This is to prevent drift errors when a signal causes operation at a point far removed from the $I_{DZ}$ value. The magnitude of this drift error can be calculated with a curve similar to those in Fig. 2. The effects of drift can be reduced by limiting 0-TC biased FET stages to low signal levels or by going to closed-loop operation. Closed-loop amplifiers are the best approach since they have the advantage of reducing the drift error by the loop gain.

## FETs for amplifiers and current sources

The FET version of the differential amplifier poses a problem (absent with transistors) because




5. **Drift due to the sodium ion migration** is demonstrated in this graph. This effect renders theoretical predictions of FET behavior very difficult.




6. **Stage gain of several thousands** can be obtained by "feeding" the FET from a simple constant-current (equal to $I_{DZ}$) source.

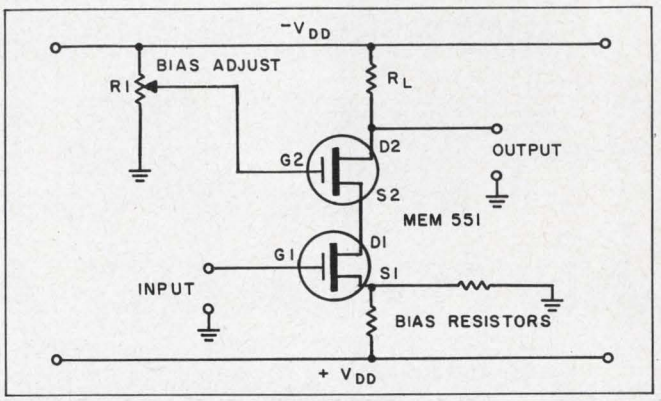
of the 0-TC point. When a dc signal is applied to a 0-TC biased differential FET stage, differential drift errors will occur. These drift errors, which appear only when a signal is applied, are caused by one FET operating above, and the other operating below, the 0-TC bias point. To reduce dynamic-differential drift errors, the bias points should be a little below the 0-TC values, depending on the signal swing. This can be deduced from an analysis of the curves of Fig. 2. If high input impedances are not required, a good differential transistor such as the 2N4044 should be used instead of a FET.

It has been implied that the operating point of a FET preceding a transistor can be adjusted to compensate for the drift in the transistor. A circuit of this nature should not be designed for production-line fabrication, however, because of the setup time required. Each circuit has to be individually trimmed to minimize drift, since drift rates of the FET and transistor vary from unit to unit.

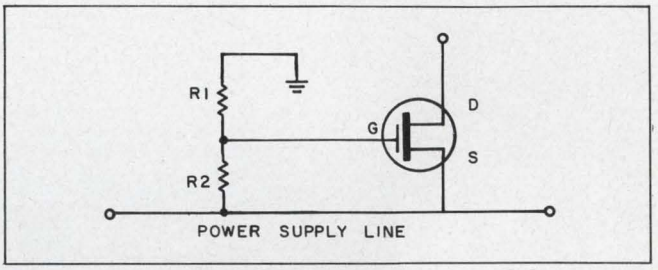
MOS-FETs can easily be adapted for use in a dc-coupled cascode amplifier. Because of the compound connection, both MOS-FETs should have nearly the same 0-TC point. Rather than match two units that have the same 0-TC point, use a dual-monolithic MOS-FET. Tests were performed on a General Instrument MEM551 dual unit to verify the similarity between the 0-TC points of each MOS-FET. On the whole, they were virtually identical. When properly biased in the circuit, as shown in Fig. 7, the result is an exceptionally stable dc-input amplifier.

Due to the constant-current nature of FETs in the pinch-off region, they lend themselves to use as simple current sources. When using J-FETs for this application, a low $V_p$ is desirable. This will minimize the voltage drop for current-limiting in the circuit of Fig. 7. *R1* can be adjusted to produce the $I_{DZ}$ current. Enhancement-mode MOS-FETs make simple current sources in the circuit of Fig. 8. The ratio of *R1* and *R2* can be adjusted to give the proper current level. The big advantage of FET current sources over conventional transistor-Zener combinations is their low minimum voltage drop for current-limiting.

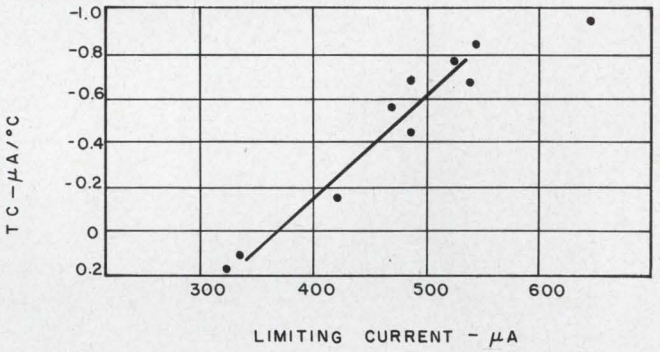
Motorola is producing a series of current-limiting diodes (type number MCL 1300) that are actually J-FETs with gate and source shorted. When FETs are used in this configuration, $I_{DSS}$ current is limited. If these current-limiting diodes are to have a 0-TC current level, the J-FET used must have a $V_p$ of about 0.63 volt. Since no data on temperature stability were supplied, tests were run on enough diodes to verify the possible existence of $I_{DZ}$ current level. The results, shown in Fig. 9, indicate that the $I_{DZ}$ current level exists at approximaely 0.37 mA. Motorola can supply diodes selected to this current at an additional cost. All the same, of course, this particular $I_{DZ}$ value will vary, depending upon the manufacturing control. ■ ■




7. **Stable single-ended dc amplifier** results when a dual MOS-FET unit is used.




8. **Enhancement-mode MOS-FET** can be used to build a simple constant-current source.




9. **Tests on a number of current-limiting FET diodes** indicate that they also possess 0-TC points. They can be obtained on special orders only.


**References:**

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