# On the Output Resistance of Self-Checking Voltage Dividers

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*Abstract*—**This paper deals with the computation of the variable output resistance of Cutkosky's self-checking binary voltage divider. For an $N$-bit divider, the maximum output resistance was found to increase with $N$ at the rate of $N/9$ times the divider's characteristic input resistance. To increase the divider's resolution while limiting its output resistance, a binary potentiometer as a termination is suggested.**

## INTRODUCTION

THE SWITCHING technique for binary voltage divisions put forward by Cutkosky promises divider accuracies around $1 \times 10^{-7}$ of input [1]. At the National Research Council of Canada, a microcomputer-based 13-bit prototype reference divider has been built and tested [2]. It is found to be as accurate as expected if external loading of the divider's output is fully accounted for.

This paper examines the output resistance of such a divider. Like the Kelvin–Varley divider, the Cutkosky divider has a constant input resistance ($R_{in}$), and a variable output resistance ($R_{out}$). In contrast, however, its $R_{out}$ can exceed its $R_{in}$ when the number of binary divisions $N$ is larger than 8. Although this $R_{out}$ varies over a wide range of values, it can be computed for any particular setting of the divider. To increase the resolution of this divider by simply adding more binary stages will lead to an unacceptably high output resistance. To limit this $R_{out}$, it is proposed that the Cutkosky divider be terminated with a different type of self-checkable binary divider circuit, such as a "binary potentiometer."

## COMPUTATION OF OUTPUT RESISTANCE

Fig. 1 shows a characteristic Cutkosky divider where all the dropping resistors have been normalized to 1 Ω, and all the load resistors, 2 Ω, with the exception of the terminating one of 1 Ω. For an $N$-bit divider, the states of the $N + 1$ switches can be represented by a switch code $S = (S_0 S_1 \cdots S_N)$ of $N + 1$ bits. From $S$, a corresponding code $D = (D_0 D_1 \cdots D_N)$ can be constructed by setting $D_0 = S_0$ and $D_i = S_i \oplus D_{i-1}$ $(i \neq 0)$. This $D$ code represents the down/up location of each of the dropping resistors. For instance, if switches 2 and 3 of the 4-bit divider have been set to 1 (Fig. 2(a)), we have

$$S = 00110$$

and

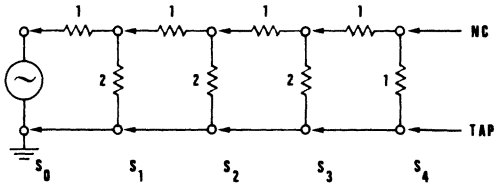


Fig. 1. A characteristic Cutkosky divider. Divider sections are cascaded by means of DPDT switches, $S_n$, represented here by pairs of reversing contacts. As shown, all resistances are normalized and all switches are in the "zero" state.

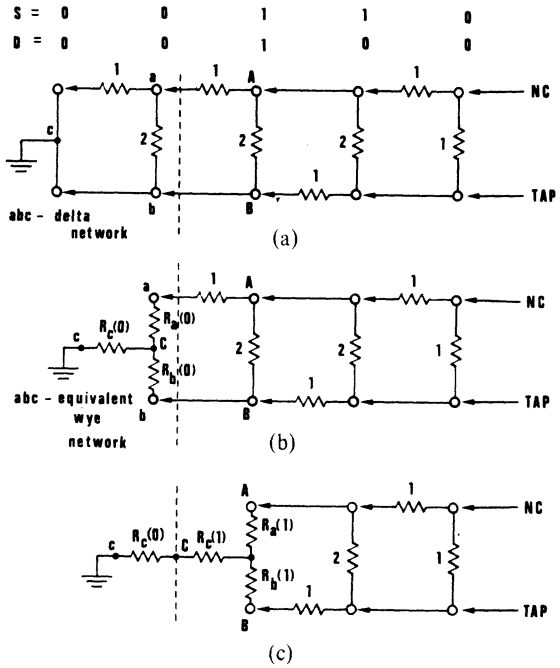


Fig. 2. Equivalent circuits (a) used for computing the output resistance of a 4-bit divider with switch setting $S$ = 00110, (b) after one delta-wye transformation, and (c) after two delta-wye transformations.

$$D = 00100.$$

The $R_{out}$ of the divider can be computed for any given setting using the $D$ code as the basis for analysis. Starting from the most significant section, one first locates the dropping resistor in either the down or up branch of the delta network in accordance with $D_0$, and then transforms that into an equivalent wye network of resistors $R_a(0)$, $R_b(0)$, and $R_c(0)$ (Fig. 2(a) and (b)). By inspection, one can write

$$R_a(0) = 2(1 - D_0)/3 \quad (1)$$

$$R_b(0) = 2(D_0)/3 \quad (2)$$

Manuscript received June 3, 1983; revised August 10, 1983.

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0018-9456/83/1200-0469$01.00 

and

$$R_c(0) = 0/3. \quad (3)$$

This process is repeated section by section and after the $i$th delta-wye transformation, one obtains (for $i = 1, \cdots, N-2$)

$$R_a(i) = 2[R_a(i-1) + 1 - D_i]/[3 + R_a(i-1) + R_b(i-1)] \quad (4)$$

$$R_b(i) = 2[R_b(i-1) + D_i]/[3 + R_a(i-1) + R_b(i-1)] \quad (5)$$

and

$$R_c(i) = [R_a(i-1) + 1 - D_i][R_b(i-1) + D_i]/[3 + R_a(i-1) + R_b(i-1)]. \quad (6)$$

The last two bits in $D$ can be processed together, bearing in mind that the output tap is located at either end of the 1-Ω terminating load resistor. Thus the last $R_c$ is given by a parallel combination of resistors, namely

$$1/R_c(N-1) = \{1/[R_a(N-2) + 2 - D_{N-1} - D_N]\} + \{1/[R_b(N-2) + D_{N-1} + D_N]\}. \quad (7)$$

Finally

$$R_{\text{out}} = \sum_{i=0}^{N-1} R_c(i). \quad (8)$$

The $R_{\text{out}}$ distributions for dividers of 13 and 16 bits are illustrated in Fig. 3. Fig. 4 shows the maximum $R_{\text{out}}$ as a function of $N$. Even for moderate $N$, this maximum increases by 2/9 Ω for each unit increase in $N$ (see Appendix). The characteristic $R_{\text{in}}$, on the other hand, is a constant 2 Ω for all $N$. Fig. 3 shows that for a 13-bit divider, more than 78 percent of all possible settings result in an output resistance exceeding this $R_{\text{in}}$, and that for a 16-bit divider, this percentage increases to 94. In practical terms, if the value of the dropping resistor was chosen to be 100 kΩ in order to minimize the effects of self-heating and switch contact resistance, the divider would have an input resistance of 200 kΩ. The corresponding maximum $R_{\text{out}}$ would be 311 kΩ and 378 kΩ for the 13- and the 16-bit dividers, respectively.

To preserve the high accuracy of the divider, it is necessary to compute $R_{\text{out}}$ for each setting in question, and to account for the effect of any external load on the divider. It is also notable that a change in some of the less significant bits can produce a substantial change in the output resistance of the divider. For example, a setting of $S$ = 11000000000000 gives an output resistance of 0.5 Ω, while a change to $S$ = 11000000000101 triples this $R_{\text{out}}$. Indeed, this fact can help one determine (by means of incremental measurements) the effect that a detector circuit, for instance, has on the output of the divider so that a correction can be applied. (A full discussion of this subject is beyond the scope of this paper.)

## The Terminating Potentiometer

The need for parts-per-million resolution or better is evident in many standards laboratories. However, if the divider of Fig. 1 is simply extended, its output resistance will rise accordingly.

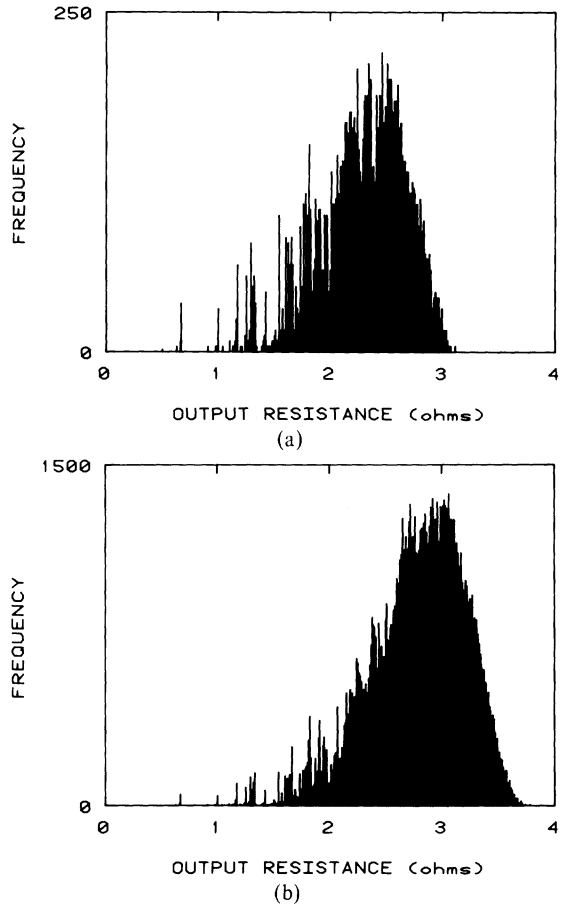


Fig. 3. Distributions of the output resistance computed with a resolution of 0.01 Ω for characteristic dividers of (a) 13 and (b) 16 bits.

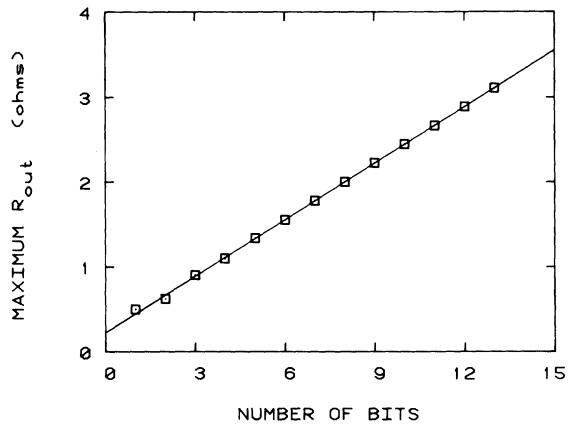


Fig. 4. Plot of the maximum output resistance of a characteristic $N$-bit Cutkosky divider.

Although the use of a suitable digital-to-analog converter for this purpose may be considered, this approach is not without its problems. It is proposed that a strictly passive analog divider be realized by terminating the Cutkosky divider with a "binary potentiometer" as shown in Fig. 5.

This potentiometer, consisting of binary weighted resistors, is itself a three-terminal resistive divider of constant input resistance. If a potentiometer of the correct input resistance is used to replace the terminating load resistor of the Cutkosky divider, increased resolution can be obtained without paying any further penalty in terms of output resistance. The exact $R_{\text{out}}$ can be computed as before, excepting that (7) will be modified to

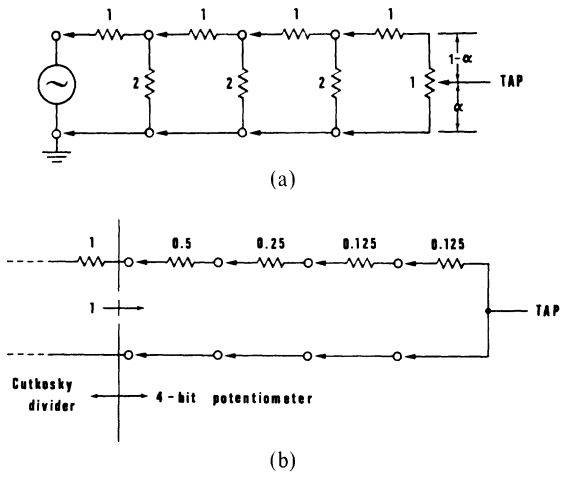


Fig. 5. (a) A characteristic Cutkosky divider terminated by a 1-Ω potentiometer. (b) Switching circuit for a 4-bit potentiometer. For clarity, DPDT switches are represented by pairs of reversing contacts.

$$1/R_c(N-1) = \{1/[R_a(N-2) + 2 - D_{N-1} - \alpha]\} + \{1/[R_b(N-2) + D_{N-1} + \alpha]\} \quad (9)$$

where $\alpha$ is the division ratio of the binary potentiometer.

In practice, a potentiometer can be made from a single commercial package consisting of a set of up to 15 individually trimmed resistors. Since this potentiometer is used in the less significant part of the divider circuit, resistor matching and switch contact requirements are less stringent. The accuracy of the potentiometer can either be self-checked or, more expediently, checked against the calibrated Cutkosky divider. Thus a 13-bit divider terminated with a 12-bit potentiometer represents a practical design that gives 25 bits of resolution ($\pm 3 \times 10^{-8}$) and offers a self-maintained accuracy approaching one least significant bit.

## Conclusion

The Cutkosky binary resistive divider provides voltage ratios that can be established readily by means of a microcomputer-based self-checking system. To achieve the highest accuracy, it has been pointed out that the effect of any loading on the divider's output must be determined and accounted for. To this end, the same microcomputer-based system is well-suited to carry out the additional computations. To strike a realistic balance between increased resolution and achievable accuracy in a passive divider, the design of a 25-bit composite divider, consisting of a 13-bit Cutkosky divider terminated with a 12-bit binary potentiometer, has been chosen for development.

Table I
Equivalent Resistances in Maximum $R_{out}$ Configuration

| Section ($i$) | $R_a(i)$ | $R_b(i)$ | $R_c(i)$ |
|---|---|---|---|
| 0 | 0.66667 | 0 | 0 |
| 1 | 0.36364 | 0.54545 | 0.18182 |
| 2 | 0.69767 | 0.27907 | 0.19027 |
| 3 | 0.35088 | 0.64327 | 0.22440 |
| 4 | 0.67643 | 0.32211 | 0.21756 |
| 5 | 0.33834 | 0.66130 | 0.22366 |
| 6 | 0.66923 | 0.33068 | 0.22128 |
| 7 | 0.33462 | 0.66535 | 0.22264 |
| 8 | 0.66732 | 0.33268 | 0.22200 |
| 9 | 0.33366 | 0.66634 | 0.22233 |
| 10 | 0.66683 | 0.33317 | 0.22217 |
| 11 | 0.33341 | 0.66659 | 0.22225 |
| 12 | 0.66671 | 0.33329 | 0.22221 |
| 13 | 0.33335 | 0.66665 | 0.22223 |
| 14 | 0.66668 | 0.33332 | 0.22222 |

## Appendix

An examination of the divider settings that gave rise to maximum $R_{out}$ showed that they were of these four forms

$$S = \begin{cases} 111\cdots111 \\ 111\cdots101 \\ 011\cdots111 \\ 011\cdots101. \end{cases}$$

The associated $D$ codes would consist of alternating 1's and 0's. Following the terminology used in the text, values of $R_a(i)$, $R_b(i)$, and $R_c(i)$ for the first 15 sections were computed (Table I) for $D = 01010101\cdots$. It is apparent that for large $i$, $R_a(i) + R_b(i) = 1\ \Omega$ and that a ratio of 2:1 exists for these two resistors. Significantly, $R_c(i)$ approaches $0.222\cdots\ \Omega$ as a limit. These results clearly indicate that for all practical purposes, the maximum value of $R_{out}$ increases by $2/9\ \Omega$ for each unit increment in $N$, as shown in Fig. 4.

## References

[1] R. D. Cutkosky, "A new switching technique for binary resistive dividers," *IEEE Trans. Instrum. Meas.*, vol. IM-27, pp. 421-422, Dec. 1978.

[2] S. H. Tsao, "Microcomputer-based calibration systems for variable voltage dividers," *IEEE Trans. Instrum. Meas.*, vol. IM-32, pp. 169-173, Mar. 1983.