

i.MX RT1024 LQFP-144 pin multiplexing

One row per package pin of the MIMXRT1024DAG5B (20 × 20 mm LQFP-144), with the function and pull it has at reset, whether the boot ROM samples it, and every IOMUXC alternate function.

Pin labels

Pad name, then the function at power-on reset (green for a GPIO, blue otherwise), the reset pull, and for boot straps the BOOT_MODE/BOOT_CFG bit latched at POR_B.

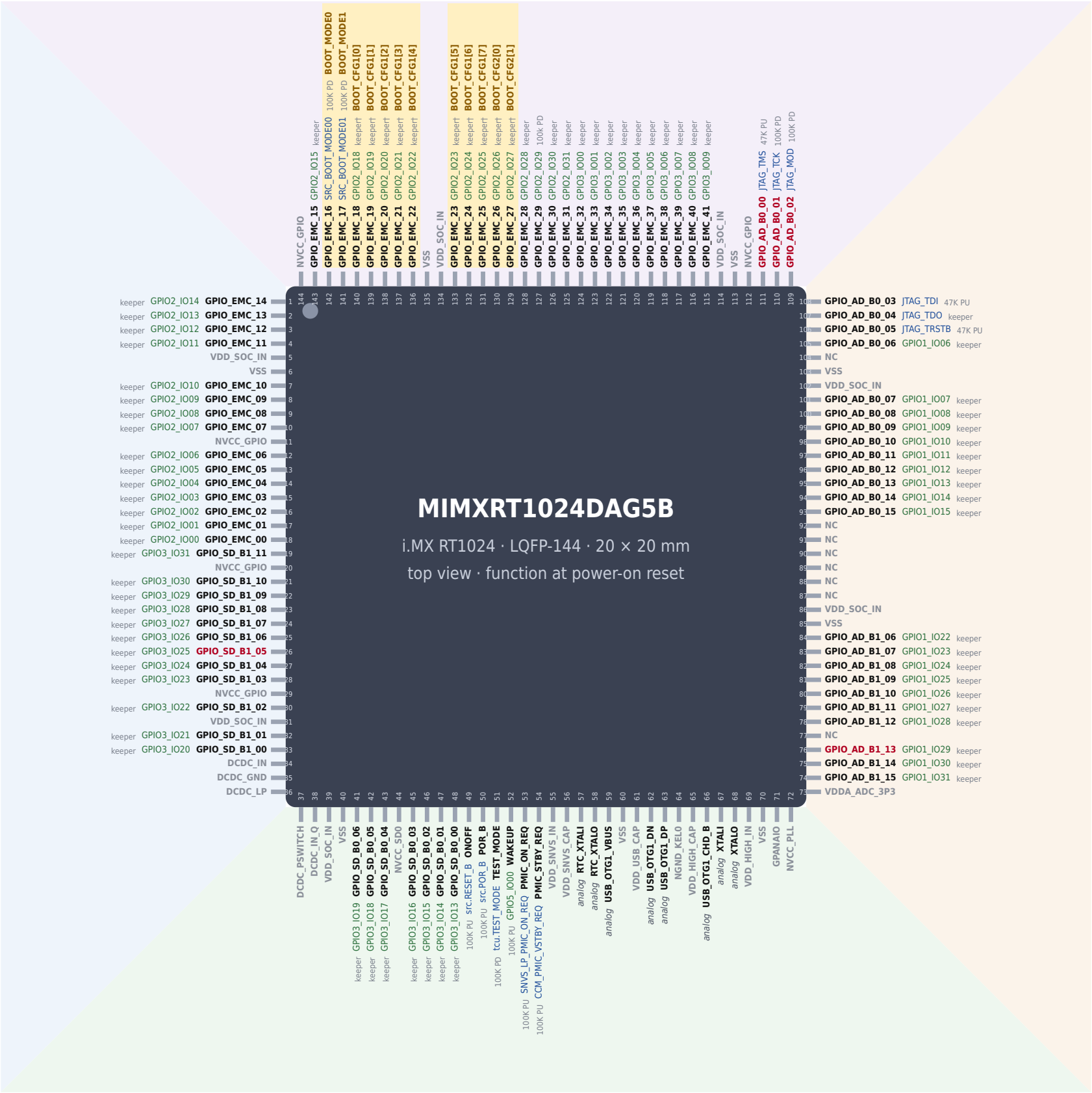
Pulls

keeper, 100K PD, 47K PU, 100K PU. † Table 82 gives a keeper and Table 68 a 100K pull-down; fit external straps.

Sides

Each side has its own tint, and the table on the following pages uses the same tint, one page per side in pin order.

Colours: left bottom right top boot strap (sampled at POR_B) supply / NC analog restricted pad (pins 26, 76, 109-111; see Notes) GPIO function



 Left side, pins 1-36 (top to bottom)

Pin	Pad	Reset function	Reset pull	Pull config	Boot sample	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1	GPIO_EMC_14	ALT5 GPIO2_IO14 (input)	Keeper	yes		SEMC_BA1	XBAR1_INOUT14	LPUART6_CTS_B	SAI1_RX_BCLK	LPSPi2_PCS1	GPIO2_IO14	FLEXCAN1_TX	
2	GPIO_EMC_13	ALT5 GPIO2_IO13 (input)	Keeper	yes		SEMC_BA0	XBAR1_INOUT13	LPUART6_RX	SAI1_RX_DATA00	LPSPi2_SDI	GPIO2_IO13	FLEXPWM2_PWMX03	CCM_PMIC_RDY
3	GPIO_EMC_12	ALT5 GPIO2_IO12 (input)	Keeper	yes		SEMC_CS0	XBAR1_INOUT12	LPUART6_TX	SAI1_TX_DATA00	LPSPi2_SDO	GPIO2_IO12	FLEXPWM2_PWMX02	
4	GPIO_EMC_11	ALT5 GPIO2_IO11 (input)	Keeper	yes		SEMC_RAS	XBAR1_INOUT11	LPI2C4_SCL	SAI1_TX_BCLK	LPSPi2_PCS0	GPIO2_IO11	FLEXPWM2_PWMX01	
5	VDD_SOC_IN	supply											
6	VSS	supply											
7	GPIO_EMC_10	ALT5 GPIO2_IO10 (input)	Keeper	yes		SEMC_CAS	XBAR1_INOUT10	LPI2C4_SDA	SAI1_TX_SYNC	LPSPi2_SCK	GPIO2_IO10	FLEXPWM2_PWMX00	
8	GPIO_EMC_09	ALT5 GPIO2_IO09 (input)	Keeper	yes		SEMC_WE	XBAR1_INOUT09	FLEXCAN2_RX	SAI2_RX_BCLK	FLEXIO1_FLEXIO21	GPIO2_IO09		
9	GPIO_EMC_08	ALT5 GPIO2_IO08 (input)	Keeper	yes		SEMC_DM00	XBAR1_INOUT08	FLEXCAN2_TX	SAI2_RX_DATA	FLEXIO1_FLEXIO20	GPIO2_IO08		
10	GPIO_EMC_07	ALT5 GPIO2_IO07 (input)	Keeper	yes		SEMC_DATA07	XBAR1_INOUT07	LPUART3_RX	SAI2_RX_SYNC	FLEXIO1_FLEXIO19	GPIO2_IO07		
11	NVCC_GPIO	supply											
12	GPIO_EMC_06	ALT5 GPIO2_IO06 (input)	Keeper	yes		SEMC_DATA06	XBAR1_INOUT06	LPUART3_TX	SAI2_TX_DATA	FLEXIO1_FLEXIO18	GPIO2_IO06		
13	GPIO_EMC_05	ALT5 GPIO2_IO05 (input)	Keeper	yes		SEMC_DATA05	XBAR1_INOUT05	SPDIF_IN	SAI2_TX_SYNC	FLEXIO1_FLEXIO17	GPIO2_IO05		
14	GPIO_EMC_04	ALT5 GPIO2_IO04 (input)	Keeper	yes		SEMC_DATA04	XBAR1_INOUT04	SPDIF_OUT	SAI2_TX_BCLK	FLEXIO1_FLEXIO16	GPIO2_IO04		
15	GPIO_EMC_03	ALT5 GPIO2_IO03 (input)	Keeper	yes		SEMC_DATA03	QTIMER2_TIMER3	LPUART4_RX	SPDIF_EXT_CLK	LPSPi2_SDI	GPIO2_IO03	LPI2C1_SDA	
16	GPIO_EMC_02	ALT5 GPIO2_IO02 (input)	Keeper	yes		SEMC_DATA02	QTIMER2_TIMER2	LPUART4_TX	SPDIF_LOCK	LPSPi2_SDO	GPIO2_IO02	LPI2C1_SCL	
17	GPIO_EMC_01	ALT5 GPIO2_IO01 (input)	Keeper	yes		SEMC_DATA01	QTIMER2_TIMER1	LPUART4_RTS_B	SPDIF_OUT	LPSPi2_PCS0	GPIO2_IO01	FLEXCAN1_RX	PIT_TRIGGER03
18	GPIO_EMC_00	ALT5 GPIO2_IO00 (input)	Keeper	yes		SEMC_DATA00	QTIMER2_TIMER0	LPUART4_CTS_B	SPDIF_SR_CLK	LPSPi2_SCK	GPIO2_IO00	FLEXCAN1_TX	PIT_TRIGGER02
19	GPIO_SD_B1_11	ALT5 GPIO3_IO31 (input)	Keeper	yes		USDHC2_DATA7	FLEXSPI_A_SS0_B	ENET_TDATA01	SAI3_RX_DATA	LPSPi2_PCS3	GPIO3_IO31		
20	NVCC_GPIO	supply											
21	GPIO_SD_B1_10	ALT5 GPIO3_IO30 (input)	Keeper	yes		USDHC2_DATA6	FLEXSPI_A_DATA01	ENET_TDATA00	SAI3_RX_SYNC	LPSPi2_PCS2	GPIO3_IO30		
22	GPIO_SD_B1_09	ALT5 GPIO3_IO29 (input)	Keeper	yes		USDHC2_DATA5	FLEXSPI_A_DATA02	ENET_TX_EN	SAI3_RX_BCLK	LPSPi2_SDI	GPIO3_IO29		
23	GPIO_SD_B1_08	ALT5 GPIO3_IO28 (input)	Keeper	yes		USDHC2_DATA4	FLEXSPI_A_DATA00	ENET_RX_ER	SAI3_TX_DATA	LPSPi2_SDO	GPIO3_IO28		
24	GPIO_SD_B1_07	ALT5 GPIO3_IO27 (input)	Keeper	yes		USDHC2_RESET_B	FLEXSPI_A_SCLK	ENET_RX_EN	SAI3_TX_SYNC	LPSPi2_SCK	GPIO3_IO27		
25	GPIO_SD_B1_06	ALT5 GPIO3_IO26 (input)	Keeper	yes		USDHC2_CD_B	FLEXSPI_A_DATA03	ENET_RDATA00	SAI3_TX_BCLK	LPSPi2_PCS0	GPIO3_IO26	CCM_STOP	
26	GPIO_SD_B1_05	ALT5 GPIO3_IO25 (input)	Keeper	yes		USDHC2_DATA1	FLEXSPI_A_DQS	ENET_RDATA01	SAI3_MCLK	FLEXSPI_B_SS0_B	GPIO3_IO25	CCM_PMIC_RDY	
27	GPIO_SD_B1_04	ALT5 GPIO3_IO24 (input)	Keeper	yes		USDHC2_DATA0	FLEXSPI_B_DATA01	ENET_TX_CLK	ENET_REF_CLK1	EWM_OUT_B	GPIO3_IO24	CCM_WAIT	
28	GPIO_SD_B1_03	ALT5 GPIO3_IO23 (input)	Keeper	yes		USDHC2_CLK	FLEXSPI_B_DATA02	LPUART8_RX	LPI2C4_SDA	ENET_1588_EVENT1_IN	GPIO3_IO23	CCM_CLK02	
29	NVCC_GPIO	supply											
30	GPIO_SD_B1_02	ALT5 GPIO3_IO22 (input)	Keeper	yes		USDHC2_CMD	FLEXSPI_B_DATA00	LPUART8_TX	LPI2C4_SCL	ENET_1588_EVENT1_OUT	GPIO3_IO22	CCM_CLK01	
31	VDD_SOC_IN	supply											
32	GPIO_SD_B1_01	ALT5 GPIO3_IO21 (input)	Keeper	yes		USDHC2_DATA3	FLEXSPI_B_SCLK	LPUART6_RX	FLEXSPI_A_SS1_B	FLEXCAN1_RX	GPIO3_IO21		
33	GPIO_SD_B1_00	ALT5 GPIO3_IO20 (input)	Keeper	yes		USDHC2_DATA2	FLEXSPI_B_DATA03	LPUART6_TX	XBAR1_INOUT10	FLEXCAN1_TX	GPIO3_IO20		
34	DCDC_IN	supply											
35	DCDC_GND	supply											
36	DCDC_LP	supply											

 Bottom side, pins 37-72 (left to right)

[illegible]

 Right side, pins 73-108 (bottom to top)

Pin	Pad	Reset function	Reset pull	Pull config	Boot sample	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
73	VDDA_ADC_3P3	supply											
74	GPIO_AD_B1_15	ALT5 GPIO1_IO31 (input)	Keeper	yes		LPI2C1_SDA	ACMP4_OUT	LPSPi3_SDI	ENET_1588_EVENT0_IN	FLEXIO1_FLEXIO00	GPIO1_IO31		
75	GPIO_AD_B1_14	ALT5 GPIO1_IO30 (input)	Keeper	yes		LPI2C1_SCL	ACMP3_OUT	LPSPi3_SDO	ENET_1588_EVENT0_OUT	FLEXIO1_FLEXIO01	GPIO1_IO30		
76	GPIO_AD_B1_13	ALT5 GPIO1_IO29 (input)	Keeper	yes		LPI2C1_HREQ	ACMP2_OUT	LPSPi3_PCS0	USDHC2_WP	FLEXIO1_FLEXIO02	GPIO1_IO29	FLEXPWM1_PWMB03	
77	NC	NC											
78	GPIO_AD_B1_12	ALT5 GPIO1_IO28 (input)	Keeper	yes		USB_OTG1_OC	ACMP1_OUT	LPSPi3_SCK	USDHC2_CD_B	FLEXIO1_FLEXIO03	GPIO1_IO28	FLEXPWM1_PWMA03	
79	GPIO_AD_B1_11	ALT5 GPIO1_IO27 (input)	Keeper	yes		USB_OTG1_ID	FLEXPWM1_PWMB02	LPUART4_RX	USDHC1_WP	FLEXIO1_FLEXIO04	GPIO1_IO27	GPT2_COMPARE1	
80	GPIO_AD_B1_10	ALT5 GPIO1_IO26 (input)	Keeper	yes		USB_OTG1_PWR	FLEXPWM1_PWMA02	LPUART4_TX	USDHC1_CD_B	FLEXIO1_FLEXIO05	GPIO1_IO26	GPT2_CAPTURE1	
81	GPIO_AD_B1_09	ALT5 GPIO1_IO25 (input)	Keeper	yes		LPI2C2_SDA	FLEXPWM1_PWMB01	LPUART2_RX	SAI1_TX_DATA03	FLEXIO1_FLEXIO06	GPIO1_IO25	LPSPi3_PCS1	XBAR1_INOUT13
82	GPIO_AD_B1_08	ALT5 GPIO1_IO24 (input)	Keeper	yes		LPI2C2_SCL	FLEXPWM1_PWMA01	LPUART2_TX	SAI1_TX_DATA02	FLEXIO1_FLEXIO07	GPIO1_IO24	LPSPi3_PCS2	XBAR1_INOUT12
83	GPIO_AD_B1_07	ALT5 GPIO1_IO23 (input)	Keeper	yes		USDHC1_VSELECT	FLEXPWM1_PWMB00	LPUART2_RTS_B	SAI1_TX_DATA01	FLEXIO1_FLEXIO08	GPIO1_IO23	LPSPi3_PCS3	KPP_ROW07
84	GPIO_AD_B1_06	ALT5 GPIO1_IO22 (input)	Keeper	yes		USDHC1_RESET_B	FLEXPWM1_PWMA00	LPUART2_CTS_B	SAI1_RX_BCLK	FLEXIO1_FLEXIO09	GPIO1_IO22	LPSPi1_PCS3	KPP_COL07
85	VSS	supply											
86	VDD_SOC_IN	supply											
87	NC	NC											
88	NC	NC											
89	NC	NC											
90	NC	NC											
91	NC	NC											
92	NC	NC											
93	GPIO_AD_B0_15	ALT5 GPIO1_IO15 (input)	Keeper	yes		ENET_TDATA01	FLEXCAN2_RX	LPUART3_RX	KPP_ROW03	FLEXPWM2_PWMB00	GPIO1_IO15	ARM_CM7_TRACE03	
94	GPIO_AD_B0_14	ALT5 GPIO1_IO14 (input)	Keeper	yes		ENET_TDATA00	FLEXCAN2_TX	LPUART3_TX	KPP_COL03	FLEXPWM2_PWMA00	GPIO1_IO14	ARM_CM7_TRACE02	WDOG1_ANY
95	GPIO_AD_B0_13	ALT5 GPIO1_IO13 (input)	Keeper	yes		ENET_TX_EN	LPSPi1_SDI	LPUART3_RTS_B	KPP_ROW02	FLEXPWM2_PWMB01	GPIO1_IO13	ARM_CM7_TRACE01	SNVS_HP_VIO_5_B
96	GPIO_AD_B0_12	ALT5 GPIO1_IO12 (input)	Keeper	yes		ENET_RX_ER	LPSPi1_SDO	LPUART3_CTS_B	KPP_COL02	FLEXPWM2_PWMA01	GPIO1_IO12	ARM_CM7_TRACE00	SNVS_HP_VIO_5_CTL
97	GPIO_AD_B0_11	ALT5 GPIO1_IO11 (input)	Keeper	yes		ENET_RX_EN	LPSPi1_PCS0	LPUART5_RX	KPP_ROW01	FLEXPWM2_PWMB02	GPIO1_IO11	ARM_CM7_TRACE_SW	
98	GPIO_AD_B0_10	ALT5 GPIO1_IO10 (input)	Keeper	yes		ENET_RDATA00	LPSPi1_SCK	LPUART5_TX	KPP_COL01	FLEXPWM2_PWMA02	GPIO1_IO10	ARM_CM7_TRACE_CLK	
99	GPIO_AD_B0_09	ALT5 GPIO1_IO09 (input)	Keeper	yes		ENET_RDATA01	LPI2C3_SDA	LPUART1_RTS_B	KPP_ROW00		GPIO1_IO09	ARM_CM7_RXEV	
100	GPIO_AD_B0_08	ALT5 GPIO1_IO08 (input)	Keeper	yes		ENET_TX_CLK	LPI2C3_SCL	LPUART1_CTS_B	KPP_COL00	ENET_REF_CLK1	GPIO1_IO08	ARM_CM7_TXEV	
101	GPIO_AD_B0_07	ALT5 GPIO1_IO07 (input)	Keeper	yes		PIT_TRIGGER01	MQS_LEFT	LPUART1_RX	QTIMER2_TIMER3	FLEXPWM2_PWMB03	GPIO1_IO07	REF_24M_OUT	
102	VDD_SOC_IN	supply											
103	VSS	supply											
104	NC	NC											
105	GPIO_AD_B0_06	ALT5 GPIO1_IO06 (input)	Keeper	yes		PIT_TRIGGER00	MQS_RIGHT	LPUART1_TX	QTIMER2_TIMER2	FLEXPWM2_PWMA03	GPIO1_IO06	REF_32K_OUT	
106	GPIO_AD_B0_05	ALT0 JTAG_TRSTB (input)	47K PU	yes		JTAG_TRSTB	FLEXCAN1_RX	USDHC1_CD_B	QTIMER2_TIMER1	ENET_MDC	GPIO1_IO05	USB_OTG1_ID	NMI_GLUE_NMI
107	GPIO_AD_B0_04	ALT0 JTAG_TDO (input)	Keeper	yes		JTAG_TDO	FLEXCAN1_TX	USDHC1_WP	QTIMER2_TIMER0	ENET_MDIO	GPIO1_IO04	USB_OTG1_PWR	EWM_OUT_B
108	GPIO_AD_B0_03	ALT0 JTAG_TDI (input)	47K PU	yes		JTAG_TDI	USDHC2_CD_B	WDOG1_B	SAI1_MCLK	USDHC1_WP	GPIO1_IO03	USB_OTG1_OC	CCM_PMIC_RDY

 Top side, pins 109-144 (right to left)

Pin	Pad	Reset function	Reset pull	Pull config	Boot sample	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
109	GPIO_AD_B0_02	ALT0 JTAG_MOD (input)	100K PD	yes		JTAG_MOD					GPIO1_IO02		GPT1_CAPTURE1
110	GPIO_AD_B0_01	ALT0 JTAG_TCK (input)	100K PD	yes		JTAG_TCK					GPIO1_IO01		GPT1_CAPTURE2
111	GPIO_AD_B0_00	ALT0 JTAG_TMS (input)	47K PU	yes		JTAG_TMS					GPIO1_IO00		GPT1_COMPARE1
112	NVCC_GPIO	supply											
113	VSS	supply											
114	VDD_SOC_IN	supply											
115	GPIO_EMC_41	ALT5 GPIO3_IO09 (input)	Keeper	yes		SEMC_READY	XBAR1_INOUT19	SPDIF_IN	USB_OTG1_PWR	ENET_MDC	GPIO3_IO09	ENET_TDATA02	GPT1_COMPARE2
116	GPIO_EMC_40	ALT5 GPIO3_IO08 (input)	Keeper	yes		SEMC_CSX00	XBAR1_INOUT18	SPDIF_OUT	USB_OTG1_ID	ENET_MDIO	GPIO3_IO08	ENET_TDATA03	GPT1_COMPARE3
117	GPIO_EMC_39	ALT5 GPIO3_IO07 (input)	Keeper	yes		SEMC_DATA15	FLEXPWM2_PWMB00	LPUART5_RX	USB_OTG1_OC	WD0G1_B	GPIO3_IO07	ENET_TX_ER	GPT1_CLK
118	GPIO_EMC_38	ALT5 GPIO3_IO06 (input)	Keeper	yes		SEMC_DATA14	FLEXPWM2_PWMA00	LPUART5_TX	MQS_LEFT	LPSPi4_PCS3	GPIO3_IO06	ENET_RDATA02	USDHC1_CD_B
119	GPIO_EMC_37	ALT5 GPIO3_IO05 (input)	Keeper	yes		SEMC_DATA13	FLEXPWM2_PWMB01	LPUART5_RTS_B	MQS_RIGHT	LPSPi4_PCS2	GPIO3_IO05	ENET_RDATA03	USDHC1_VSELECT
120	GPIO_EMC_36	ALT5 GPIO3_IO04 (input)	Keeper	yes		SEMC_DATA12	FLEXPWM2_PWMA01	LPUART5_CTS_B	CCM_PMIC_RDY	LPSPi4_PCS1	GPIO3_IO04	ENET_RX_CLK	USDHC1_WP
121	GPIO_EMC_35	ALT5 GPIO3_IO03 (input)	Keeper	yes		SEMC_DATA11	QTIMER1_TIMER3	LPUART7_RX	USDHC2_WP	LPSPi4_SDI	GPIO3_IO03	ENET_COL	
122	GPIO_EMC_34	ALT5 GPIO3_IO02 (input)	Keeper	yes		SEMC_DATA10	QTIMER1_TIMER2	LPUART7_TX	SAI3_TX_SYNC	LPSPi4_SDO	GPIO3_IO02	ENET_CRS	
123	GPIO_EMC_33	ALT5 GPIO3_IO01 (input)	Keeper	yes		SEMC_DATA09	QTIMER1_TIMER1	LPUART4_RX	SAI3_TX_BCLK	LPSPi4_PCS0	GPIO3_IO01		
124	GPIO_EMC_32	ALT5 GPIO3_IO00 (input)	Keeper	yes		SEMC_DATA08	QTIMER1_TIMER0	LPUART4_TX	SAI3_TX_DATA	LPSPi4_SCK	GPIO3_IO00		REF_24M_OUT
125	GPIO_EMC_31	ALT5 GPIO2_IO31 (input)	Keeper	yes		SEMC_DM01	FLEXPWM2_PWMB02	LPUART4_RTS_B	SAI3_RX_DATA	WD0G2_B	GPIO2_IO31	GPT2_CLK	FLEXPWM1_PWMX03
126	GPIO_EMC_30	ALT5 GPIO2_IO30 (input)	Keeper	yes		SEMC_CLK	FLEXPWM2_PWMA02	LPUART4_CTS_B	SAI3_RX_SYNC	WD0G1_RST_B_DEB	GPIO2_IO30	GPT2_COMPARE3	FLEXPWM1_PWMX02
127	GPIO_EMC_29	ALT5 GPIO2_IO29 (input)	100k PD	yes		SEMC_CKE	FLEXPWM2_PWMB03	XBAR1_INOUT19	SAI3_RX_BCLK	WD0G2_RST_B_DEB	GPIO2_IO29	GPT2_COMPARE2	FLEXPWM1_PWMX01
128	GPIO_EMC_28	ALT5 GPIO2_IO28 (input)	Keeper	yes		SEMC_DQS	FLEXPWM2_PWMA03	XBAR1_INOUT18	SAI3_MCLK	EWM_OUT_B	GPIO2_IO28	GPT2_CAPTURE2	FLEXPWM1_PWMX00
129	GPIO_EMC_27	ALT5 GPIO2_IO27 (input)	Keeper (Table 68: 100K PD)	yes	BT_CFG[9] = BOOT_CFG2[1] → SRC_SBMR1[9]	SEMC_ADDR12	FLEXPWM1_PWMB00	LPUART8_RX	SAI1_TX_SYNC	FLEXIO1_FLEXIO31	GPIO2_IO27	SRC_BT_CFG09	
130	GPIO_EMC_26	ALT5 GPIO2_IO26 (input)	Keeper (Table 68: 100K PD)	yes	BT_CFG[8] = BOOT_CFG2[0] → SRC_SBMR1[8]	SEMC_ADDR11	FLEXPWM1_PWMA00	LPUART8_TX	SAI1_TX_BCLK	FLEXIO1_FLEXIO30	GPIO2_IO26	SRC_BT_CFG08	
131	GPIO_EMC_25	ALT5 GPIO2_IO25 (input)	Keeper (Table 68: 100K PD)	yes	BT_CFG[7] = BOOT_CFG1[7] → SRC_SBMR1[7]	SEMC_ADDR09	FLEXPWM1_PWMB01	LPUART8_RTS_B	SAI1_TX_DATA00	FLEXIO1_FLEXIO29	GPIO2_IO25	SRC_BT_CFG07	
132	GPIO_EMC_24	ALT5 GPIO2_IO24 (input)	Keeper (Table 68: 100K PD)	yes	BT_CFG[6] = BOOT_CFG1[6] → SRC_SBMR1[6]	SEMC_ADDR08	FLEXPWM1_PWMA01	LPUART8_CTS_B	SAI1_TX_DATA01	FLEXIO1_FLEXIO28	GPIO2_IO24	SRC_BT_CFG06	
133	GPIO_EMC_23	ALT5 GPIO2_IO23 (input)	Keeper (Table 68: 100K PD)	yes	BT_CFG[5] = BOOT_CFG1[5] → SRC_SBMR1[5]	SEMC_ADDR07	FLEXPWM1_PWMB02	LPUART2_RX	SAI1_TX_DATA02	FLEXIO1_FLEXIO27	GPIO2_IO23	SRC_BT_CFG05	
134	VDD_SOC_IN	supply											
135	VSS	supply											
136	GPIO_EMC_22	ALT5 GPIO2_IO22 (input)	Keeper (Table 68: 100K PD)	yes	BT_CFG[4] = BOOT_CFG1[4] → SRC_SBMR1[4]	SEMC_ADDR06	FLEXPWM1_PWMA02	LPUART2_TX	SAI1_TX_DATA03	FLEXIO1_FLEXIO26	GPIO2_IO22	SRC_BT_CFG04	
137	GPIO_EMC_21	ALT5 GPIO2_IO21 (input)	Keeper (Table 68: 100K PD)	yes	BT_CFG[3] = BOOT_CFG1[3] → SRC_SBMR1[3]	SEMC_ADDR05	FLEXPWM1_PWMB03	LPUART2_RTS_B	SAI1_RX_DATA00	FLEXIO1_FLEXIO25	GPIO2_IO21	SRC_BT_CFG03	
138	GPIO_EMC_20	ALT5 GPIO2_IO20 (input)	Keeper (Table 68: 100K PD)	yes	BT_CFG[2] = BOOT_CFG1[2] → SRC_SBMR1[2]	SEMC_ADDR04	FLEXPWM1_PWMA03	LPUART2_CTS_B	SAI1_MCLK	FLEXIO1_FLEXIO24	GPIO2_IO20	SRC_BT_CFG02	
139	GPIO_EMC_19	ALT5 GPIO2_IO19 (input)	Keeper (Table 68: 100K PD)	yes	BT_CFG[1] = BOOT_CFG1[1] → SRC_SBMR1[1]	SEMC_ADDR03	XBAR1_INOUT17	LPI2C2_SCL	SAI1_RX_BCLK	FLEXIO1_FLEXIO23	GPIO2_IO19	SRC_BT_CFG01	
140	GPIO_EMC_18	ALT5 GPIO2_IO18 (input)	Keeper (Table 68: 100K PD)	yes	BT_CFG[0] = BOOT_CFG1[0] → SRC_SBMR1[0]	SEMC_ADDR02	XBAR1_INOUT16	LPI2C2_SDA	SAI1_RX_SYNC	FLEXIO1_FLEXIO22	GPIO2_IO18	SRC_BT_CFG00	
141	GPIO_EMC_17	ALT6 SRC_BOOT_MODE01 (input)	100K PD	yes	BOOT_MODE1 → SRC_SBMR2[25] (BMOD[1])	SEMC_ADDR01		MQS_LEFT	SAI3_MCLK		GPIO2_IO17	SRC_BOOT_MODE01	
142	GPIO_EMC_16	ALT6 SRC_BOOT_MODE00 (input)	100K PD	yes	BOOT_MODE0 → SRC_SBMR2[24] (BMOD[0])	SEMC_ADDR00		MQS_RIGHT	SAI2_MCLK		GPIO2_IO16	SRC_BOOT_MODE00	
143	GPIO_EMC_15	ALT5 GPIO2_IO15 (input)	Keeper	yes		SEMC_ADDR10	XBAR1_INOUT15	LPUART6_RTS_B	SAI1_RX_SYNC	WD0G1_B	GPIO2_IO15	FLEXCAN1_RX	
144	NVCC_GPIO	supply											

Sources

- **Pin numbers and reset state:** datasheet IMXRT1024CEC.pdf Table 82.
- **Alternate functions:** the SDK's sdk/fs1_iomuxc_MIMXRT1024.h, via planning/pinplan/pads.csv. The RM gives the same options per pad in chapter 11 (IOMUXC SW_MUX_CTL_PAD_*), and by peripheral in section 10.1.1.
- **Boot sampling:** RM Table 9-4 (GPIO boot overrides) and the SRC_SBMR1/SBMR2 registers (RM 21.8).

Columns

- **Reset function:** the ALT mode selected at reset, and its direction.
- **Reset pull:** the pull or keeper active at reset. The SNVS pads and the boot-strap pads have real pulls at reset. Most GPIO pads only have a keeper, so they float to whatever level they last saw.
- **Pull config:** yes means the pad has a SW_PAD_CTL_PAD_* register with PKE/PUE/PUS. Each such pad can select a keeper, no pull, or one of 100K pull-down, 47K pull-up, 100K pull-up or 22K pull-up. This applies to all GPIO pads and to the six SNVS-domain pads (WAKEUP, PMIC_ON_REQ, PMIC_STBY_REQ, TEST_MODE, POR_B, ONOFF). Analog and supply pins have no pull control.
- **Boot sample:** what the pin's level is latched into on the rising edge of POR_B.

- BOOT_MODE0/1 always select the boot mode (SRC_SBMR2 BMOD).
- The BT_CFG pads override the BOOT_CFG1/BOOT_CFG2 fuses only while the BT_FUSE_SEL fuse is unblown. The latched value is in SRC_SBMR1 either way.
- **Strap pulls disagree in the datasheet.** Table 68 (boot pins) gives all twelve strap pads a 100K pull-down at reset, while Table 82 gives one only to BOOT_MODE0/1 and a keeper to BT_CFG[0..9]. The RM's pad-register reset values don't settle it. Don't rely on the internal pull for a strap's level: fit an external resistor wherever the value matters.

- **ALT0-ALT7:** the IOMUXC mux modes. A blank cell is an unused mode.

Notes

- **Pins 87-92 are NC.** The on-package flash uses die-internal pads GPIO_AD_B1_00..05. Their pad-side DQS, GPIO_SD_B1_05 (pin 26), must be left floating (AN12878).
- **GPIO_AD_B1_13 (pin 76)** is driven by the ROM as the serial-NOR reset output.
- **GPIO_AD_B0_00..02 (pins 111, 110, 109)** are SWDIO, SWCLK and JTAG_MOD. JTAG_MOD must be tied to GND for SWD.
- **GPIO_AD_B0_06..09** are taken over by the ROM as LPUART1 in serial-download mode.