

Proposed modification to the Usif REV 1-1 (2000)

Motivation :

The existing product stores card holder's data in SRAM (U14 and U 8) which are BS62LV4006SIP55 Ic's . Although the SRAMS receive power on pin 32 from either VCC , or BAT via a wired OR diode configuration (D1 & D2), when the primary power is interrupted there is a requirement to hold CE/ (Pin 22 of the SRAM's) high as well to retain data and – hopefully prevent data corruption .

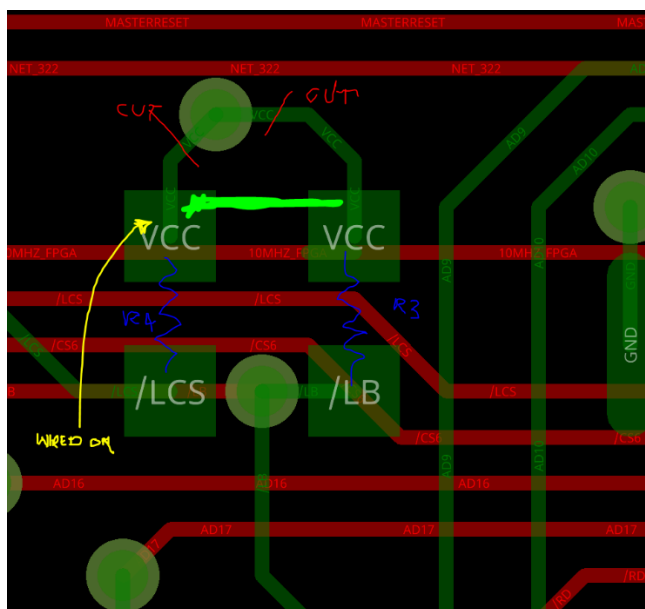
Problem definition :

The CE lines to the SRAM chips are held high by two resistors (10K) which are connected to VCC only . So when VCC is not available then the SRAM data is lost.

Resolution first attempt to solve the problem was to supply the pullup resistors with either VCC or BAT as is the case with the pin 32 power .

Steps –

1. Cut tracks from through hole to R3 & R 4 (red lines in image)
2. Join R3 and R4 (green line in image)
3. Run a wire from the wired or (D1 & D2) supplying SRAM power to the Pullup resistors (Yellow line in image)

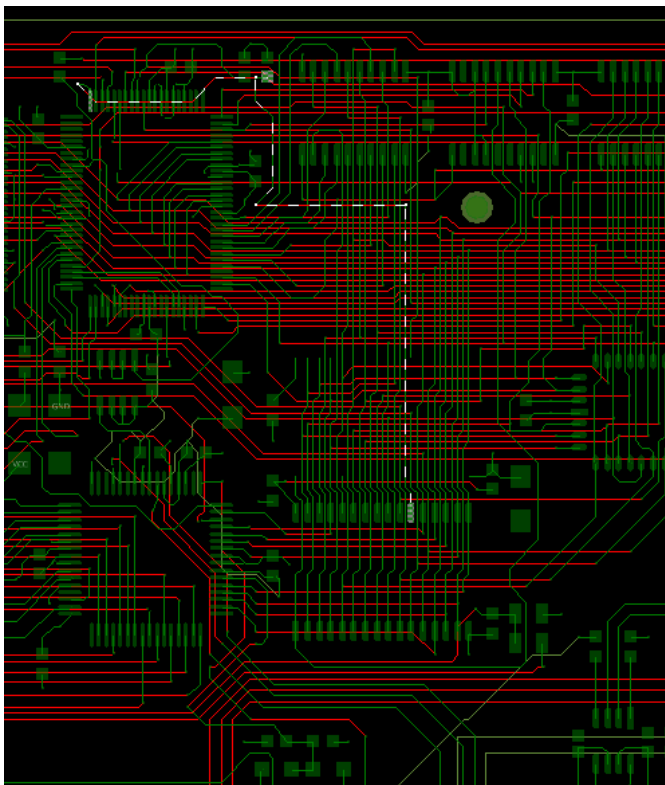


Result of first attempt : When switching to battery power the battery ran flat in a shorter time period that expected.

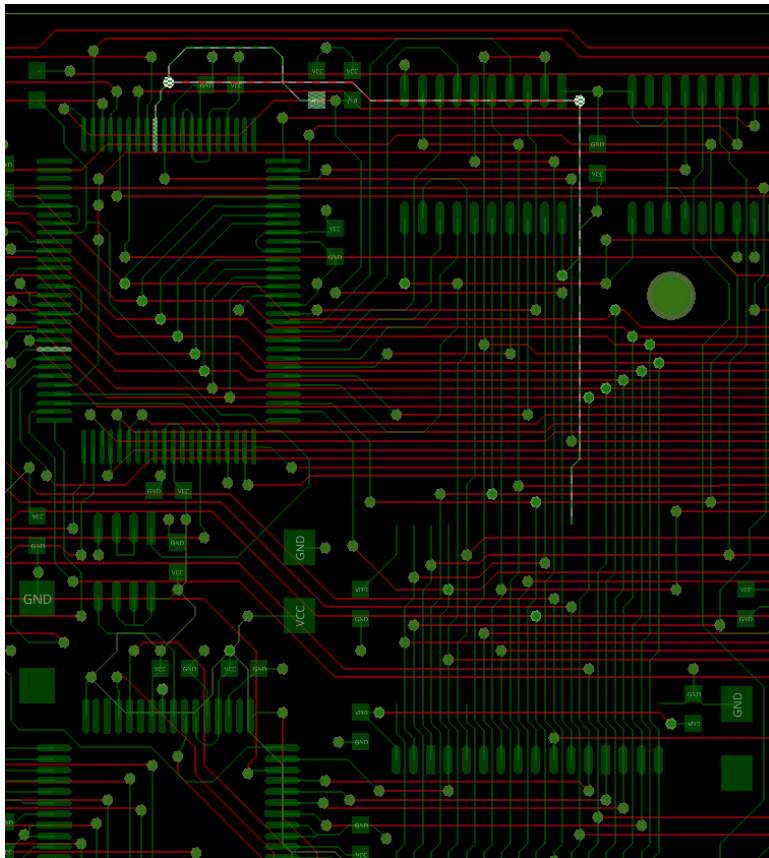
The CE lines were then checked on the PCB layout and buzzed out with a multimeter

- The first CE line (/LCS) has pullup resistor R4 and the signal starts at CPU pin 92 and goes to SRAM (U8 – Pin 22) .
- The second CE line (/LB) has pullup resistor R3 and the signal starts at CPU pin 100 and goes to SRAM (U14 pin 22)
- It was further noticed that /LCS also exist the CPU PIN 22 , and goes to the Lonworks Neuron chip Pin 16 .

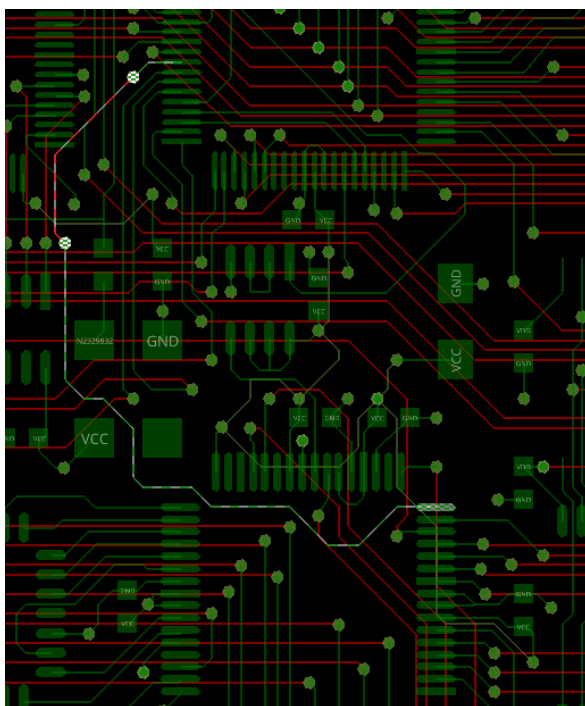
The pictures below show routing :



LB routing .



LCS routing



LCS to neuron chip

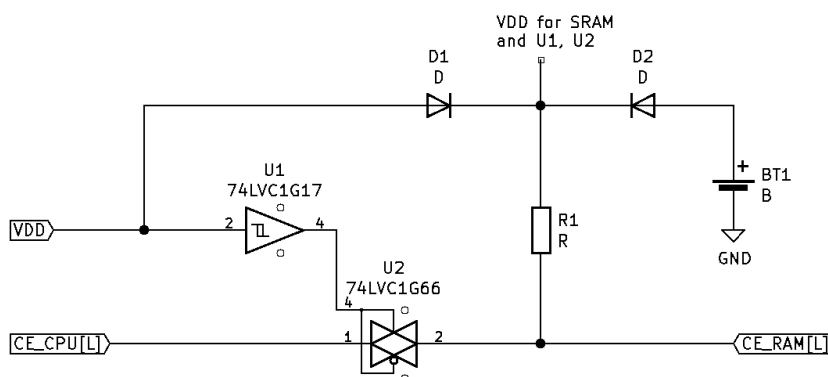
Summary : It appears as if current is being drained through the CPU I/O pins . Even though the CPU is not powered there is a path and we suspect through the internal protection diodes. We lifted the CPU pins 100 and 92 and the current drain reduced substantially. (Insert measured numbers ...)

Second attempt : It was decided to try and insert a FET – 2N7000 in the LCS and LB lines such that when VCC was lost the SRAMS pullups would still operate BUT the circuit to CPU pin 100 and 92 would be “ disconnected / isolated “ by the FET – This did not work so I then placed questions on the EEVBLOG forum.

Summarized feedback :

1. **Benta** – 74hct1g66 or use fram or nvram , schematic suggestion , agree with tim ‘ main power supervisor should be tied into a solution .
2. **Opossum** – ds1312
3. **Edavid** – 2n700 not suitable due to vgs too high – require logic level fets , caution re 4066 rc delays – look at 74hc32 + inverter (TL 7705 supervisor) , If you use 74hc32 you don’t need pullups
4. **Cjay** – how can 2.4AH battery deplete I 20 hrs through 10k resistor, Is vcc to sram isolated from rest of the board .
5. **Silicon wizard** – isolate ce lines with diodes , try Schottky diode if vf too high
6. **T3sl4col1** – Mosfets have ~ 30pf capacitance and threshold should be ttl level . Analogue switch 74hc4066 better . A logic gate that disconnects output when power off such as a buffer eg 74LVC series (note marginal with 5V) . Transmission gate 74hc125 with OE driven from inverted VCC – power inverter from vbatt – HC4066 probably best solution . 74HC2g02 will do it in one chip. Should detect power failing before it crosses logic threshold an active high reset generator / voltage detector IC would be perfect . Concurs with **benta** that supervisor chip should be used as a natural fit.

Conclusion – A power / reset supervisor chip should be used . An analogue switch can be used to open these lines. Mosfets are not best fit . Benta sent suggested circuit (below) and we will procure the components and try this out



For multiple isolation just duplicate U2 and R1 – Many Thanks to all.

