

CPU (Slot #0) module

A		Dir	B		Dir	C		Dir
1	+5V	O DC power	+12V	O DC power		-12V	O DC power	
2	GND		SSDA	I/O Shared I2C SDA (not isolated!)		SSCL	I/O Shared I2C SCL	
3	Vbat	O Backup battery (max. +3.3 V)	GND			RESET	O Master reset	
4	STARX1	I/O #1 STARX	MASTER_CLK-	O Master clock 100 MHz		MASTER_CLK+	O Master clock 100 MHz	
5	STARY1	I/O #1 STARY	CS1 Diff+	O #1 SPI chip select		GND		
6	STRGIN1	I Trigger in #1	CS1 Diff-	O #1 SPI chip select		SCLK1	O #1 SPI clock	
7	STARX2	I/O #2 STARX	CS2 Diff+	O #2 SPI chip select		MOSI1	O #1 SPI MOSI	
8	STARY2	I/O #2 STARY	CS2 Diff-	O #2 SPI chip select		MISO1	I #1 SPI MISO	
9	STRGIN2	I Trigger in #2	CS3	O #3 SPI chip select		GND		
10	STARX3	I/O #3 STARX	CS4	O #4 SPI chip select		SCLK2	O #2 SPI clock	
11	STARY3	I/O #3 STARY	CS5	O #5 SPI chip select		MOSI2	O #2 SPI MOSI	
12	STRGIN3	I Trigger in #3	CS6	O #6 SPI chip select		MISO2	I #2 SPI MISO	
13	STARX4	I/O #4 STARX	CS7	O #7 SPI chip select		GND		
14	STARY4	I/O #4 STARY	GND			SCLK3	O #3 SPI clock	
15	STRGIN4	I Trigger in #4	ITRO1	I IRQ1 or Trigger out #1		MOSI3	O #3 SPI MOSI	
16	STARX5	I/O #5 STARX	ITRO2	I IRQ2 or Trigger out #2		MISO3	I #3 SPI MISO	
17	STARY5	I/O #5 STARY	ITRO3	I IRQ3 or Trigger out #3		GND		
18	STRGIN5	I Trigger in #5	ITRO4	I IRQ4 or Trigger out #4		SCLK4	O #4 SPI clock	
19	STARX6	I/O #6 STARX	ITRO5	I IRQ5 or Trigger out #5		MOSI4	O #4 SPI MOSI	
20	STARY6	I/O #6 STARY	ITRO6	I IRQ6 or Trigger out #6		MISO4	I #4 SPI MISO	
21	STRGIN6	I Trigger in #6	ITRO7	I IRQ7 or Trigger out #7		GND		
22	STARX7	I/O #7 STARX	XL_DN1 Diff+	I/O 2-wire xlink0_rx1		SCLK5	O #5 SPI clock	
23	STARY7	I/O #7 STARY	XL_DN1 Diff-	I/O 2-wire xlink0_rx1		MOSI5	O #5 SPI MOSI	
24	STRGIN7	I Trigger in #7	XL_DN0 Diff+	I/O 2-wire xlink0_rx0		MISO5	I #5 SPI MISO	
25	Reserved	(e.g. JTAG TDI)	XL_DN0 Diff-	I/O 2-wire xlink0_rx0		GND		
26	Reserved	(e.g. JTAG TDO)	XL_UP0 Diff+	I/O 2-wire xlink0_tx0		SCLK6	O #6 SPI Clock	
27	Reserved	(e.g. JTAG TCK)	XL_UP0 Diff-	I/O 2-wire xlink0_tx0		MOSI6	O #6 SPI MOSI	
28	Reserved	(e.g. JTAG TMS)	XL_UP1 Diff+	I/O 2-wire xlink0_tx1		MISO6	I #6 SPI MISO	
29	Reserved	(e.g. JTAG TRST#)	XL_UP1 Diff-	I/O 2-wire xlink0_tx1		GND		
30	GND		???			SCLK7	O #7 SPI clock	
31	+3.3V	O DC power	???			MOSI7	O #7 SPI MOSI	
32	+3.3V	O DC power	+3.3VAUX	O Shutdown/standby power		MISO7	I #7 SPI MISO	

Slot #1 to #7 modules

A		Dir	B		Dir	C		Dir
1	+5V	I	DC power	+12V	I	DC power	-12V	I
2	GND			SSDA	I/O	Shared I ² C SDA	SSCL	I/O
3	Vbat	I	Backup battery (max. +3.3 V)	GND			RESET	I
4	STARX	I/O	#1 STARX	MASTER_CLK-	I	Master clock 100 MHz	MASTER_CLK+	I
5	STARY	I/O	#1 STARY	CS	I	SPI chip select	GND	
6	ITR \overline{O}	O	IRQ or Trigger output	???			SCLK	I
7	Reserved		(e.g. JTAG TDI)	???			MOSI	I
8	Reserved		(e.g. JTAG TDO)	STRGIN	I	Trigger input	MISO	O
9	Reserved		(e.g. JTAG TCK)	XL_DN1 Diff+	I/O	2-wire xlink0_rx1	XL_DN3 Diff+	I/O
10	Reserved		(e.g. JTAG TMS)	XL_DN1 Diff-	I/O	2-wire xlink0_rx1	XL_DN3 Diff-	I/O
11	Reserved		(e.g. JTAG TRST#)	XL_DN0 Diff+	I/O	2-wire xlink0_rx0	XL_DN2 Diff+	I/O
12	???			XL_DN0 Diff-	I/O	2-wire xlink0_rx0	XL_DN2 Diff-	I/O
13	+3.3VAUX	I	Shutdown/standby power	XL_UP0 Diff+	I/O	2-wire xlink0_tx0	XL_UP2 Diff+	I/O
14	GND		DC power	XL_UP0 Diff-	I/O	2-wire xlink0_tx0	XL_UP2 Diff-	I/O
15	+3.3V	I	DC power	XL_UP1 Diff+	I/O	2-wire xlink0_tx1	XL_UP3 Diff+	I/O
16	+3.3V	I	DC power	XL_UP1 Diff-	I/O	2-wire xlink0_tx1	XL_UP3 Diff-	I/O

CS \overline{n}	Module (chip) select input
ITR $\overline{O}n$	Module interrupt or trigger output
SNHN \overline{n}	Module shutdown/standby (can be used for module hard reset)
STRGIN \overline{n}	The Star Trigger lines STRGIN \overline{n} and ITR \overline{n} are used for simultaneous system wide triggering/sampling. Star trigger distribution logic in the slot 0 controller allows for one-to-one and one-to-many trigger distribution among all slots with very low skew. The distribution logic is controlled by the Slot 0 controller.
STARX \overline{n} , STARY \overline{n}	Provide inter-module async communication. Two STAR lines are connected between each module slot and Slot 0. Slot 0 may provide a cross matrix switch (e.g. MT8808/9, ADG2188, etc.) which can programmably route signals between any two STARX or STARY lines. It may also broadcast a signal received on one STAR line to a group of STAR lines. The STAR lines are bidirectional, providing additional flexibility.
Notes:	Master clock could become multidrop LVDS, and SPI #1 and SPI #2 point-to-point LVDS If two or more modules have to be galvanically isolated (e.g. like in case of power supply with floating outputs) use appropriate isolators for control and data lines (e.g. Silabs Si86xx for digital lines)

Connectors

CPU to backplane	96-pin socket DIN 41612, male (type C; a+b+c), angled 90° (e.g. TME: 09031966921)
Backplane to CPU	96-pin plug DIN 41612, female (type C; a+b+c), straight (e.g. TME: 09032966825)
Module to backplane	48-pin socket DIN 41612, male (type 2C; a+b+c), angled 90° (e.g. TME: 09231486921)
Backplane to module	48-pin plug DIN 41612, female (type 2C; a+b+c), straight (e.g. TME: 09232486824)