

Reference Specifications

Product Name: RAS102 (1 to 1 Receiver LSI for 'A-format')

This set of specifications consists of the tables and drawings for the following specifications.

Note that no revised edition will be issued.

REFERENCE ONLY

SANYO DENKI Co., Ltd.
1st Design Department, Servo System Division

Approval	Designed
	

1. Overview

The RAS 102 is a custom LSI that has functions of making transmission to and reception from encoders, such as the Absolute encoder MAR-M30A/M35A, with Nikon's proprietary serial communication format (a.k.a. '*A-format*')

Features

- Transmission/reception functions in a one-to-one connection with an encoder are supported.

Transmission/reception functions in a bus connection are not supported.

- As operation modes, the 16-bit/32-bit CPU (and DSP) modes and the manual mode are supported.
- Read and write processes to the EEPROM of an encoder are supported.
These are not supported in the manual mode.
- Communication baud rate 2.5 Mbps/4 Mbps (selectable)
- As the operation power supply voltage, both single 5V and single 3.3V are supported.

Subject Absolute Encoder

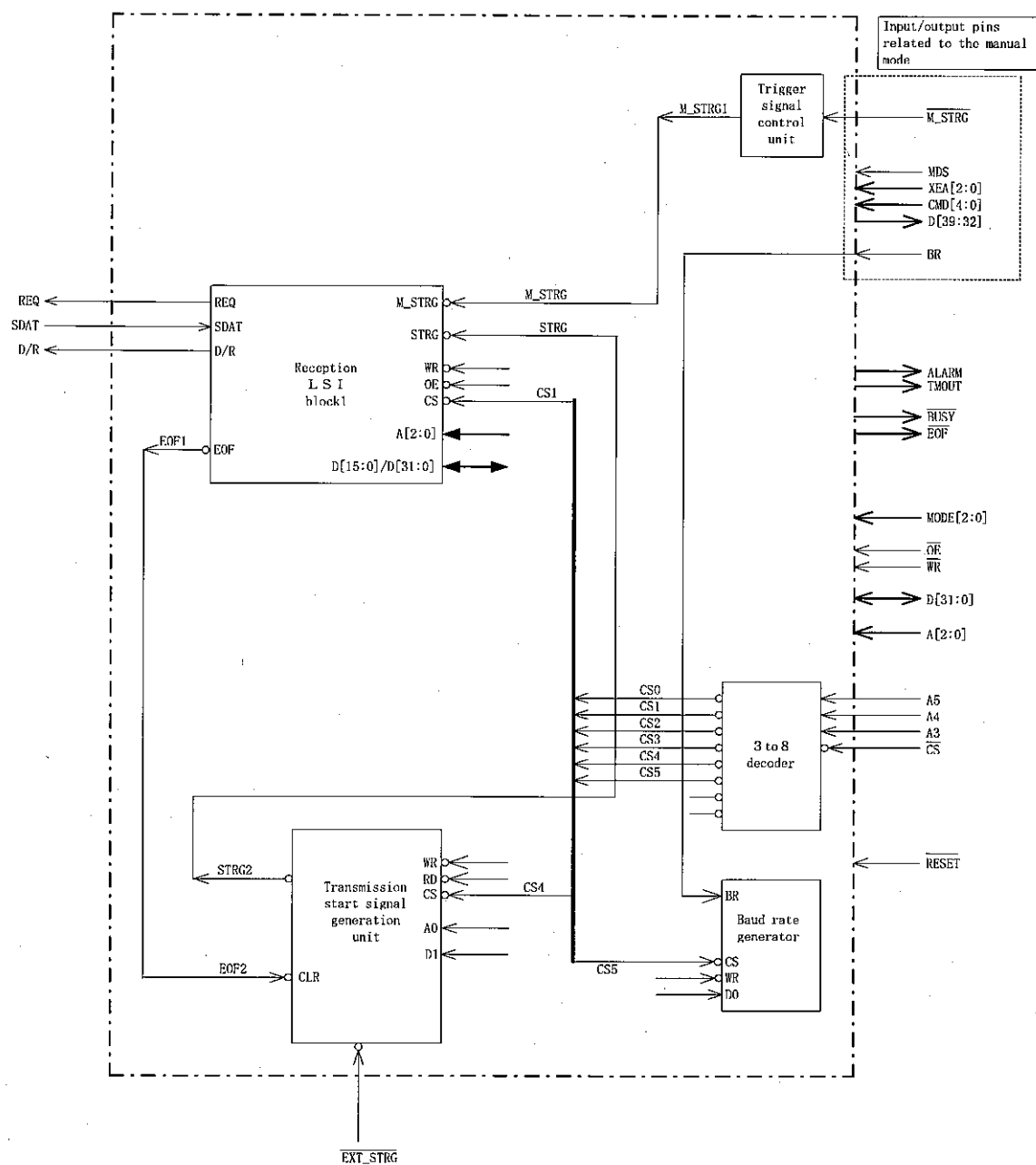
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|--------------|--|
| MAR-M30A/35A | 33-bit output type (1-rotation data 17 bits; multiple-rotation data 16 bits) |
| MAR-M35AH | 36-bit output type (1-rotation data 20 bits; multiple-rotation data 16 bits) |
| - | |

2. Specifications for Serial Communication

Item		Specifications	Remarks
Transmission method		Half-duplex(Semi double) serial communication	Compliance with the EIA standard RS-485
Transmission code		NRZ code	
Synchronous method		Asynchronous communication	
Baud rate		2.5 Mbps/4 Mbps	
Command data	Transmission frames	1 to 4 frames	
	Frame configuration	18 bits/frame	
	Transmission error check	3-bit CRC code	$P(X)=X^3+X+1$
Encoder data	Transfer frames	1 frame	
	Frame configuration	3-4 fields/frame	
	Field configuration	18 bits/field	
	Transmission error check	8-bit CRC code	$P(X)=X^8+X^4+X^3+X^2+1$
	Position data format	Binary data 40 bits ABS [0:39]	ABS[0:16]=ST[0:16] ABS[17:32]=MT[0:15] ABS[33:39]="0000000"

For more information on the frame format, see the specifications for the encoder M30A/M35A. With regard to the specifications for the communication timing, see Chapter "9. Serial Data Transmission/Reception Timings."

3. Internal Configuration



4. Electrical Specifications

4.1 Absolute Maximum Rating

Item	Abbreviation	Condition	Rating	Unit
Power supply voltage	Vdd		-0.3 to +6.0V	V
Input voltage	Vi		-0.3 to Vdd+0.5	V
Output voltage	Vo		-0.3 to Vdd+0.5	V
Output current pin	Iout		±25	mA
Storage temperature	Tstg		-65 to +150	°C

4.2 Recommended Operation Conditions

Item	Abbreviation	Condition	MIN	TYP	MAX	Unit
Power supply voltage	Vdd	When single 5V power supply is in operation	4.5	5.0	5.5	V
		When single 3.3V power supply is in operation	3.0	3.3	3.6	V
Operation temperature	Topr		-40	25	85	°C
Input rise time	Tri	Normal input	-	-	50	ns
Input decay time	Tfi	Normal input	-	-	50	ns
Input rise time	Tri	Schmitt input	-	-	5	ms
Input rise time	Tfi	Schmitt input	-	-	5	ms
Operation frequency				20		MHz
Oscillation frequency deviation			-100	0	100	ppm

4.3 Electrical Features

(1) Single 5V power supply operation (VDD = 5V common, VSS = 0V, Ta = -40 to 85 °C)

Item	Abbreviation	Condition	MIN	TYP	MAX	Unit
Static consumption current	IDDS	Static state	—	—	400	μA
Input leakage current	ILI		-1	—	1	μA
Off-state leakage current	IOZ		-1	—	1	μA
H-level output voltage	VOH	IOH = -12mA, VDD = Min	VDD-0.4	—	—	V
L-level output voltage	VOL	IOL = 12mA, VDD = Min	—	—	0.4	V
H-level input voltage	VIH1	CMOS level, VDD = Max	3.5	—	—	V
L-level input voltage	VIL1	CMOS level, VDD = Min	—	—	1.0	V
H-level input	VT1+	CMOS Schmitt, VDD	—	—	4.0	V

voltage		= 5.0V				
L-level input voltage	VT1-	CMOS Schmitt, VDD = 5.0V	0.8	—	—	V
Hysteresis voltage	VH	CMOS Schmitt, VDD = 5.0V	0.3	—	—	V
Pull-up resistor	RPU	VI = 0V	25	50	100	k Ω
Input terminal capacity	CI	F = 1MHz, VDD = 0V	—	—	12	pF
Output terminal capacity	CO	F = 1MHz, VDD = 0V	—	—	12	pF
Input/output terminal capacity	CIO	F = 1MHz, VDD = 0V	—	—	12	pF

(2) Single 3.3V power supply operation (VDD = 3.3V $\pm$ 0.3V, VSS = 0V, Ta = -40 to 85 °C)

Item	Abbreviation	Condition	MIN	TYP	MAX	Unit
Static consumption current	IDDS	Static state	—	—	290	μ A
Input leakage current	ILI		-1	—	1	μ A
Off-state leakage current	IOZ		-1	—	1	μ A
H-level output voltage	VOH	IOH = -12mA, VDD = Min	VDD-0.3	—	—	V
L-level output voltage	VOL	IOL = 12mA, VDD = Min	—	—	0.3	V
H-level input voltage	VIH1	CMOS level, VDD = Max	2.2	—	—	V
L-level input voltage	VIL1	CMOS level, VDD = Min	—	—	0.8	V
H-level input voltage	VT1+	CMOS Schmitt, VDD = 5.0V	—	—	2.4	V
L-level input voltage	VT1-	CMOS Schmitt, VDD = 5.0V	0.6	—	—	V
Hysteresis voltage	VH	CMOS Schmitt, VDD = 5.0V	0.1	—	—	V
Pull-up resistor	RPU	VI = 0V	45	90	180	k Ω
Input terminal capacity	CI	F = 1MHz, VDD = 0V	—	—	12	pF
Output terminal capacity	CO	F = 1MHz, VDD = 0V	—	—	12	pF
Input/output terminal capacity	CIO	F = 1MHz, VDD = 0V	—	—	12	pF

5. Input/Output Signal

5.1 List of Signal Names

Signal name		Function		Output signal state during reset and immediately after reset
		CPU mode	Manual mode	
X1	I	Input terminal for oscillation.		—
X2	O	Output terminal for oscillation. Reversal phase of X1.		—
REQ	O	Command (serial data) output for an encoder.		H
SDAT	I	Serial data input.		—
D/R	O	Line transceiver control signal. Normally L output. H output during transmission.		L
A5_BR	I	A5: Address input	BR: Communication baud rate setting input.	—
A4_CMD4	I	A4: Address input	CMD4: Command input	—
A3_CMD3	I	A3: Address input	CMD3: Command input	—
A2_CMD2	I	A2: Address input	CMD2: Command input	—
A1_CMD1	I	A1: Address input	CMD1: Command input	—
A0_CMD0	I	A0: Address input	CMD0: Command input	—
D[31:0]	I/O	D [31:0]: Input/output data bus. (D [31:16] must be open in the 16-bit CPU mode.)	D[31:0]: Output data bus	Input state (L in the manual mode)
D[39:32]	O	L output	D[39:32]: Output data bus	L
IOSEL	O	Data bus input/output state signal. L indicates data output. H indicates data input.	L output.	H
/BUSY	O	Communication BUSY signal. L output during data transmission and reception.		H
/EOF	O	Communication processing completion signal. L is output when data reception is completed, and it is released when data is read. Data of the bits in the transmission Trigger register is reset with an EOF signal.	Communication processing completion signal. A strobe signal (L) is output when data reception is completed	—
MODE[1:0]	I	Selection signal for the CPU and manual modes.		—
/CS_XEA2	I	/CS: Chip selection signal. Negative logic	XEA2: Encoder address input	—
/WR_XEA1	I	/WR: Write control signal. Negative logic. L input when data is written.	XEA1: Encoder address input	—
/OE_XEA0	I	/OE: Output enable signal. Negative logic. L input when data is read	XEA0: Encoder address input	—
/STRG	I	External transmission start trigger signal input. An alternative of the CPU control.	Transmission start trigger signal input. Conversion starts by the rise.	—

		Conversion starts by the rise		
MDS	I	Not in use.	Output data selection signal in the manual mode.	—
ALARM	O	L output.	Alarm output. (Logical sum of all alarms)	L
TMOUT	O	A timeout error is output regardless of the mode setting. When data is not returned in response to a transmission of a request within a designated period of time, H output is done. Same as SYNC of the communication alarm CA2 of the register output.		L
/RESET	I	System reset signal. It is reset with L input.		—
OPT0	I	Control selection signal when EEPROM data is read. For more information, see Section 7.8.1.	Not in use.	—
OPT1	I	Timing for t2 in Chapter 9 “Serial Data Transmission/Reception Timings” can be selected. For more information, see Chapter 9.		—
CLKOUT	O	20MHz clock output.		

5.2 Pin Layout

Pin No.	Terminal	I/O	Note
1	VDD	—	
2	SDAT	I2	
3	REQ	O	
4	D_R	O	
5	VSS	—	
6	MODE1	I	
7	MODE0	I	
8	TST1	I	L fixed(test input)
9	OPT1	I	Setting input
10	OPT0	I	Setting input
11	TST0	I	L fixed(test input)
12	VSS	—	
13	X1	I x	
14	VDD	—	
15	X2	O x	
16	VSS	—	
17	D39	O	
18	D38	O	
19	D37	O	
20	D36	O	
21	D35	O	
22	D34	O	
23	D33	O	
24	D32	O	
25	VSS	—	
26	VDD	—	
27	CLKOUT	O	
28	VSS	—	
29	/CS_XEA2	I	
30	/WR_XEA1	I	
31	/OE_XEA0	I	
32	A5_BR	I	
33	A4_CMD4	I	
34	A3_CMD3	I	
35	A2_CMD2	I	
36	A1_CMD1	I	
37	A0_CMD0	I	
38	VSS	—	
39	VDD	—	
40	TSTEN	I	L fixed(test input)
41	INP0	I	L fixed(test input)
42	INP1	I	L fixed(test input)
43	INP2	I	L fixed(test input)
44	OUT3	O	(test output)
45	VSS	—	
46	ALARM	O	
47	TMOUT	O	
48	/BUSY	O	
49	/EOF	O	
50	VSS	—	

Pin No.	Terminal	I/O	Note
51	VDD	—	
52	MDS	I	
53	/STRG	I	
54	VSS	—	
55	D31	I/O	
56	D30	I/O	
57	D29	I/O	
58	D28	I/O	
59	VDD	—	
60	D27	I/O	
61	D26	I/O	
62	D25	I/O	
63	D24	I/O	
64	VSS	—	
65	VDD	—	
66	D23	I/O	
67	D22	I/O	
68	D21	I/O	
69	D20	I/O	
70	VSS	—	
71	D19	I/O	
72	D18	I/O	
73	D17	I/O	
74	D16	I/O	
75	VSS	—	
76	VDD	—	
77	IOSEL	O	
78	D15	I/O	
79	D14	I/O	
80	D13	I/O	
81	D12	I/O	
82	VSS	—	
83	D11	I/O	
84	D10	I/O	
85	D9	I/O	
86	D8	I/O	
87	VSS	—	
88	VDD	—	
89	D7	I/O	
90	D6	I/O	
91	D5	I/O	
92	D4	I/O	
93	VSS	—	
94	D3	I/O	
95	D2	I/O	
96	D1	I/O	
97	D0	I/O	
98	VDD	—	
99	/RESET	I1	
100	VSS	—	

Note) I/O buffer types

- I CMOS level input buffer
- I₁ CMOS level input buffer, Schmitt input
- I₂ CMOS level input buffer, 5V tolerant (when 3.3V operation)
- O CMOS level output buffer
- I/O CMOS level interactive buffer, 50k Ω pull-up
- I_x, O_x Oscillation buffer

6. Operation mode setting (MODE)

Operation modes are roughly classified into the CPU mode and the manual mode. Taking into consideration the control bus settings, the following three modes are available.

MODE1	MODE0	Function	Remarks
1	×	Manual mode	40-bit output. D[39:0]
0	0	16-bit CPU mode	16-bit bus output. D[15:0]
0	1	32-bit CPU mode	32-bit bus output. D[31:0]

7. CPU Mode Operation

7.1 Basic Operation

After writing commands and memory data (write data and address data) into the RAS102, when a trigger signal to start a transmission is input from the CPU or the external trigger input terminal (EXT_STRG) in accordance with the contents of the trigger input setting register, a transmission process for command data is started.

(1) CPU control

When the data is written to the transmission trigger register, a specified command starts being transmitted to the encoder.

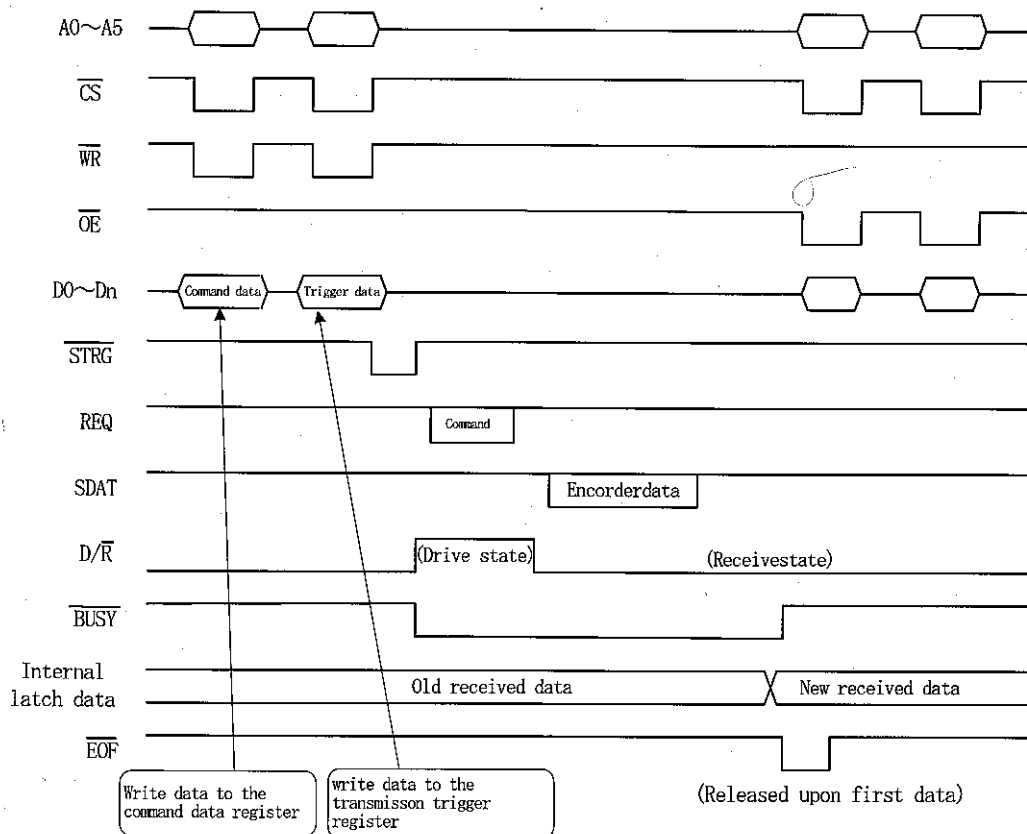
(2) External trigger input

When a trigger signal is directly input to the external input terminal (EXT_STRG), a specified command starts being transmitted to the encoder.

Received encoder data is set to each output register, and an EOF signal (L-level) is output when the communication is completed. The EOF is released when the output register is read for the first time, and the transmission of a next command becomes available at this point.

During a communication process, a BUSY signal is output (L-level).

7.2 Transmission/Reception Control Timings



7.3 Block Selection (Chip Select)

Internal chip select	A5	A4	A3	Remarks
CS1	0	0	1	Enable control (R/W) of block transmission and reception
CS4	1	0	0	Enable control (write) of the trigger input setting register and the transmission block selection register
CS5	1	0	1	Enable baud rate setting
-	Other than those above			Not defined

7.4 Data bus Input/Output Control(IOSEL)

/CS	/OE	/WR	Operation Mode	State of IOSEL
1	×	×	No selection	H
0	1	1	Read	L
0	0	1	Read	
0	×	0	Write	H

7.5 Read Address (common in 16 bits and 32 bits)

MODE1	MODE0	CS	/OE	/WR	A5	A4	A3	A2	A1	A0	Description
1	×	×	×	×	×	×	×	×	×	×	Manual mode
0	×	0	0	1	0	0	1	×	×	×	Various data of Encoder (See Chapter 11 for data address)

For more information, see Chapter 11 (I/O Register) and Section 7.11 (Operation Timings).

7.6 Write Address (in the case of 16-bit bus mode)

MODE1	MODE0	/CS	/OE	/WR	A5	A4	A3	A2	A1	A0	Description
1	×	×	×	×	×	×	×	×	×	×	Manual mode
0	×	0	1	0	0	0	1	0	0	0	Command code/ Encoder address
0	×	0	1	0	0	0	1	0	0	1	EEPROM write data
0	×	0	1	0	0	0	1	0	1	0	EEPROM address
0	×	0	1	0	1	0	0	×	×	0	Trigger input setting register
0	×	0	1	0	1	0	0	×	×	1	Transmission block selection register
0	×	0	1	0	1	0	1	×	×	×	Baud rate setting register

For more information, see Chapter 11 (I/O Register) and Section 7.11 (Operation Timings).

7.7 Input Register

7.7.1 Command Configuration

(1) 1-frame command (CDF0-12)

Location data request/various clear requests/EC address setting/One rotation data zero preset

Command data

(2) 2-frame command (CDF13) Command data

EEPROM data read

Command data	Read Address (8bit)
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(3) 4-frame command (CDF14)

EEPROM data write

Command data	Write data (lower8bit)	Write data (upper8bit)	Read Address (8bit)
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7.7.2 Command Data Register

A command register makes settings for encoder addresses and command codes. For more information, see Chapter 11 (I/O Register).

(Up to bit 15 in the case of the 16-bit bus setting)

Bit	31	~	16	15	~	8	7	6	5	4	3	2	1	0
	0		0			CC4	CC3	CC2	CC1	CC0	XEA2	XEA1	XEA0	
Default						0	0	0	0	0	0	0	0	0

(1) Command Code Settings

Command code	CC4	CC3	CC2	CC1	CC0	Segment	Remarks
CDF0	0	0	0	0	0	Request data (individual mode)	Abusolute full data request
CDF1	0	0	0	0	1		Abusolute lower 24-bit data request
CDF2	0	0	0	1	0		Abusolute upper 24-bit data request
CDF3	0	0	0	1	1		Encorder status request
CDF4	0	0	1	0	0	Request data (continuous mode)	Not support
CDF5	0	0	1	0	1		
CDF6	0	0	1	1	0		
CDF7	0	0	1	1	1		
CDF8	0	1	0	0	0	Operation request (individual mode)	Status flag clear request
CDF9	0	1	0	0	1		Multiple rotation data clear request
CDF10	0	1	0	1	0		Status + Multiple rotation data cleae request
CDF11	0	1	0	1	1		Encorder address setting
CDF12	0	1	1	0	0		One rotation data zero preset
CDF13	0	1	1	0	1	Memory access request (individual mode)	Memory read request
CDF14	0	1	1	1	0		Memory write request
CDF15	0	1	1	1	1	Request data	Temperature data
CDF16~31	Other than those above					Not defined	

7.7.5 Trigger Input Setting Register

An output control method for a transmission start trigger signal (STRG; see Chapter 5 Internal Configuration), is selected. For more information, see Chapter 11 (I/O Register).

(Up to bit 15 in the case of a 16-bit bus setting)

bit	31	~	16	15	~	4	3	2	1	0
	0			0			0	0	EXT	0
Default	0									

EXT = 0/A trigger signal is controlled by the CPU.

= 1/A trigger signal is treated as an external input

7.7.6 Transmission Trigger Register

In the case that the CPU control is selected from the trigger input setting register, a transmission start trigger signal (STRG; see Chapter 5 Internal Configuration) is output in accordance with the bit setting. In the case that the external control is selected, the data in this register becomes invalid (masked).

The bits of this register are reset with the rise (i.e., when the output data is read for the first time) of an EOF signal, which is output when communication with the encoder is completed. For more information, see Chapter 11 (I/O Register).

(Up to bit 15 in the case of a 16-bit bus setting)

bit	31	~	16	15	~	4	3	2	1	0
	0			0			0	0	TRG	0
Default	0									

TRG: = 0 / A transmission start trigger signal is not output

= 1 / A transmission start trigger signal is output

7.7.8 Communication baud rate setting register

It is usually set to 2.5 Mbps (when the power is turned on).

The baud rate can be changed by rewriting the setting of the internal register.

For more information, see Chapter 11 (I/O Register).

bit	31	~	16	15	~	4	3	2	1	0
	0			0			0	0	0	BR
Default										0

BR	Baud Rate
0	2.5 Mbps
1	4.0 Mbps

7.8 Other Input

7.8.1 OPT 0 Terminal

This is an input terminal to set a control method when reading EEPROM data (CDF13). In the case of EEPROM data read, valid read data can be obtained only after CDF13 command is transmitted to an encoder twice (reference: Encoder M30A/M35A Specifications). The OPT 0 terminal is a setting input terminal to select whether the second transmission is controlled by the RAS102 or by the CPU.

OPT0	Function
0	EEPROM data read is controlled by the RAS102. (*1) A read operation becomes available after the CPU issues a command for EEPROM data read. In the meantime, it becomes the communication state (/BUSY = L) during approx. 350-375 μ s of data read.
1	EEPROM data read is controlled by the upper CPU. The first and second commands for EEPROM data read can be controlled by the CPU.

*1 When using this mode, verify that the “BUSY” or “MEMBUSY” flag is not set to the encoder status just before transmitting CDF13.

7.8.2 OPT 1 Terminal

This is to enable to select the timing for t2 in Chapter 9 “Serial Data Transmission/Reception Timings.”

For more information, see Chapter 9.

7.9 Output Register

Various data of received encoder data are written to the output register in accordance with a transmitted command.

For information on the contents of output data, see Chapter 11.

7.9.1 Encoder Status

Bit	Status Flag
ES0	BUSY + MEMBUSY
ES1	BATT
ES2	OVSPD + MEMERR + OVTEMP
ES3	STERR + PSERR + MTERR + INCERR*2

*1 For more information on the encoder status, see the specifications for the encoder M30A/M35A.

*2 INCERR is supported only by the M35A.

7.9.2 Communication Alarm

Bit	Status Flag	Remarks
CA0	CMD	The transmitted command and the received command do not match.
CA1	FORM	The logical sum of the start bits and the stop bits of all the fields does not match. Or the received data length after IF is insufficient.
CA2	SYNC	Received data fail to be returned within a designated period of time after a command is transmitted.
CA3	CRC	CRC generated by the received data and the transmitted CRC do not match.

* CRC code: A computing range of the received data for a CRC code include all bits except the start bit and the stop bit for each field (IF and DFn).

Generative polynomial equation $G(x) = X^8 + X^4 + X^3 + X^2 + 1$

7.9.3 Alarm Flag (AF)

The logical sum of the encoder status (Section 7.9.1) and the communication alarm (Section 7.9.2) is output.

An output format in which an alarm flag is assigned at the most significant bit (MSB) of each data can be selected.

7.10 Other Output

7.10.1 BUSY Signal (output to each block)

In both the CPU mode and the manual mode, the output becomes L level just before communication starts, and it returns to H level after the received encoder data is set to the output register.

7.10.2 EOF Signal

In the CPU mode, L level is output after the received encoder data is stored in the output register, and a series of receiving and transmitting operations are completed. When output data read is performed for the first time after the output, the EOF signal is reset, and the output returns to H level.

The bits of the transmission trigger register which an EOF signal is output are reset by this signal.

7.10.3 TMOUT Signal

In both the CPU mode and the manual mode, if data fail to be returned in response to a request signal within a designated period of time, H level is output..

It is released when the next communication starts.

When a period of time from when the transmission of command data is completed to

when encoder data is received (i.e., until a start bit is detected) exceeds the criteria listed in the table below, it considers as an error.

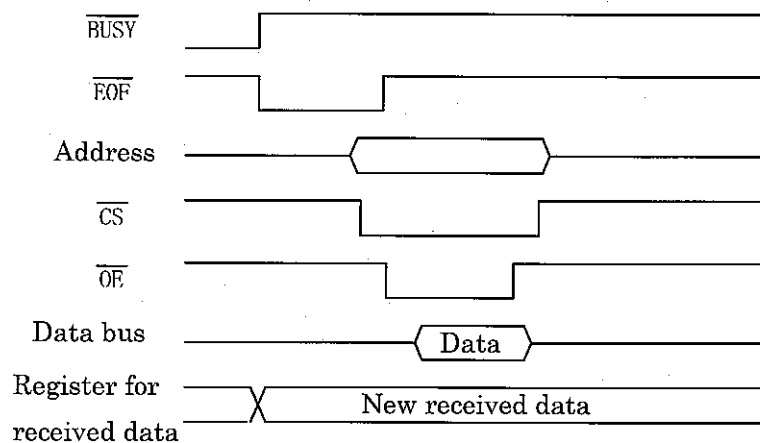
Mode	Communication Baud Rate	Criteria
Individual Mode	2.5 Mbps	t5 (+2.0us, -0.5us)
	4.0 Mbps	t5 (+2.0us, -0.3us)

Note) For information on the values of t5 , see Chapter 9.

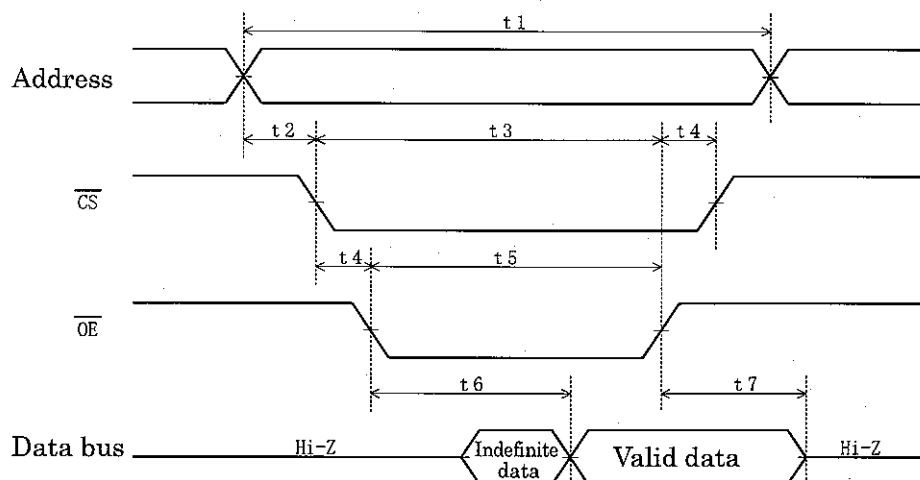
7.11 Read/Write Operations

7.11.1 Read Cycle / Timing Chart

(1)Control Timing



(2)Timing Chart



[Common in VCC = 5V / VCC = 3.3V]

Time	Standards		Unit
	MIN	MAX	
t_1	100		ns
t_2	0		ns
t_3	100		ns
t_4	0		ns
t_5	100		ns
t_6		72 (82)	ns
t_7		17(33)	ns

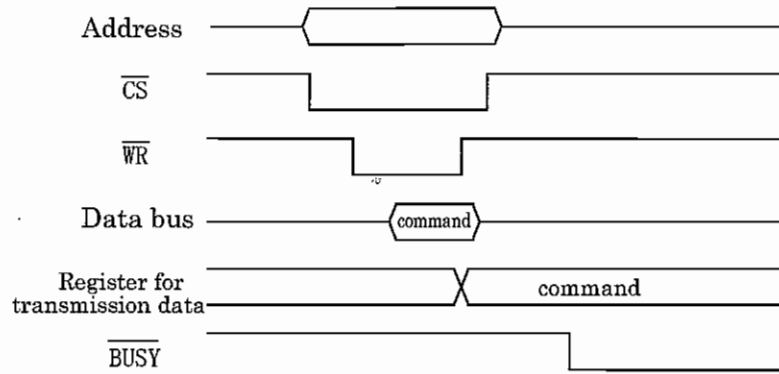
Note) The values of t_6 and t_7 in parentheses are those for 3.3V operation.

Note) When conducting the read cycle operation continuously, take 50ns or more for the

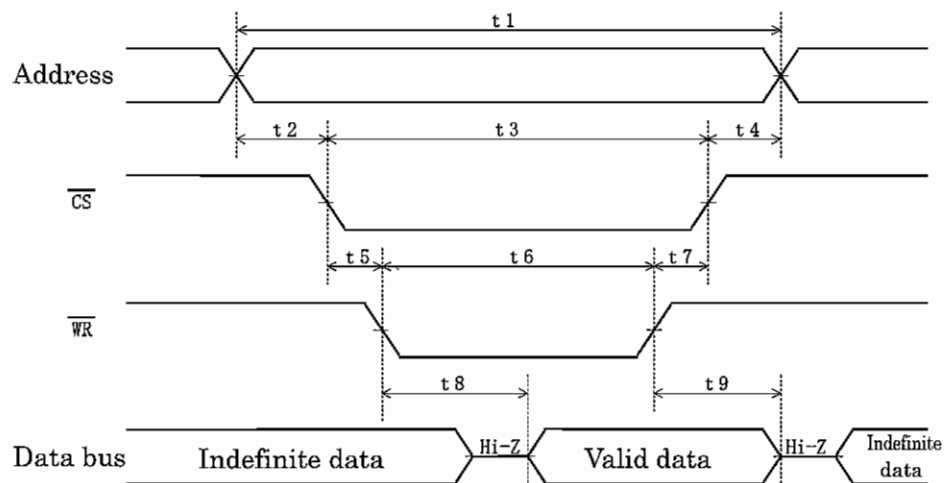
non-active time (H) of /CS and /OE signals.

7.11.2 Write Cycle / Timing Chart

(1) Control Timing



(2) Timing Chart



[Common in VCC = 5V / VCC = 3.3V]

Time	Standards		Unit
	MIN	MAX	
t 1	100		ns
t 2	0		ns
t 3	100		ns
t 4	0		ns
t 5	0		ns
t 6	100		ns
t 7	0		ns
t 8		50	ns
t 9	0		ns

Note) When conducting the write cycle operation continuously, take 50ns or more for the non-active time (H) of /CS and /WR signals.

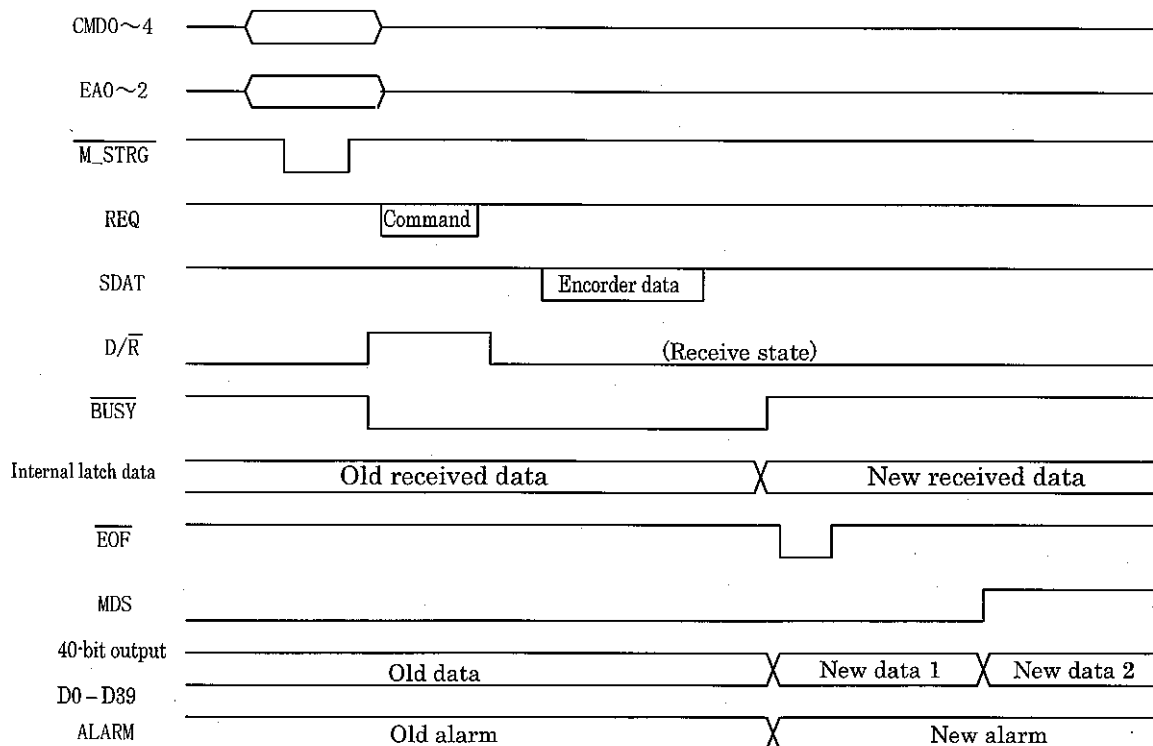
8. Manual Mode Operation

Encoder addresses, and command codes to be used for communication to an appropriate setting input terminal, and then input a start trigger signal (negative pulse) from the M_STRG terminal. A start trigger signal is output the rise of the signal starts the transmission process of command data in accordance with the settings of encoder addresses and command codes.

The received encoder data is stored in each register, an EOF signal in L-pulse is output when the communication is completed.

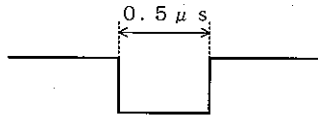
The manual mode does not support that process of EEPROM data read/write and communication through a bus connection.

8.1 Transmission/Reception Control Timing



8.2 EOF Signal

When encoder data is stored in the output register after communication is completed, the BUSY signal is released, and L-pulse with the pulse width given in the following figure is output



8.3 Encoder Address Setting

In accordance with the table below, set address data of the encoder which controls communication to the input terminal.

Terminal Name			Encoder Segment
XEA2	XEA1	XEA0	
0	0	0	ENC1
0	0	1	ENC2
0	1	0	ENC3
0	1	1	ENC4
1	0	0	ENC5
1	0	1	ENC6
1	1	0	ENC7
1	1	1	ENC8

8.4 Command Code Setting

In accordance with the table below, set command data which is going to be transmitted to the encoder to the input terminal.

CDF13,14(EEPROM control) in CPU mode is not support.

Frame Name	Terminal Name					Segment	Remarks
	CMD4	CMD3	CMD2	CMD1	CMD0		
CDF0	0	0	0	0	0	Data request (individual mode)	Absolute full data request
CDF1	0	0	0	0	1		Absolute lower 24-bit data request
CDF2	0	0	0	1	0		Absolute upper 24-bit data request
CDF3	0	0	0	1	1		Encoder status request
CDF8	0	1	0	0	0	Operation request (individual mode)	Status flag clear request
CDF9	0	1	0	0	1		Multiple rotation data clear request
CDF10	0	1	0	1	0		Status + multiple rotation data clear request
CDF11	0	1	0	1	1		Encoder address change request
CDF12	0	1	1	0	0	Data request (individual)	One rotation data zero preset
CDF15	0	1	1	1	1		Temperature data (10 bits) request

8.6 Communication Baud Rate Setting

In accordance with the table below, set the communication baud rate.

Terminal Name	Baud Rate Setting
BR	
0	2.5 Mbps
1	4.0 Mbps

8.7 Output Data

8.7.1 40-bit Parallel Output

Output contents are switched in accordance with the setting of the MDS terminal. For more information, see Chapter 12.

8.7.2 Alarm Logical Sum Output

Output terminal: ALARM

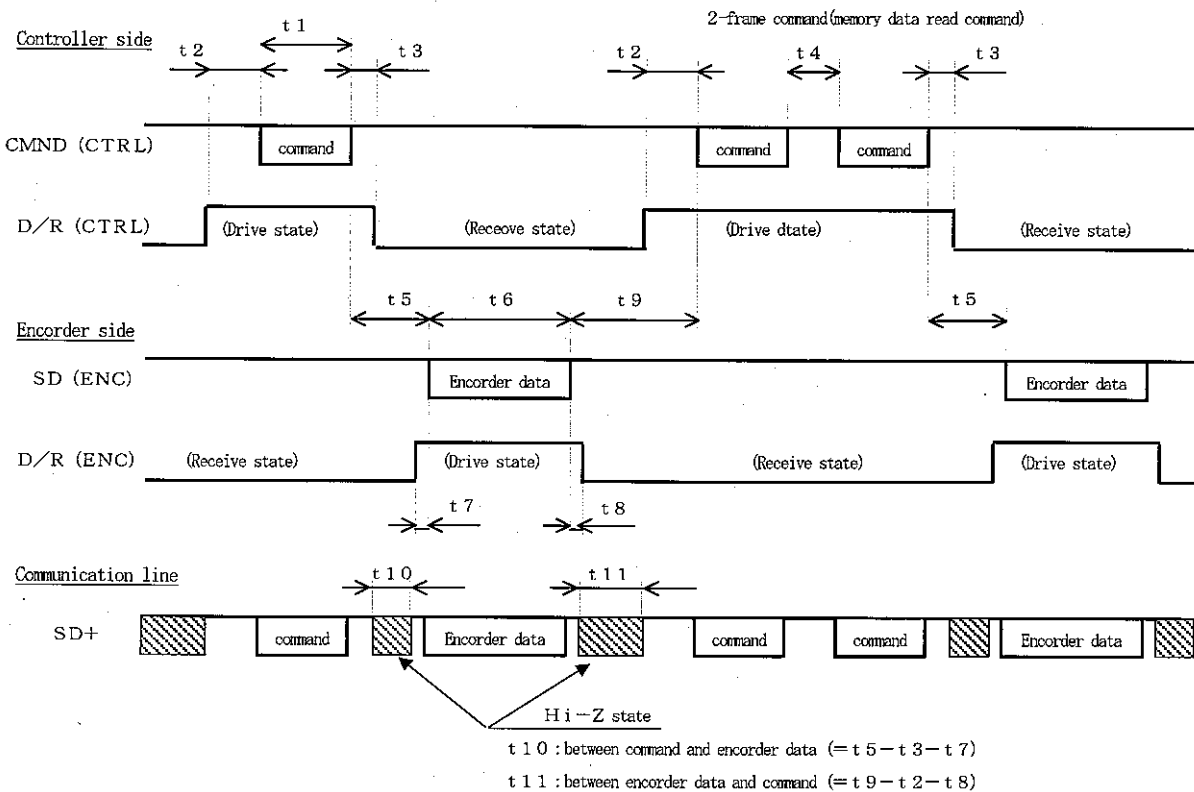
Only in the manual mode, regardless of the input state of the MDS terminal, the logic sum of the encoder status and the communication alarm is output. The output data is retained until next received data is obtained.

In the CPU mode, the logic sum is not output, and L-level remains unchanged.

9. Serial Data Transmission/Reception Timings

9.1 Timing Chart

9.1.1 Individual Mode



Time	Transmission Speed		Time	Transmission Speed	
	2.5 Mbps	4 Mbps		2.5 Mbps	4 Mbps
t_1	7.2 μ s	4.5 μ s	t_7	200 ns	50 ns
t_2 (OPT1 = 0)	7.95 μ s	5.35 μ s	t_8	200 ns	150 ns
t_2 (OPT1 = 1)	750 ns	600 ns	t_9	10 μ s (MIN)	7 μ s (MIN)
t_3	50 ns	50 ns	t_{10}	2.75 μ s	1.9 μ s
t_4	10 μ s (Min)	7 μ s (Min)	t_{11}	1.85 μ s (MIN)	1.5 μ s (MIN)
t_5	3 μ s	2 μ s			
t_6	21.6/28.8 μ s	13.5/18 μ s			

Note1) It is assumed that the delay of the transmission path and the propagation delay of the transmission/reception circuits are "0."

Note 2) The timing for t_2 can be set with the OPT1 terminal.

Note 3) In case of long-distance transmission (becomes 30m or more), there is the necessity of setting the t_3 time for a long (1-1.5 μ s), in order to prevent incorrect of an error which of TMOUT. For more

information on long-distance transmission, see Chapter 13 (Example of Application Circuit)

9.2 Detection of Encoder Data

(1) Verification of the response waiting time

↓ OK

(2) Detection of the start bit

↓ OK

(3) Detection of the sync code

↓ OK

(4) Read of the main data

↓ OK

(5) Detection of the stop bit

↓ OK

(6) Detection of the start bit

↓ OK

(7) Read of the main data

↓ OK

(8) Detection of the stop bit

↓ OK



Repeat the number of times equivalent to the number of the data fields

(9) Judgment of acceptable or unacceptable using the CRC code

(10) End of reception

10. Clock Oscillation Circuit

An oscillation circuit is constituted by connecting a crystal oscillator to the X1 and X2 terminals.

Clock frequency: 20 MHz

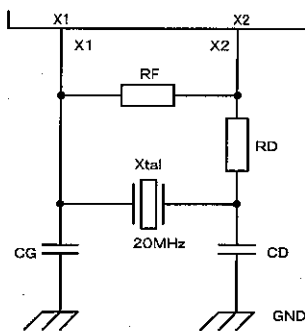
Frequency deviation: within $\pm 100\text{ppm}$

See the information given below for the recommended circuit.

An appropriate circuit configuration and values of the constants must be selected according to an oscillator to be used.

<Configuration of an oscillation circuit>

(1) Example of a circuit with internal oscillation

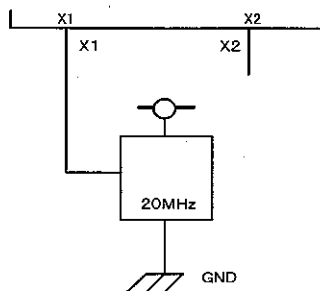


Reference Values for Circuit Constants

Xtal: FA-238 (20 MHz, Seiko Epson Corp.)

	VCC = 5.0V	VCC = 3.3V
RF	1 M Ω	1 M Ω
RD	390 Ω	240 Ω
CG,CD	6 pF	5 pF

2) Example of a circuit with external oscillation



11. I/O Register (CPU Mode)

11.1 16-bit Bus Mode

11.1.1. Write Data

- Internal chip select: CS1

A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	1	0	0	0	0	0	0	0	0	0	0	0	Command code[4:0]				EC address[2:0]				
0	0	1	0	0	1	16bit EEPROM data																LSB
0	0	1	0	1	0	0	0	0	0	0	0	0	0	MSB	8bit EEPROM address						LSB	

- Internal chip select: CS4

A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	×	×	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EXT	0
1	0	0	×	×	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TRG	0

- Internal chip select: CS5

A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	×	×	×	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	BR

Note) × : Don't care

11.1.2 Read Data

Internal chip select: CS1

CDF	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0			
0	0	0	1	0	0	0	Communication alarm CA[3:0]				EC status ES[3:0]				Command code[4:0]				EC address[2:0]						
	0	0	1	0	0	1	ABS 40bit full data (ABS[15:0])															LSB			
	0	0	1	0	1	0	ABS 40bit full data (ABS[31:16])																		
	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	MSB ABS 40bit full data (ABS[39:32])									
	0	0	1	1	0	1	AF	ABS 40bitfull data (ABS[14:0])															LSB		
	0	0	1	1	1	0	AF	ABS 40bit full data (ABS[29:15])																	
1	0	0	1	1	1	1	AF	0	0	0	0	0	0	MSB	ABS 40bitfull data (ABS[39:30])										
	0	0	1	0	0	0	Communication alarm CA[3:0]				EC status ES[3:0]				Command code[4:0]				EC address[2:0]						
	0	0	1	0	0	1	ABS Lower24bit data (ABS[15:0])															LSB			
	0	0	1	0	1	0	0	0	0	0	0	0	0	0	MSB	ABS Lower 24bit data (ABS[23:16])									
	0	0	1	1	0	1	AF	ABS Lower 24bit data (ABS[14:0])															LSB		
2	0	0	1	1	1	0	AF	0	0	0	0	0	0	0	MSB	ABS Lower 24bit data (ABS[23:15])									
	0	0	1	0	0	0	Communication alarm CA[3:0]				EC status ES[3:0]				Command code[4:0]				EC address [2:0]						
	0	0	1	0	0	1	ABS Upper 24bit data (ABS[31:16])															LSB			
	0	0	1	0	1	0	0	0	0	0	0	0	0	0	MSB	ABS Upper 24bit data (ABS[39:32])									
	0	0	1	1	0	1	AF	ABS Upper 24bit data (ABS[30:16])															LSB		
3, 8~ 12	0	0	1	1	1	0	AF	0	0	0	0	0	0	0	MSB	ABS Upper 24bit data (ABS[39:31])									
	0	0	1	0	0	0	Communication alarm CA[3:0]				EC status ES[3:0]				Command code [4:0]				EC address[2:0]						
13, 14	Status code (ALM[15:0])																								
	0	0	1	0	0	0	Communication alarm CA[3:0]				EC status ES[3:0]				Command code [4:0]				EC address [2:0]						
	0	0	1	0	0	1	MSB 16bit EEPROM data															LSB			
	0	0	1	0	1	0	0	0	0	0	0	0	0	0	MSB	8bit EEPROM address							LSB		
15 ※1	0	0	1	1	1	0	AF	0	0	0	0	0	0	0	0	MSB	8bit EEPROM address							LSB	
	0	0	1	0	0	0	Communication alarm CA[3:0]				EC status ES[3:0]				Command code [4:0]				EC address [2:0]						
	0	0	1	0	0	1	AF	0	0	0	0	0	0	MSB	10bit temperature data (DB[9:0])							LSB			

*1, CDF15 is not supported by M30A

[illegible]

11.2.2 Read Data

Internal chip select: CS1

CDF	A5	A4	A3	A2	A1	A0	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																				
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Communication alarm CA[3:0]				EC status			Command code [4:0]			EC address [2:0]																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																									
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	0	0	1	0	1	0	AF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

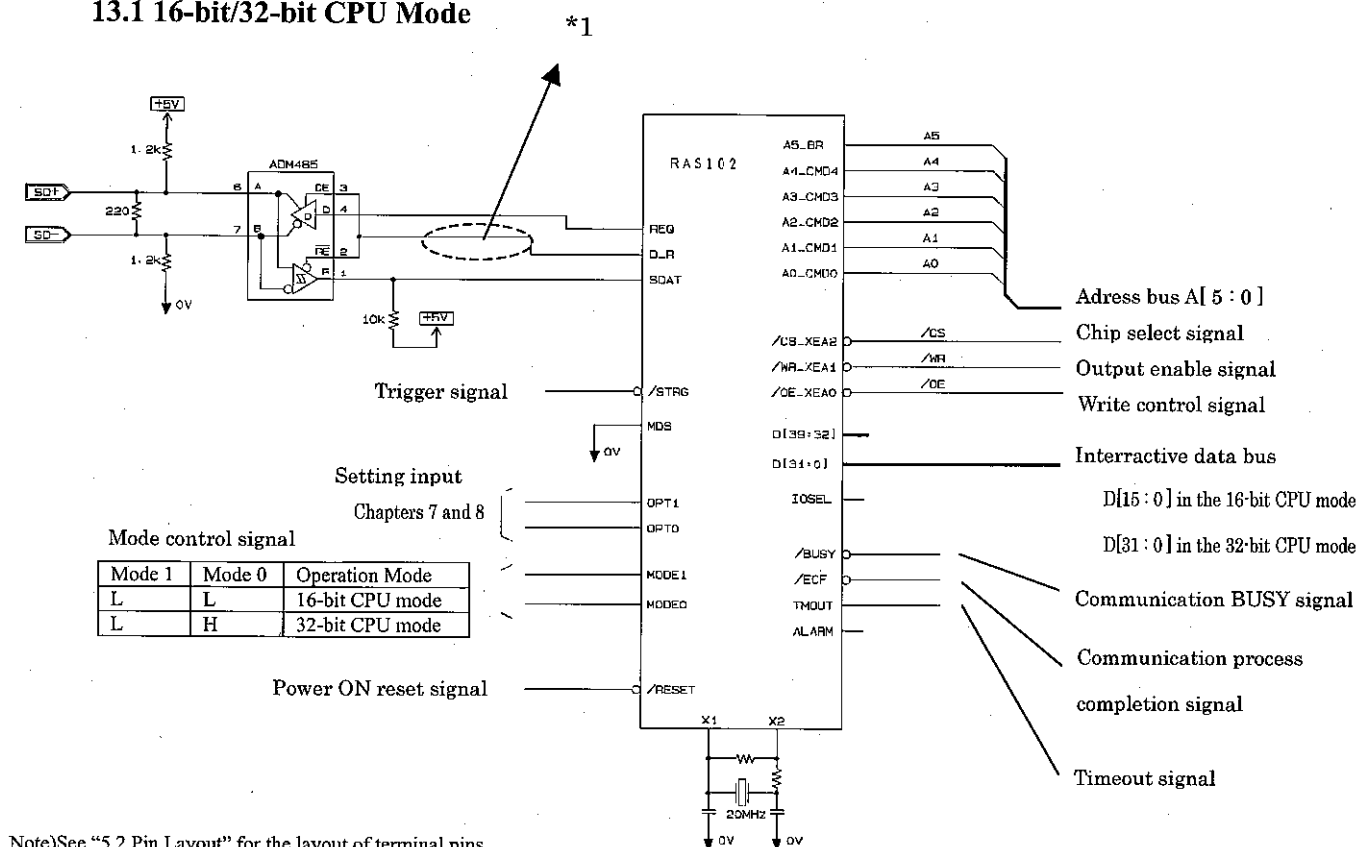
*1,CDF15 is not supported by M30A

12.Manual Mode Output

CDF	MSB	D39	D38	D37	D36	D35	D34	D33	D32	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Communication alarm CA[3:0]				EC status ES[3:0]			Command code [4:0]			EC address [2:0]						
	0	MSB ABS 40bit full data (ABS[39:0]) LSB																																							
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Communication alarm CA[3:0]				EC status ES[3:0]			Command code [4:0]			EC address [2:0]						
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	MSB ABS lower 24bit data (ABS[23:0]) LSB																							
2	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Communication alarm CA[3:0]				EC status ES[3:0]			Command code [4:0]			EC address [2:0]						
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	MSB ABS upper24bit data (ABS[39:16]) LSB																							
3,8~12	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Communication alarm CA[3:0]				EC status ES[3:0]			Command code [4:0]			EC address [2:0]						
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Status code' (ALM[15:0])																
15※1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Communication alarm CA[3:0]				EC status ES[3:0]			Command code [4:0]			EC address [2:0]						
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	MSB 10bit temperature data (DB[9:0]) LSB								

13. Example of Application Circuit

13.1 16-bit/32-bit CPU Mode

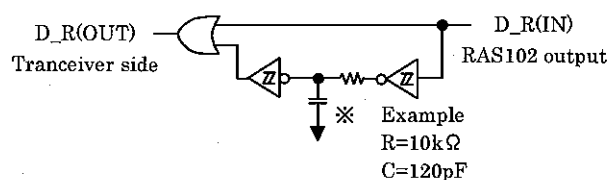


Note) See "5.2 Pin Layout" for the layout of terminal pins.

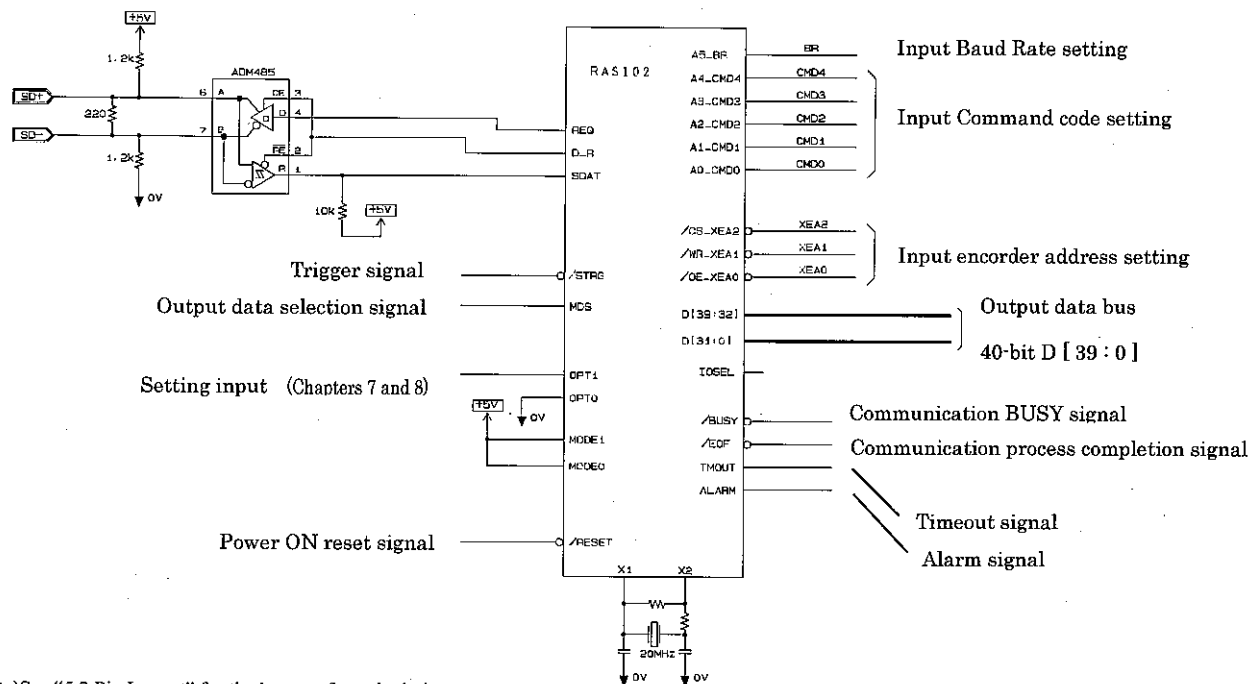
Terminals D16 to D32 must be open in the case of the 16-bit CPU mode

*1: Points to note in the case of a long-distance transmission

If the communication path length between the encoder and the controller becomes 30m or more, insert the circuit below into the D_R signal line.



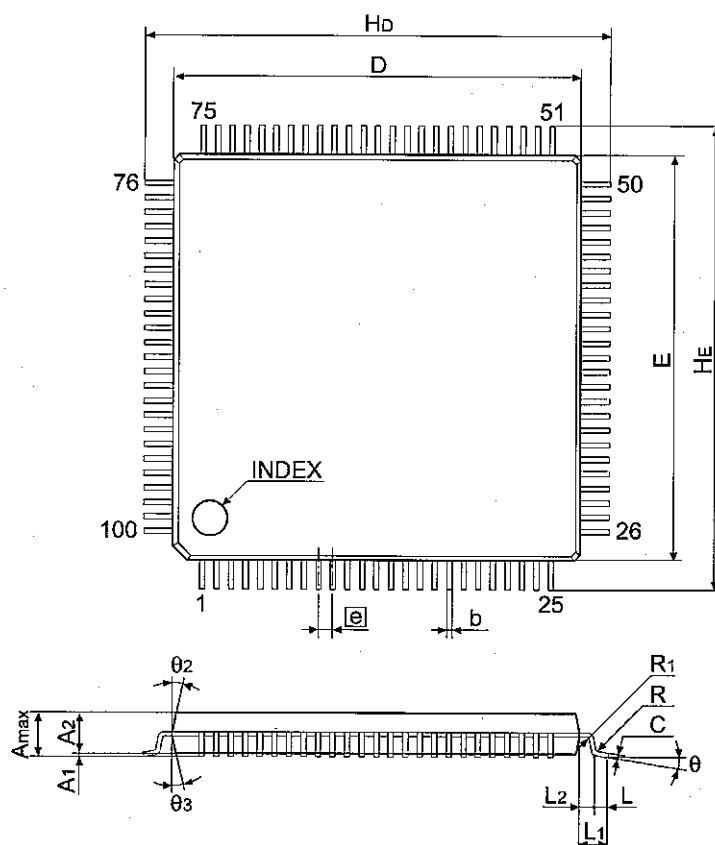
1 3. 2 Manual Mode



Note) See "5.2 Pin Layout" for the layout of terminal pins.

14. Packaging dimension

Plastic QFP 100pin Body size 14 x 14 x 1.4mm(QFP15)



Lead type STD (QFP15-100pin STD)						
Symbol	Dimension in Millimeters			Dimension in Inches *		
	Min.	Nom.	Max.	Min.	Nom.	Max.
E	13.9	14	14.1	(0.548)	(0.551)	(0.555)
D	13.9	14	14.1	(0.548)	(0.551)	(0.555)
A			1.7			(0.066)
A1		0.1			(0.004)	
A2	1.3	1.4	1.5	(0.052)	(0.055)	(0.059)
e		0.5			(0.020)	
b	0.13	0.18	0.28	(0.006)	(0.007)	(0.011)
C	0.1	0.125	0.175	(0.004)	(0.005)	(0.006)
θ	0°		10°	(0°)		(10°)
L	0.3	0.5	0.7	(0.012)	(0.020)	(0.027)
L1		1			(0.039)	
L2		0.5			(0.020)	
HE	15.6	16	16.4	(0.615)	(0.630)	(0.645)
HD	15.6	16	16.4	(0.615)	(0.630)	(0.645)
θ2		12°			(12°)	
θ3		12°			(12°)	
R		0.2			(0.008)	
R1		0.2			(0.008)	

* for reference