Operational Multiplier

GENERAL DESCRIPTION

The XR-2208 operational multiplier combines a four-quadrant analog multiplier (or modulator), a high frequency buffer amplifier, and an operational amplifier in a monolithic circuit that is ideally suited for both analog computation and communications signal processing application. As shown in the functional block diagram, for maximum versatility the multiplier and operational amplifier sections are not internally connected. They can be interconnected, with a minimum number of external components, to perform arithmetic computation, such as multiplication, division, square-root extraction. The operational amplifier can also function as a preamplifier for low-level input signals, or as a post detection amplifier for synchronous demodulator applications. For signal processing, the high frequency buffer amplifier output is available at pin 15. This multiplier/buffer amplifier combination extends the small signal 3-db bandwidth to 8-MHz and the transconductance bandwidth to 100MHz.

The XR-2208 operates over a wide range of supply voltages, ±4.5V to ±16V. Current and voltage levels are internally regulated to provide excellent power supply rejection and temperature stability. The XR-2208 operates over a 0°C to 70°C temperature range. The XR-2208M is specified for operation over the military temperature range of –55°C to +125°C.

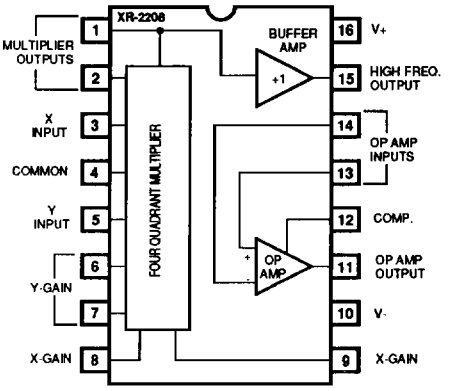
FEATURES

Maximum Versatility
  Independent Multiplier, Op Amp, and Buffer
Excellent Linearity (0.3% typ.)
Wide Bandwidth
  3 dB B.W. — 8MHz typ.
  3° Phase Shift B.W. — 1.2MHz typ.
  Transconductance B.W. — 100MHz typ.
Simplified Offset Adjustments
Wide Supply Voltage Range (±4.5V to ±16V)

ABSOLUTE MAXIMUM RATINGS

Power Supply V+	+18 Volts
V–	–18 Volts
Power Dissipation	
Ceramic Package	750mW
Derate above +25°C	6mW/°C
Plastic Package	625mW
Derate above + 25°C	5mW/°C
Storage Temperature Range	–65°C to +150°C

PIN ASSIGNMENT



APPLICATIONS

Analog Computation
  Multiplication
  Division
  Squaring
  Square-Root
Signal Processing
  AM Generation
  Frequency Doubling
  Frequency Translation
  Synchronous AM Detection
  Triangle-to-Sinewave Converter
  AGC Amplifier
  Phase Detector
Phase-Locked Loop (PLL)
Applications
  Motor Speed Control
  Precision PLL
  Carrier Detection
  Phase-Locked AM Demodulation

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2208M	Ceramic	–55°C to +125°C
XR-2208N	Ceramic	0°C to +70°C
XR-2208P	Plastic	0°C to +70°C
XR-2208CN	Ceramic	0°C to +70°C
XR-2208CP	Plastic	0°C to +70°C

ELECTRICAL CHARACTERISTICS

Test Conditions: Supply Voltage = ±15V, T_A = 25°C, unless otherwise specified.

PARAMETERS	XR-2208/ XR-2208M MIN	XR-2208/ XR-2208M TYP	XR-2208/ XR-2208M MAX	XR-2208C MIN	XR-2208C TYP	XR-2208C MAX	UNITS	FIGURES	CONDITIONS
GENERAL									
Supply Voltage	±4.5		±16	±4.5		±16	Vdc		See Figure 11
Supply Current		4	7		5	8	mA	2	Measured at Pin 16
MULTIPLIER SECTION									
Non-linearity (Output Error in % of Full Scale)		0.3	0.5		0.5	1.0	%	3	No external offset trim $V_y = \pm 10V, -10V < V_x < +10V$
		0.3	0.5		0.5	1.0	%		$V_x = \pm 10V, -10V < V_y < +10V$
		0.7	1.0		0.8		%		$T_{LOW} \le T_A \le T_{HIGH}$ (Note 1)
Feedthrough									f = 50Hz
a) With Offset Adj.									
X-input		45	80		70	120	mVp-p		V_x = 20 Vp-p, V_y = 0
Y-input		60	100		90	150	mVp-p		V_y = 20 Vp-p, V_x = 0
b) No Offset Adj.									
X-input		120			200		mVp-p		V_x = 20 Vp-p, V_x = 0
Y-input		120			200		mVp-p		V_y = 20 Vp-p, V_x = 0
Temperature Coefficient of Scale Factor		±0.07			±0.07		%/°C		$T_{LOW} \le T_A \le T_{HIGH}$ (Note 1)
Input Bias Current									
X, Y input		2	6		3	8	µA	2	I_3, I_5 of Figure 2
Common input		4	12		6	16	µA	2	I_4 of Figure 2
Input Resistance	0.5	1.0			1.0		MΩ	2	Measured looking into Pin 3 or Pin 5
Output Offset Voltage		50	80		80	140	mV	2	Measured across Pins 1 and 2
Avg. Temp. Drift		0.5			0.5		mV/°C		$T_{LOW} \le T_A \le T_{HIGH}$
Dynamic Response								5	See Definition Section
3-dB Bandwidth									
X-input	6	8		6	8		MHz		
Y-input	3	4		3	4		MHz		
3° Phase-Shift Bandwdith		1.2			1.2		MHz		
1% Absolute Error Bandwidth		30			30		kHz		
Transconductance Bandwidth		100			100		MHz		
Output Impedance		6			6		kΩ		Measured looking into Pins 1 or 2
BUFFER AMPLIFIER									
Output Impedance		200			200		Ω	4	Measured looking into Pin 15
Gain	1.0			1.0					
OPERATIONAL AMPLIFIER									
Input Offset Voltage		1	3		2	6	mV	6	$R_S < 50\Omega$
Temperature Coefficient of Input Offset Voltage		6	20		9	30	µV/°C		$T_{LOW} \le T_A \le T_{HIGH}$
Input Offset Current		4	75		10	100	nA	6	$I_{B1} - I_{B2}$
Input Bias Current		30	200		50	300	nA	6	$\frac{I_{B1} + I_{B2}}{2}$
Voltage Gain	70	75		70	75		dB	6	$R_L \ge 2K, V_o = \pm 10V$, f = 20Hz
Differential Input Resistance	0.5	3			3		MΩ	6	
Output Voltage Swing	±10	±12		±10	±12		V		$R_L \ge 2K, T_{LOW} \le T_A \le T_{HIGH}$
Input Common Mode Range	+12 −10	+14 −12		+12 −10	+14 −12		V	6	
Common Mode Rejection	70	90		70	90		dB	6	f = 20 Hz
Output Resistance		2			2		kΩ	6	
Output Short Circuit Current	50 −30	10 −10	30 65		10 −10		mA mA	5 5	Positive Negative
Slew Rate		0.5			0.5		V/µs	7	Gain = 1, $R_L \ge 2K, C_L \le 100pF$ C_C = 20pF
Power Supply Sensitivity		30			30		µV/V	6	$R_S \le 10K$

Note 1: T_{LOW} = −55°C, T_{HIGH} = +125°C for XR-2208M T_{LOW} = 0°C, T_{HIGH} = +70°C for XR-2208/XR-2208C

CAUTION: *When using only the op amp or only the multiplier section of the XR-2208, the input terminals to the unused section must be grounded. Thus, when using the multiplier section alone, ground pins 13 and 14; when using the op amp section alone, ground pins 3, 4 and 5.*

SYSTEM DESCRIPTION

The XR-2208 operational multiplier contains a four-quadrant multiplier with a buffer amplifier for one of the differential outputs for applications requiring high frequency applications. The inputs have a dynamic response of 4MHz (8MHz for the X input) and a transconductance bandwidth of 100MHz for phase detector applications. The fully independent operational amplifier features high gain and a large common mode rejection ratio (90dB). The device can be powered by voltages from 4.5 VDC to 16 VDC.

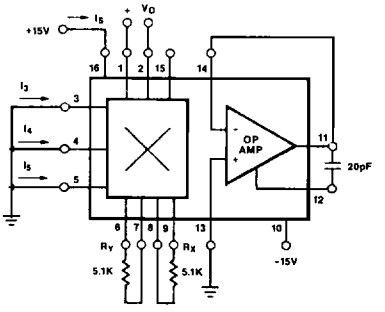


Figure 1. Test Circuit for Quiescent Supply Current, Multiplier Input Bias and Output Offset Voltage.

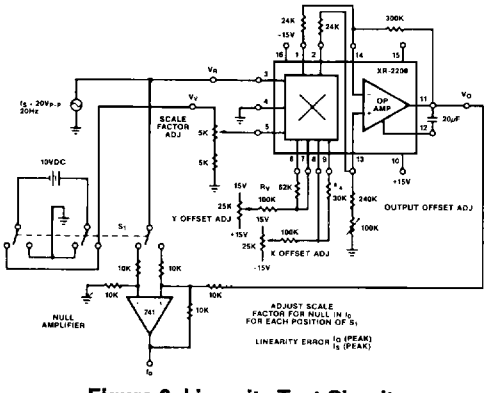


Figure 2. Linearity Test Circuit

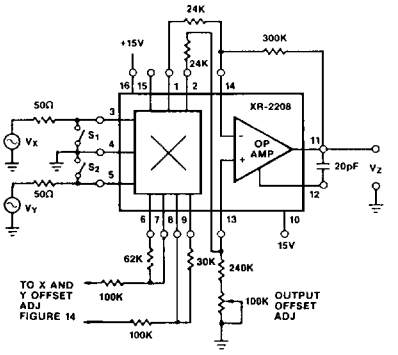


Figure 3. Test Circuit for Feedthrough Measurement X-Input Feedthrough = V_Z with S_1, open, S_2 closed. Y-Input Feedthrough = V_Z with S_1, closed, S_2 open.

DEFINITION OF MULTIPLIER TERMS

NONLINEARITY: Nonlinearity is the maximum deviation of the output voltage from a straight-line transfer function. It is measured separately for the X and Y inputs and is specified as (%) of full scale output.

FEEDTHROUGH: The amount of peak-to-peak output voltage present with one input grounded and a specified peak-to-peak input applied to the other input. Feedthrough is a function of multiplier offsets and can be minimized by offset adjustment (see Figure 13).

OFFSET VOLTAGES: A four-quadrant analog multiplier has three separate offsets: the X and Y input offsets and the output offset. The transfer function of a practical multiplier with scale factor K can be written as:

$$V_z = K[(Vx + \varnothing_x)\,(V_y + \varnothing_y)] + \varnothing_o$$

where $\varnothing_x$ and $\varnothing_y$ are the offset voltages associated with the respective inputs, $\varnothing_o$ is the offset voltage of the output, V_z is the multiplier output, V_x and V_y are the multiplier inputs. As shown in Figures 13 and 14, each of these offset voltages can be nulled to zero by external adjustments.

SCALE FACTOR, K: The constant of proportionality that relates the multiplier output to the X and Y inputs. If the offset terms are neglected, the multiplier output, V_z, is related to the X and Y inputs as $V_z = K(V_x \cdot V_y)$. The scale factor K has the dimensions of (volts) – 1 and can be adjusted externally.

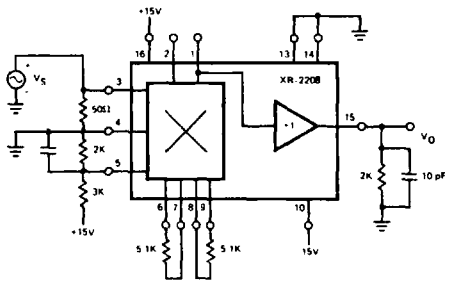


Figure 4. Test Circuit for Multiplier Small-Signal Bandwidth for X-Input (for Y-Input, reverse connections between Pin 3 and 5).

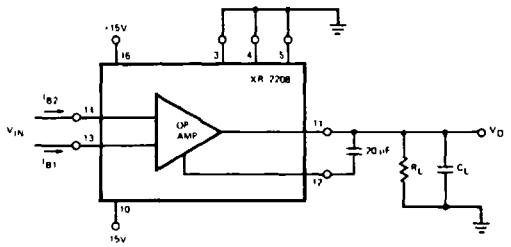


Figure 5. Test Circuit for Op Amp DC Parameters

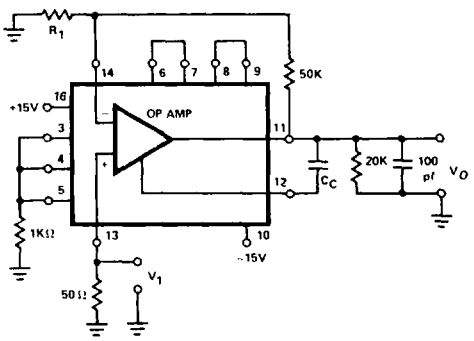


Figure 6. Op Amp AC Test Circuit

In most arithmetic applications the multiplier and op amp sections of the XR-2208 are interconnected as shown in Figure 14. In such applications, over-all scale factor K can be written as:

$$K = (K_m)(K_a) = \left(\frac{V_o}{V_x V_y}\right)\left(\frac{V_z}{V_o}\right)$$

where K_m is the gain constant of the multiplier section, and K_a is the gain of the op amp stage in Figure 14, V_o is the multiplier output across pins 1 and 2, and V_z is the op amp output at pin 11. With reference to Figure 14, these gain constants can be expressed as:

$$K_m \simeq \frac{25}{R_x R_y}\ (\text{volts})^{-1}; \qquad K_a \simeq \frac{R_f}{6 + R_i}$$

where all resistors are in kΩ.

Thus, overall scale factor K can be adjusted by varying R_x, R_y, R_f. For fine adjustment of the scale factor, K, an additional potentiometer can be included into the circuit, as shown in Figure 14.

INPUT DYNAMIC RANGE: The maximum peak signal which can be applied to the X or Y inputs for a given supply voltage without impairing linearity. (See Figure 10).

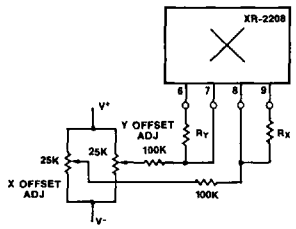


Figure 13. Offset Adjustment

MULTIPLIER BANDWIDTH: Depending on the particular application, a different definition of "multiplier bandwidth" may be used. The most commonly accepted definitions are:

a) *3-dB Bandwidth:* Frequency where the multiplier output is 3-dB below its low frequency (f = 20Hz) level.

b) *3° Phase Shift Bandwidth:* Frequency where the net phase shift across the multiplier is equal to 3°.

c) *1% Absolute Error Bandwidth:* Frequency where the phase vector error between the actual and ideal output vectors is equal to 1%. This frequency is reached when the net phase shift across the multiplier is equal to 0.01 radian or 0.57°.

d) *Transconductance Bandwidth:* Frequency where the transconductance of the multiplier drops 3-dB below its low frequency value. This bandwidth defines the frequency range of operation for phase-detector and synchronous AM detector applications.

TYPICAL CHARACTERISTIC CURVES

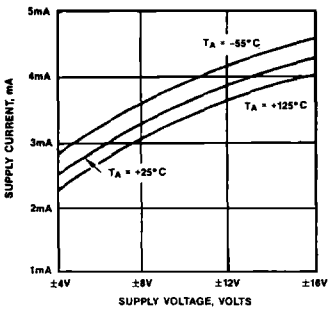


Figure 7. Supply Current vs Supply Voltage

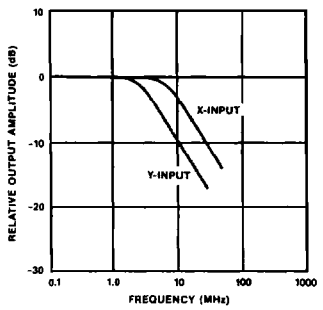


Figure 8. Small-Signal Frequency Response for the Multiplier Section. (Output Measured at Pin 15 — See Fig. 4).

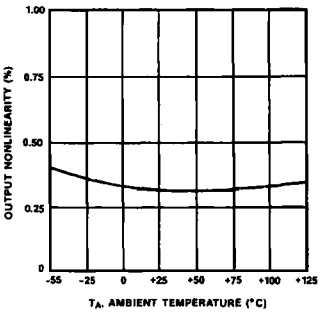


Figure 9. Temperature Dependence of Output Nonlinearity for X or Y Inputs (See Figure 2).

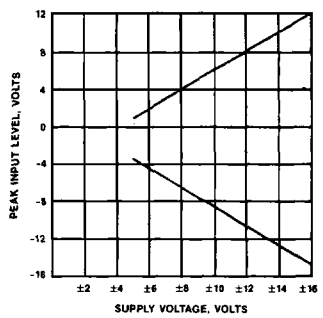


Figure 10. Multiplier Input Dynamic Range vs Power Supply

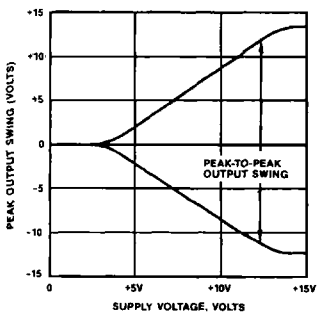


Figure 11. Op Amp Output Swing vs Power Supply

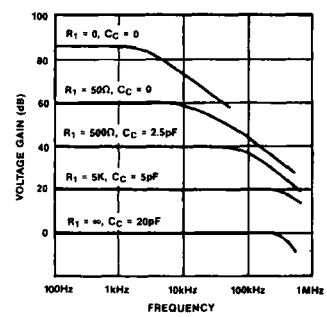


Figure 12. Op Amp Frequency Response

DESCRIPTION OF CIRCUIT CONTROLS

Multiplifer Inputs (Pins 3, 4, and 5)

The X and Y inputs to the multiplier are applied to pins 3 and 5 respectively. The third input (pin 4) is common to both X and Y portions of the multiplier, and in most applications serves as a "reference" or ground terminal. The typical bias current at the multiplier inputs is 3μA for the X- and Y-inputs and 6μA for the "common" terminal. In circuit applications such as "synchronous AM detection" or "frequency doubling" where the same input signal is applied to both X and Y inputs, pin 4 can be used as the input terminal since it is common to both X and Y sections of the multiplier.

Multiplier Outputs (Pins 1 and 2)

The differential output voltage, V_o, across these terminals is proportional to the linear product of voltages V_x and V_y applied to the inputs. V_o can be expressed as:

$$V_o \approx \left(\frac{25}{R_x R_y}\right)\left(V_x V_y\right)$$

where all voltages are in volts and the resistors are in kΩ. R_x and R_y are the gain control resistors for X and Y sections of the multiplier.

The common-mode dc potential at the multiplier outputs is approximately 3 volts below the positive supply. One of the multiplier outputs (pin 1) is internally connected to the unity-gain buffer amplifier input for high-frequency applications.

In most analog computation operations, such as multiplication, division, etc., pins 1 and 2 are dc coupled to the op amp inputs (pins 13 and 14). The final output, V_Z, is then obtained from the op amp output at pin 11, as shown in Figure 14.

X and Y Gain Adjust (Pins 6, 7, 8, 9)

The gains of the X and Y sections of the multiplier are inversely proportional to resistors R_x and R_y connected across the respective gain terminals. The multiplier conversion gain, K_m, can be expressed as:

$$K_m \simeq \frac{25}{R_x R_y} (\text{volts})^{-1}$$

where R_x and R_y are in kΩ.

X and Y Offset Adjust (Pins 7 and 8)

Two of the gain-control terminals, pins 7 and 8, are also used for adjusting X and Y offsets. Figure 13 shows the typical adjustment circuitry which can be connected to these pins to null-out input offsets.

OP AMP Inputs (Pins 13 and 14)

Pin 13 is the non-inverting and pin 14 the inverting input for the op amp section. In most multiplier applications, these terminals are connected to the multiplier outputs (pins 1 and 2). **Note: When the op amp section is not used, these terminals should be grounded.**

OP AMP Compensation (Pin 12)

The op amp section can be compensated for unconditional stability with a 20pF capacitor connected between pin 12 and pin 11. For op amp voltage gains greater than unity, this compensation capacitance can be reduced to improve slew rate and small signal bandwidth as shown in Figure 12.

OP AMP Output (Pin 11)

This terminal serves as the output for the op amp section. It is internally protected against accidental short circuit conditions, and can sink or source 10mA of current into a resistive load. In most multiplier applications, pin 11 is the actual XR-2208 output, with the op amp inputs being connected to the multiplier outputs.

Buffer Amplifier Output (Pin 15)

The buffer amp is internally connected to the multiplier section. The buffer amp has unity voltage gain, and provides a low-impedance output at pin 15 for the multiplier section. The buffer amp is particularly useful for high frequency operation since it minimizes the capacitive loading effects at the multiplier outputs.

The buffer amplifier is activated by connecting a load resistor, R_1, from pin 15 to ground. When it is not used, pin 15 can be left open circuited. However, since the buffer amplifier output is a low impedance point, reasonable care should be taken to avoid burnout due to accidental short circuits. The maximum dc current drawn from pin 15 should be limited to 10mA. The dc voltage at pin 15 is typically 4.5 volts below V+.

APPLICATIONS INFORMATION

PART I: ARITHMETIC OPERATIONS

Multiplication

For most multiplication applications, the multiplier and op amp sections are interconnected as shown in Figure 15 to provide a single-ended analog output with a wide dynamic range. The circuit of Figure 14 provides a linear output swing of 10V for maximum input signals of 10V, with a scale factor K = 0.1. The trimming procedure for the circuit is as follows:

1. Apply 0V to both inputs and adjust the output offset to 0V using the output offset control.
2. Apply 20Vp-p at 50Hz to the X-input and 0V to the Y-input. Trim the Y-offset adjust for minimum peak-to-peak output.
3. Apply 20Vp-p to the Y-input and 0V to the X-input. Trim X-offset adjust for minimum peak-to-peak out-put.
4. Repeat step 1.
5. Apply +10V to both inputs and adjust scale factor for V_o = +10V. This step may be repeated with different amplitudes and polarities of input voltages to optimize accuracy over the entire range of input voltages, or over any specific portion of input voltage range.

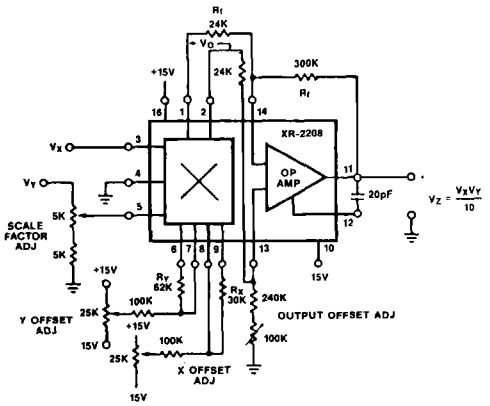


Figure 14. Multiplication Circuit

Squaring Circuit

The recommended circuit connection for squaring applications is shown in Figure 15. This circuit is the same as the basic multiplier circuit with both inputs tied together, except only one input offset adjustment is necessary. Trimming procedure for the squaring circuit is as follows:

1. Apply 0 volts to the input and adjust the output offset to zero.
2. Apply 1.0V to the input and adjust the Y-offset until $V_o = 0.10V$.
3. Apply 10V to the input and adjust the scale factor until $V_o = +10V$
4. Apply –10V to the input and check that $V_o = +10V$. If not, repeat steps 1 through 3. Some compromise may be necessary in scale factor adjustments given in

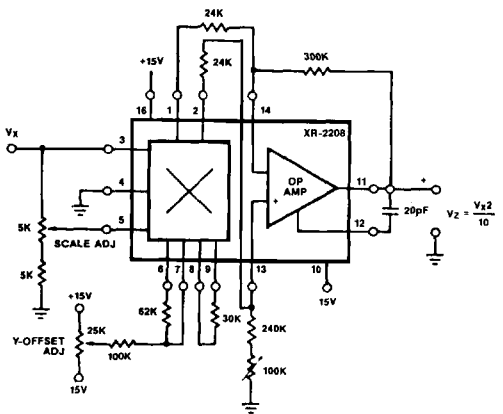


Figure 15. Squaring Circuit

Dividing Circuit

Recommended circuit connection for performing analog division is shown in Figure 16. This circuit uses the multiplier in the feedback path of the op amp. For the circuit shown, $V_o = +10\ V_z/V_x$ where $V_x < 0$ and V_z can have either sign. Positive values of V_x are not allowed, since this will reverse the polarity of the feedback loop, causing positive feedback and latchup.

This latchup mode is nondestructive to the XR-2208, and is common to all analog division circuits. The divide circuit is trimmed as follows:

1. Apply $V_z = 0$ and trim the output offset adjustment for constant output voltage as V_x is varied from –1V to –10V.
2. Keeping $V_z = 0$, and applying $V_x = -10V$, trim the Y-offset adjust until $V_o = 0$.
3. Let $V_z = V_x$ and/or $V_z = -V_x$ and trim the X-offset adjustment for constant output voltage as V_x is varied from –1V to –10V.
4. Repeat steps 1 and 2 if step 3 required a large initial adjustment.
5. Keeping $V_z = V_x$, adjust the scale factor trim for $V_o = -10V$ as V_x is varied from –1V to –10V.

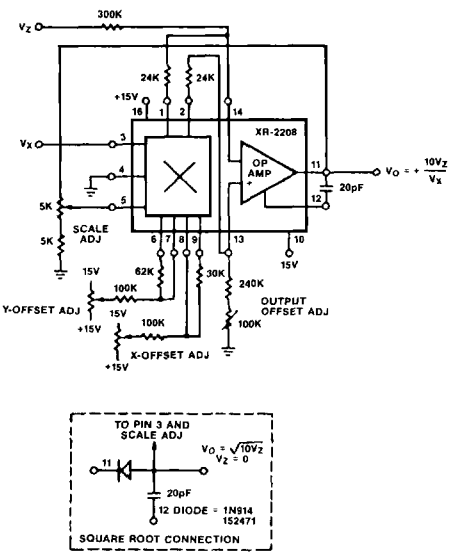


Figure 16. Dividing Circuit

Square Root Circuit

This is essentially the dividing circuit with the X input tied to the output. Thus, the voltage on the Z input is divided by the output voltage, i.e. the output is proportional to the square root of the input. A diode is included in series with the output to prevent a latchup condition which would result if V_Z were allowed to go negative. The square root circuit may be trimmed as a divider by disconnecting the X-input from the output, keeping $V_Z > 0$ and $V_X < 0$. The square root circuit may also be trimmed in the closed-loop mode by the following procedure:

1. Apply V_Z = +0.10V and trim the output offset adjust for V_O = –0.316V.
2. Apply V_Z = +0.9V and trim the X-offset adjust for V_O = –3.0V.
3. Apply V_Z = +10V and trim the scale factor adjust for V_O = –10V.
4. Repeat steps 1 through 3 until desired accuracy is achieved.

EQUIVALENT SCHEMATIC DIAGRAM

PART II: SIGNAL PROCESSING

AM Generation

Figure 17 is the recommended circuit connection for generating double side-band (DSB) or suppressed carrier AM signals. Modulation and carrier inputs are applied to the X and Y inputs respectively. The carrier level at the output can be adjusted by the dc voltage applied to pin 3. For suppressed carrier operation, the carrier feedthrough can be further reduced by using the X and Y offset adjustments. In this application, the unity-gain buffer amplifier section will provide a low impedance output if desired. If the buffer amp is not used, pin 15 should be open circuited to reduce power dissipation.
Typical carrier suppression without offset adjustment is 40 dB for frequencies up to 1MHz, and 30dB for frequencies up to 10MHz. For low frequency applications (f < 10kHz), carrier suppression can be reduced to 60dB by using the offset adjustment controls.

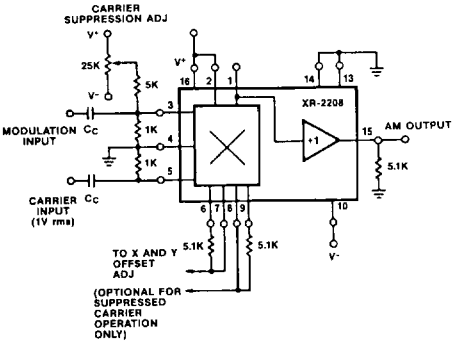


Figure 17. AM Generation

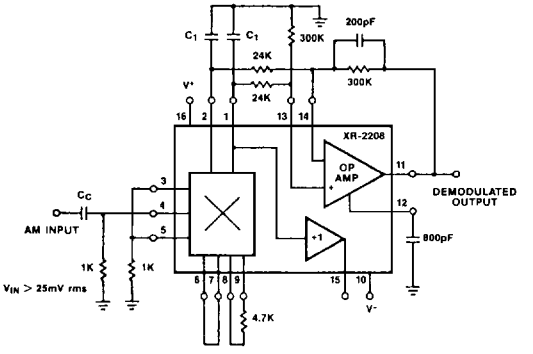


Figure 18. Synchronous AM Detector

Synchronous AM Detection

Figure 18 is a typical circuit connection for synchronous AM detection for carrier frequencies up to 100MHz. The AM input signal is applied to the multiplier "common" terminal (pin 4). The Y-gain terminals are shorted, and this section of the multiplier serves as a "limiter" for input signals ≥ 50mVrms; the X-section of the multiplier operates in its linear mode. The low-pass filter capacitors, C_1, at pins 1 and 2 are used to filter the carrier feedthrough. If desired, the op amp section can be used as an audio preamplifier to increase the demodulated output amplitude.

Triangle-to-Sinewave Conversion

A triangular input can be converted into a low distortion (THD < 1%) sinusoidal output with the XR-2208. A recommended connection for this application is shown in Figure 19. The triangle input signal is applied to the X-input (pin 3). The multiplier section rounds off the peaks of this input and converts it to a low distortion sine wave. For the component values shown in Figure 19, the recommended input signal level at pin 3 is ≃ 300mV pp in order to obtain a 2V pp sine wave output at pin 15. This waveform can be further amplified using the op amp section to provide high level (10V pp), low distortion output at pin 11.

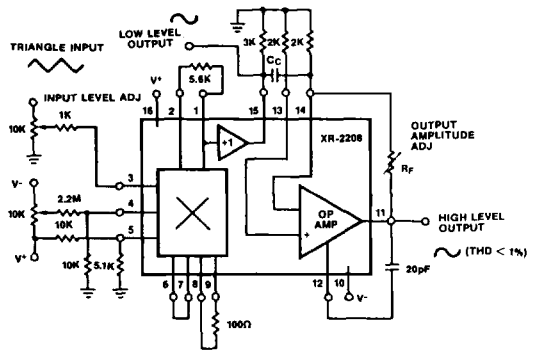


Figure 19. Triangle-to-Sine Converter

Phase Detection

The multiplier section can be used as a phase detector. A recommended circuit connection is shown in Figure 20. The reference input is applied to pin 5, and the input signal whose phase is to be detected is applied to pin 3. The differential dc voltage, $V_ø$, at the multiplier outputs (pins 1 and 2) is related to the phase difference, ø, between the two input signals, V_1 and V_2, as:

$$V_ø = K_d \cos ø$$

where K_d is the phase detector conversion gain. For input signals ≥ 50mV rms, K_d is ≈ 2V/radian and is independent of signal amplitude. For lower input amplitudes, K_d decreases linearly with the decreasing input level. The capacitors C_1 at pins 1 and 2 provide a low-pass filter with a time constant $T_1 = R_1C_1$, where R_1 = 6kΩ is the internal impedance level at these pins.

If needed, the phase conversion gain can be increased by using the op amp section of the XR-2208 to further amplify the output voltage, $V_ø$. The XR-2208 is suitable for phase detection for input frequencies up to 100MHz. Pins 1 and 2 are normally tied to an operational amplifier placed in a difference amplifier configuration.

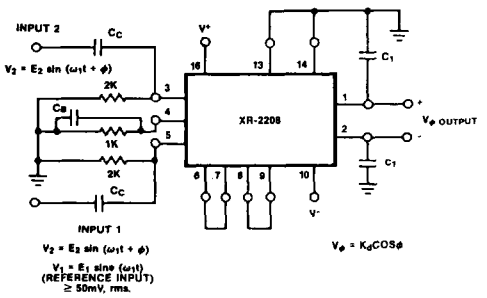


Figure 20. Phase-Detector Circuit

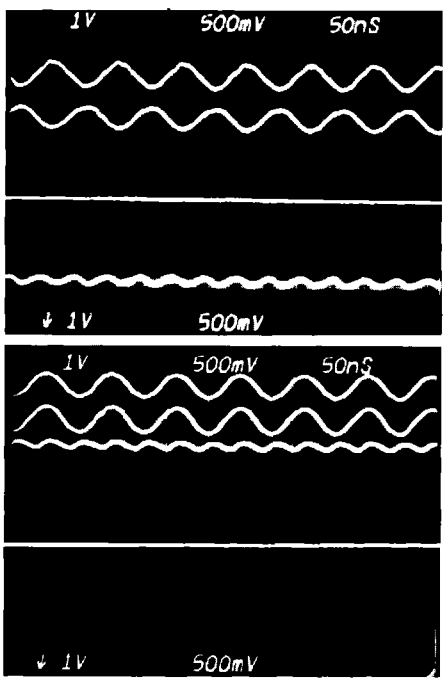


Figure 21. Shows the summed output of the phase detector circuit with pin 1 applied to the inverting input of oscilloscope; pin 2 applied to the noninverting input of oscilloscope.

C_1 = 12pF, f_{INPUT} = 12MHz, ø = 180°, V_0 = -2.5 V_{DC}, (a) ø = 0°, (b) V_0 = +2.5 V_{DC}.

Motor Speed Control

A motor speed control where the frequency of the motor is "phase-locked" to the input reference frequency, f_r, is shown in Figure 22. The multiplier section of the XR-2208 is used as a phase-comparator, comparing the phase of the tachometer output signal with the phase of the reference input. The resulting error voltage across pins 1 and 2 is low-pass filtered by capacitors C_1 and amplified by the op amp section. This error signal is then applied to the motor field-winding to phase-lock the motor speed to the input reference frequency.

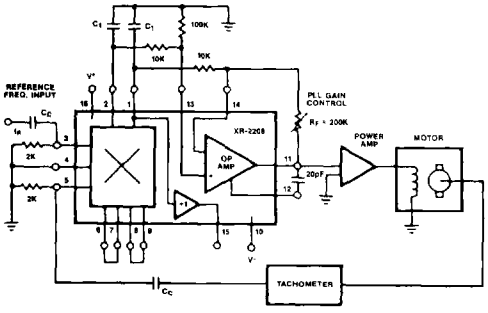


Figure 22. Motor Speed Control Circuit

Precision PLL

A precision phase-locked loop may be constructed using an XR-2207 voltage controlled oscillator and an XR-2208. (See Figure 23.) Due to the excellent temperature stability and wide sweep range of the XR-2207 this PLL circuit exhibits especially good stability of center frequency and wide lock range. In this application the XR-2208 serves as a phase comparator and level shifter. Resistor R_L adjusts the loop gain of the PLL, thus varying the lock range. Tracking range may be varied from about 1.5:1 up to 12:1. For large values of R_L, temperature stability of center frequency is better than 30ppm/°C.

Phase-Locked AM and Carrier Detection

The XR-2208 can be used as a "quadrature detector" in conjunction with monolithic PLL circuits to perform phase-locked AM demodulation and for carrier-level detection. Figure 24 shows a recommended circuit connection for such applications. The XR-210 or XR-215 monolithic PLL circuits can be adjusted to lock on the desired input AM signal and re-generate the unmodulated carrier. This carrier frequency appears across the timing capacitor, C_o, of the PLL and is used as the "reference input" to the XR-2208 multiplier. The AM signal is applied simultaneously to the PLL input and to the XR-2208 multiplier input (pin 3), as shown in Figure 24.

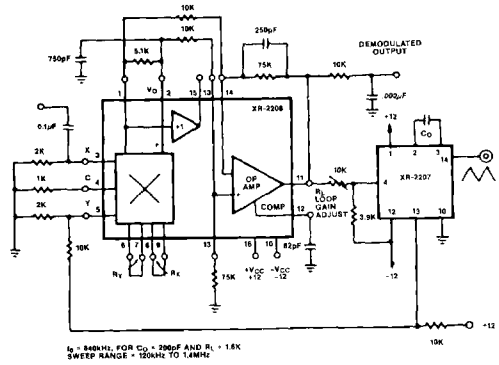


Figure 23. Precision PLL

The demodulated signal is then low-pass filtered by capacitor C_1 at the multiplier output, and can be amplified further to the desired audio level by using the op amp section of the XR-2208.

In the carrier detector applications, the op amp is used as a voltage comparator and produces a "high" or "low" level logic signal at the op amp output when the input carrier level reaches a detection threshold level set by an external potentiometer. The output from the carrier detector can then be used to enable the "logic-output" stage of the XR-210 FSK modem.

The phase-locked AM or carrier detector system of Figure 23 shows a high degree of frequency selectivity, as determined by the monolithic PLL "capture" band-width.

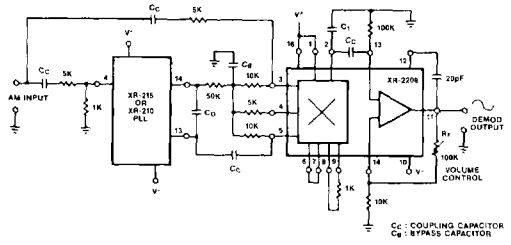


Figure 24. Phase-Locked AM Demodulation or Carrier Detection