Analog Multiplier

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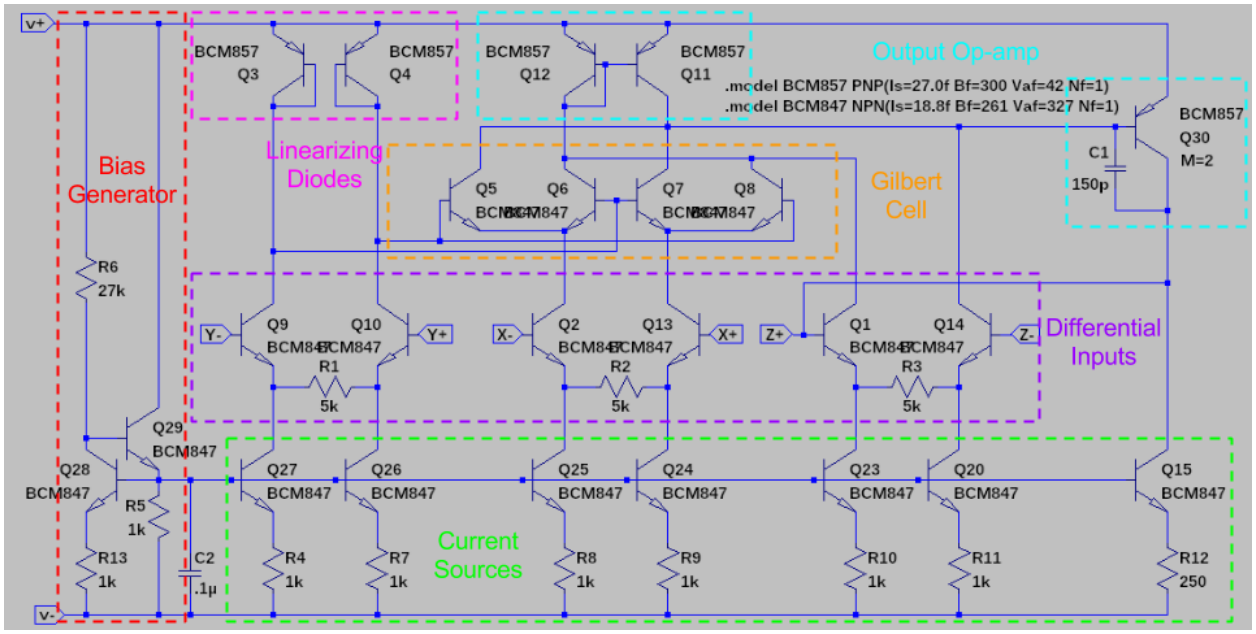
Summary

The goal of this project was to build an analog multiplication unit entirely out of matched transistor pairs, one that would be suitable for analog computation purposes. The primary specification to evaluate the multiplier was it's linearity and accuracy. After successfully building the gilbert cell multiplier core, which had several performance issues, we enhanced the basic multiplier core using various circuit techniques to arrive at the final design. Despite some setbacks, we ultimately succeeded in building a complete, functioning multiplier with a controllable transfer function of the form $Z = \frac{XY}{\alpha}$, where alpha is a constant represented in volts that can be arbitrarily chosen via the selection of one or more resistor values and bias currents. We did not, however, have enough time to design a PCB for the final project.

Circuit Design

Shown below is the schematic which depicts the final design for the analog multiplier. Each functional section of the multiplier has been outlined in different color, to facilitate clarity.



The first section, the bias generator highlighted in red, generates a reference voltage that is used to bias all of the current sources in the circuit, shown in green. It was assumed that this circuit would always be powered from a bipolar ±15V supply, so R6 was chosen so that about 1mA of current would flow through R13, thus producing 1V across it. This produces three important effects: First, the current produced by the current sources can be easily selected by selecting an

appropriate emitter resistor. Second, the current sources are protected against thermal runaway, which resulted in the destruction of two transistor pairs in an earlier version of the circuit which omitted the emitter resistors. And third, the output impedance of the sources are greatly increased, which has a beneficial effect on the linearity and common mode rejection of the multiplier.

The next section, the differential inputs, which are highlighted in purple, serve to linearly convert the input voltages into differential currents with a specific transconductance, selected by resistors R1, R2 and R3. As shown, this gives the circuit a linear differential input voltage range of about 5V, which is a great improvement over the input voltage range allowed by a simple differential pair, which is only on the order of 20-40mV. While the X, Y, and Z inputs are all identical, the Z "input" is not actually an input, as such. Instead, it is used inside the feedback loop of the output op-amp so that the output voltage is produced in the inverse way that the input currents are produced from the input voltages.

The next section, shown in orange, is the Gilbert cell, which is the heart of the analog multiplier. This is where the multiplication is performed, and the output of the cell is a differential current corresponding to the multiplication of the input currents. While the currents from the X input can be sent directly into the Gilbert cell, the Y input currents must first be "pre-distorted" by the linearization diodes Q3 and Q4, shown in magenta. This is done so that the Y input responds linearly to input voltage, in the same fashion as the X input. Each of the two currents from the X input are differentially scaled by a differential pair driven by the Y input linearizing diodes. Then the four currents are summed to produce a differential output current.

The final part of the analog multiplier is the output op-amp, which has been highlighted in cyan. Absent from this op-amp structure is the differential input pair, since the Gilbert already produces a differential output current. Instead, all that is required is a current mirror, formed by Q11 and Q12 and a gain transistor, Q30. Actually, Q30 comprises of two transistors, as indicated by the 2x multiplier shown in the schematic and is biased by four times the normal current. This was done so that the current density and the Vbe of Q11, Q12 and Q30 would match. In simulations this helped to improve output DC offset, but practically this discrete circuit suffers from enough significant thermal fluctuations and mismatch in the PNP current mirror Q11, Q12 to make this improvement insignificant. The output of the circuit feeds one of the inputs to the Z input of the multiplier, while the other Z input is grounded. Thus, the Z input produces a third differential feedback current and this feedback loop acts to keep the currents into each transistor of the PNP mirror balanced. Also present in the op-amp section of the multiplier is a frequency compensation capacitor C1, which was required to keep the feedback loop from oscillating.

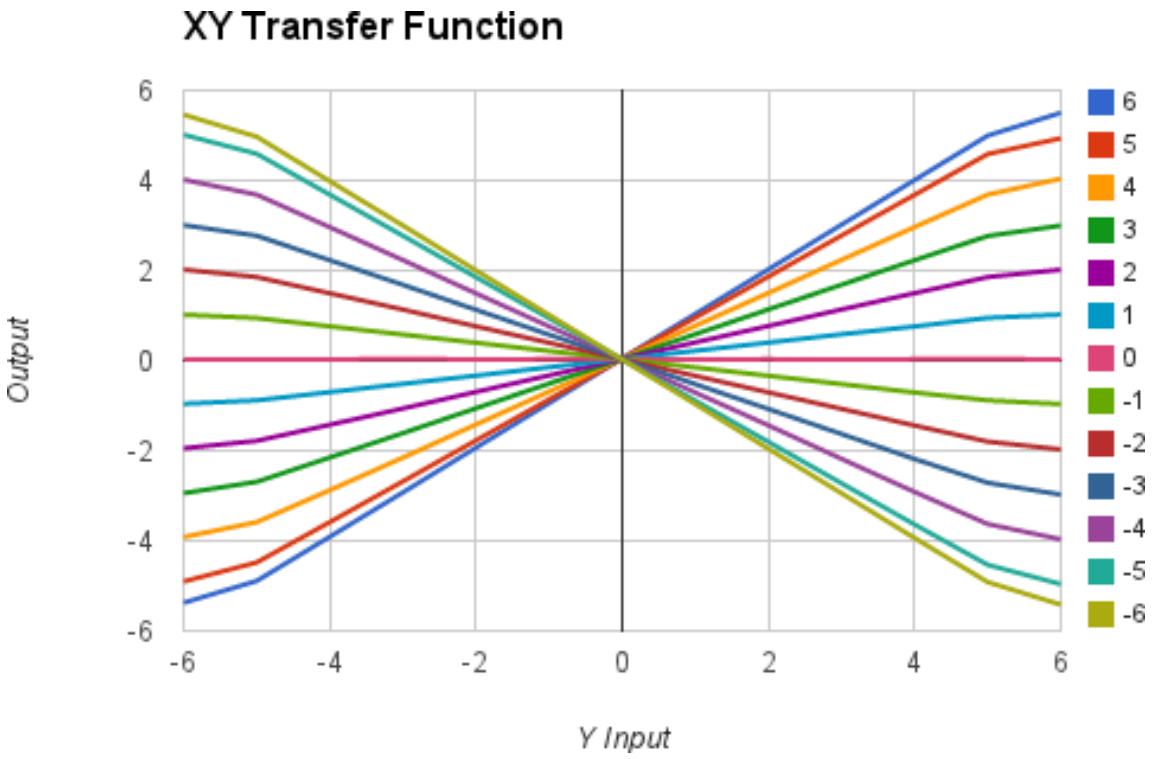
Theoretical Analysis

At the end of the day, this multiplier is highly linear with an accurately controllable transfer function. Theoretically, the circuit can be analysed to derive its transfer function. It turns out that it takes the following form: $V_{out} = \frac{V_x V_y R_Z}{R_x R_y I_y}$. Somewhat curiously, the bias current for the Y input appears in the transfer function, but this is due to that fact that the effective multiplication factor

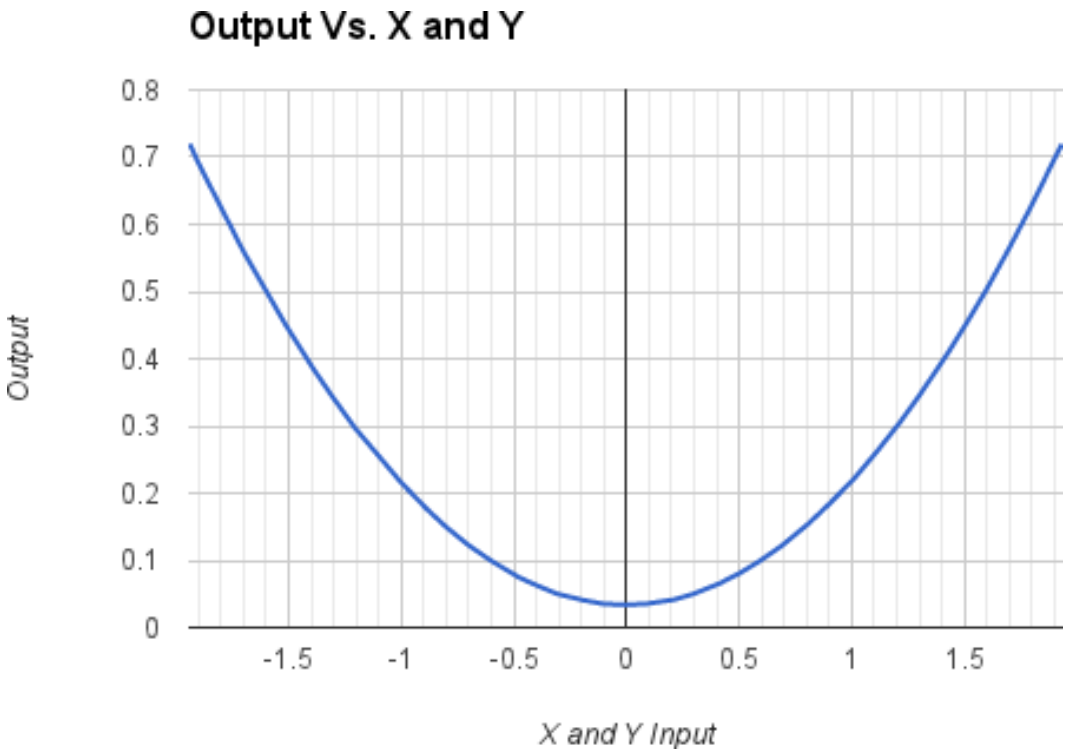
of the Y input is determined by the ratio of the differential Y input current with respect to its DC component, I_y, which is not true of the X or Z inputs. At any rate, as the circuit is currently designed, the overall transfer function is equal to the multiplication of the input voltages divided by a 5V constant. Also, we can easily theoretically calculate the maximum linear differential input voltage for each of the three inputs, which occurs when one of the input transistors becomes starved of current, and this expression is simply $V_{in,max} = I_{DC}R_{diff}$. Thus, for the shown component values this turns out to be 5V for any of the three inputs.

Measurement Results

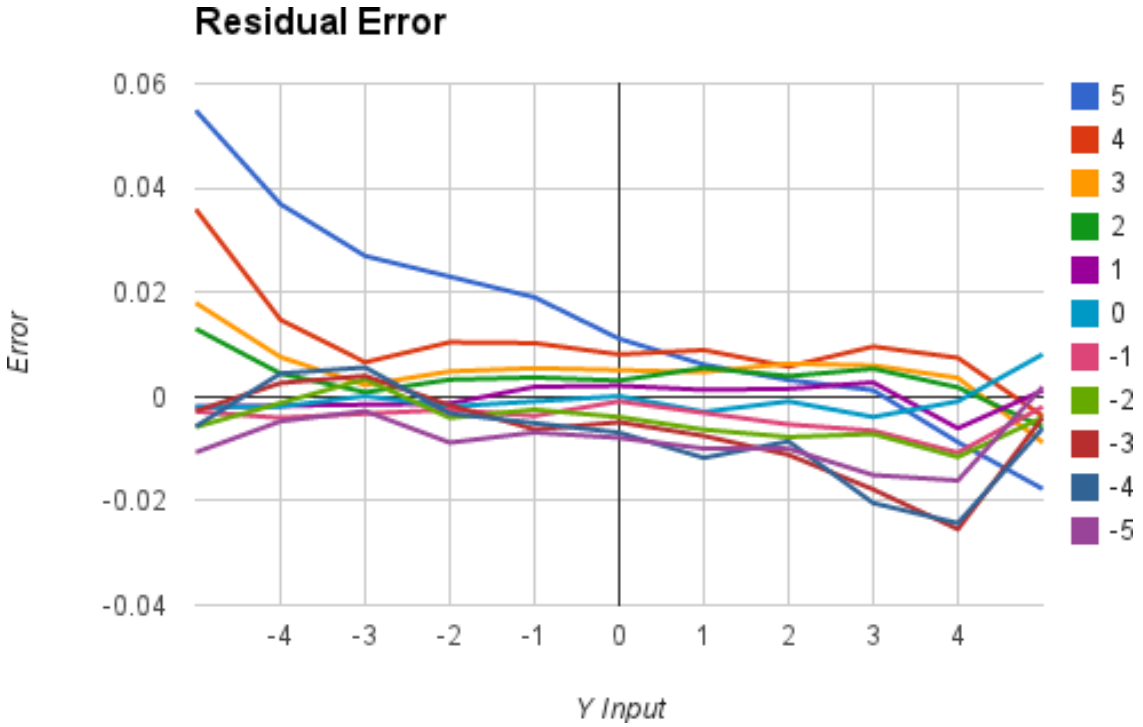
The first and primary measurement to be made of this multiplier is to record it's transfer function, which should match the one derived in the previous section. Shown below is a graph of the resulting measurement, which was taken from -6V to +6V for each input, at 1V steps. It clearly shows that the multiplier is very linear, up until an input voltage past 5V.



To evaluate the nonlinearity of the transfer function, a second transfer function was obtained by connecting both the X and Y inputs together so that the multiplier would produce a squaring function. Here, measurements were taken from -1.9 to +1.9V at roughly 100mV steps.



From this, linear regression analysis was used to find the squared and constant coefficient of the transfer function. It turns out that the multiplier has an alpha coefficient of 5.47V, instead of the predicted 5V, and a hefty DC offset of 34mV. By calculating a corresponding theoretical set of data using the measured transfer function coefficient, including the DC term, and subtracting to find the difference, the graph of residual error shown below was obtained.



Here, there is a large amount of noise due to measurement error, but if you look very closely, a very slight linear trend can be seen in the data. This would be caused by variations in the output of the current sources due to changes in the input voltage. However, this linear coefficient is very small, and is only on the order of 1-2mV/V.

Conclusion

This project aimed to design and build a linear analog multiplier using nothing but matched transistor pairs. We achieved this by first building and testing a simple gilbert cell multiplier, which had severe issues with input voltage range and non-linearity. We addressed these issues by adding extra circuit blocks, including degeneration resistors, current sources, linearizing diodes, and an integrated op-amp with symmetric feedback. The updated design resolved these problems, but suffered from a few unforeseen issues, like thermal runaway with the current sources. Once addressed, the final design proved to meet the linearity requirement that was critical to its performance. Despite a few flaws, such as significant DC offset