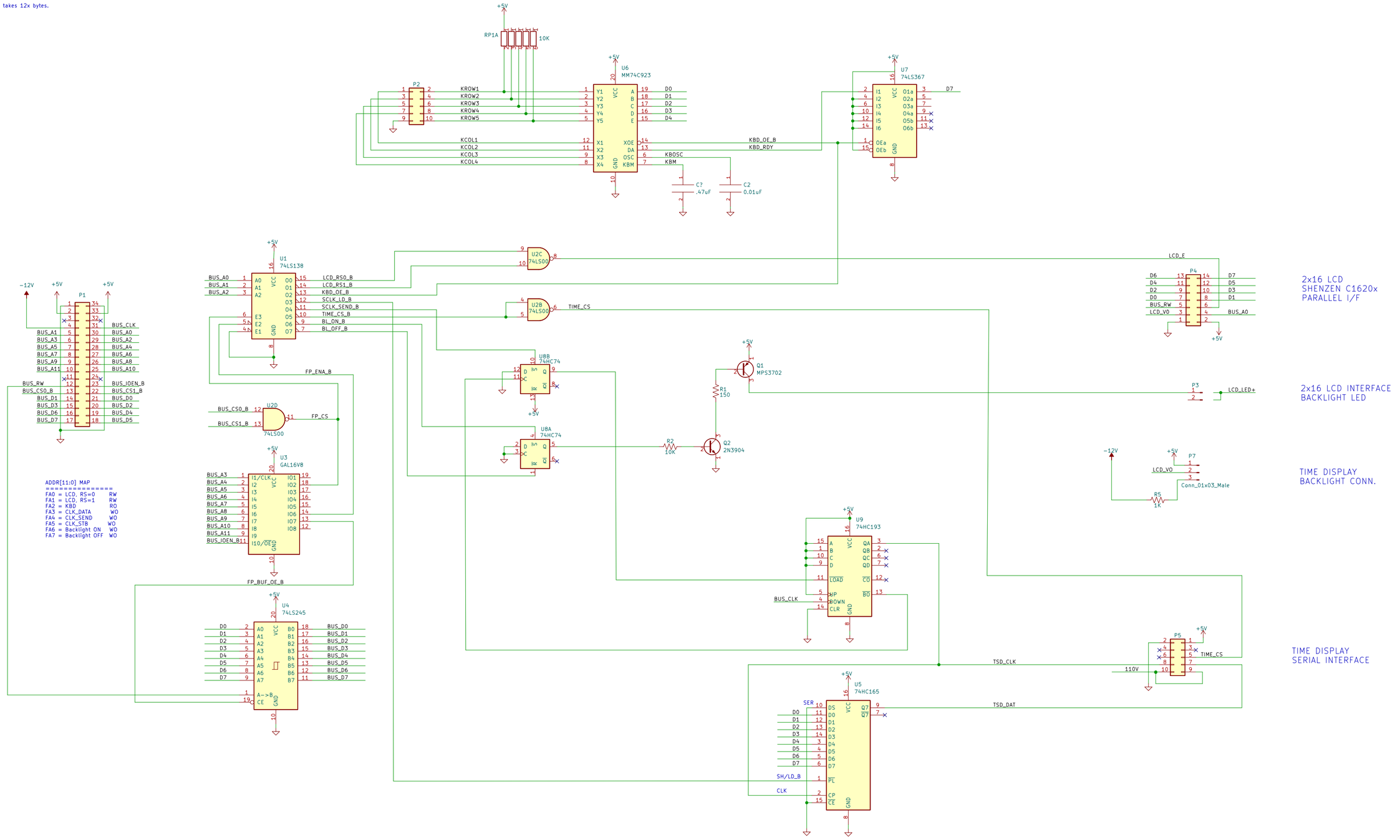
NOTES
* Pin 23 could be A12, but given the gap between it and the others it seems more like an IO enable.
* Addr order is inferred from PAL and U1. MSBs could be out of order.
* BUSCLK drives an HC165 directly, so FMAX <= 43 MHz – perhaps 33 MHz. Any clock >= 1 MHz will be fast enough to redraw clock display.
* Writing to 0xFA3 loads the SR with data.
* Writing to 0xFA4 causes the generation of 8 clock pulses, clocking out the S/R MSB first.
* Writing to 0xFA5 causes the previous data to be loaded in.
* The time display takes 12x bytes.



Gary Milliorn
Sheet: /
File: XLDC_front_panel.kicad_sch
Title: TrueTime XL–DC Display Front Panel
Size: C | Date: 2022_0520 | Rev:
KiCad E.D.A. eeschema (6.0.4) | Id: 1/1