Memory Maps

Since the memory map is not fully decoded, unused addresses may actually map into real memory somewhere. Unfilled address space may cause a bus error when accessed or it may overlay some other address space.

Table 1–7: 68020 Memory Map

Base Address	Chip Select	Description	Port Size
0000 0000–00FF FFFF	~KERNEL	Kernel address space, see "Kernel Addr Decode"	Byte
0100 0000–01FF FFFF	~SYSROM	System ROM address space. The firmface buffer enable bit in the Bus Control Register must be set. The number of wait states for system ROM must be set in Miscellaneous Register inside U2000.	Long
0200 0000–02FF FFFF	~OPTION1CS	Reserved for options	B,W,L
0300 0000–03FF FFFF	~OPTION2CS	Reserved for options	B,W,L
0400 0000–040F FFFF	~NVRAM	Non-volatile memory for calibration constants, front panel setups, waveform storage, and 2 kilobytes of hardware write protected calibration constants.	Byte
0500 0000–051F FFFF	~DRAM	System dynamic RAM	Long
0600 0000–06FF FFFF	~FLOPPY	Floppy chip select	B
0700 0000–07FF FFFF	~TRISTAR	DSP (U1097) space	Word only
0800 0000–08FF FFFF	~DISPLAY	Display address space	Word
0900 0000–09FF FFFF	~SYSMMIO	System memory mapped I/O	Byte
0900 0000	~IMSKREG	Interrupt Mask Register	Byte
0920 0000	~MISCREG	Miscellaneous Register	Byte
0940 0000	~INTREG1	Interrupt Read Register 1 (R)	Byte
0960 0000	~INTREG2	Interrupt Read Register 2 (R)	Byte
0980 0000	~CLRTIMER	Clear Timer (6.5 ms timer) (R)	Byte
09A0 0000	~RDFIFO	Read FIFO (R)	Byte
09C0 0002	~Shutdown		
09E0 0000	~SCOPELOOP	Scope Trigger (R)	Byte
0A00 0000–0AFF FFFF	~XPANDRAM	Reserved for development	Long
0B00 0000–0BFF FFFF	~SYSROMII	Second ROM address space	——
0C00 0000–0CFF FFFF	Unused		——
0D00 0000–0DFF FFFF	~DUARTCS	Dual parallel-to-serial interface to the Front Panel and Acquisition Processors	Byte
0E00 0000–0EFF FFFF	~IOCS	Chip select for I/O option bus	Byte
0F00 0000–0FFF FFFF	Reserved	Reserved for test fixture. An interrupt acknowledge cycle generates a low strobe at this location.	——

Table 1–8: Kernel Memory Map (0000 0000 to 00FF FFFF) All 8 Bits Wide

Start Addr	Size	Description
0000 0000	256 K by 8	Boot ROM
0020 0000	32 K by 8	Kernel RAM
0040 0000	Single Register R/W	Bus Control Register
0060 0000	Single Register W only	7 Segment LED
0080 0000	Single Register R only	Configuration Dip Switch
00A0 0000	Depends on Console	Console
00C0 0000	8 R, 8 W Registers	GPIB IC
00E0 0000	Register (read only)	ID Register 1
00E0 0001	Register (read only)	ID Register 2

Table 1–9: Bus Control Register (0040 0000 R/W)

680020 Data Bit	Signal Name	Description
D31	PWRDWN	System power down, asserting this bit resets the Processor System
D30	ENABLEBUS	Enable buffers to rest of system outside Kernel
D29	FFBUFEN	Enable buffers to get to system ROM
D28	-	Unused
D27	~ENABLESP	Enable SP bus to the Display and DUART
D26	ENABLEINT	Enable all interrupts outside the Kernel (These interrupts still have their respective mask bits)
D25	MSKGPIB	Masks the GPIB interrupt
D24	MSKCONSOLE	Masks the console interrupt

Table 1–10: 7 Segment LED (0060 0000 Write Only)

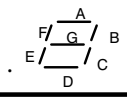
680020 Data Bit	Signal Name	Description 
D31	~DEC POINT	7 Segment LED decimal point
D30	~SEGMENT G	7 Segment LED segment G
D29	~SEGMENT F	7 Segment LED segment F
D28	~SEGMENT E	7 Segment LED segment E
D27	~SEGMENT D	7 Segment LED segment D
D26	~SEGMENT C	7 Segment LED segment C
D25	~SEGMENT B	7 Segment LED segment B
D24	~SEGMENT A	7 Segment LED segment A

Table 1–11: DSP Interrupt Mask Register

DSP Data Bit	680020 Data Bit	Signal Name	Description
D15	D31	M020INTTS	Masks the 68020 interrupt to DSP
D14	D30	MPTAVAIL	Masks the point-available interrupt from the acquisition system
D13	D29	MACQDN	Masks the done interrupt from the acquisition system
D12	D28	MDISPINTTS	Masks the display system's interrupt
D11	D27	MACQINTTS	Unused
D10	D26	M0.4MSINT	Masks the 0.4 ms periodic interrupt
D9	D25	MVERTINT	Masks the display system's vertical-blanking interrupt
D8	D24	MTSOPINT	Masks an option interrupt

Table 1–12: DSP Interrupt Read Register

DSP Data Bit	680020 Data Bit	Signal Name	Description
D15	D31	~020INTTS	Asserted when a 68020 interrupt to DSP is pending
D14	D30	~PTAVAIL	Asserted when a point-available interrupt is pending
D13	D29	~ACQDN	Asserted when an acquisition-done interrupt is pending
D12	D28	~DISPINTTS	Asserted when a display interrupt is pending
D11	D27	Unused	Unused
D10	D26	~0.4MSINT	Asserted when a 0.4 ms interrupt is pending
D9	D25	~VERTINT	Asserted when synchronizing the waveform planes with vertical blanking
D8	D24	~TSOPTINT	Asserted when a D2 bus option interrupt is pending

Table 1–13: DSP Memory Map

DSP D1 Address	68020 Address	Description
00000–07FFF 00000–1FFFF	0720 0000–0720 FFFF 0720 0000–0727 FFFF	D1 Memory 32K by 16 256K by 16
60000–7FFFF	072C 0000–072E 00XX	D1 Memory Mapped I/O (on the A10 Acquisition board)
601XX	072C 02XX	SETHW
602XX	072C 04XX	Unused
604XX	072C 08XX	LSTL, HSTL
608XX	072C 10XX	ACQP
610XX	072C 20XX	DSP/DMUX CH1
620XX	072C 40XX	DSP/DMUX CH2
640XX	072C 80XX	DSP/DMUX CH3
680XX	072D 00XX	DSP/DMUX CH4
700XX	072E 00XX	Unused
80000–FFFFF	0730 0000–073F FFFF	Acquisition Memory (on the A10 Acquisition board)
DSP D2 Address	**68020 Address**	**Description**
00000–17FFF 00000–5FFFF	0740 0000–0747 FFFF 0740 0000–075B FFFF	D2 Memory 256K by 16 896K by 16
F0000–F3800	075E 0000–075E 7FFF	D2MMIO
F0000	075E 0000	DSP Interrupt Mask Register
F0800	075E 1000	DSP Interrupt Read Register
F1800	075E 3000	D2 Miscellaneous Register
F2000	075E 4000	Clear DSP Periodic Interrupt
F7000	075E E000	Write FIFO Data
80000–FFFFF	075C 0000–075F FFFF	Display
DSP Instruction Memory Address	**68020 Address**	**Description**
00000–0FFFF	0700 0000–0701 FFFF	DSP Instruction Memory

Table 1–14: D2MMIO Miscellaneous Register

DSP Data Bit	680020 Data Bit	Signal Name	Description
D15	D31	~TSINT020	Asserted when DSP wants to interrupt the 68020
D14	D30	Unused	
D13	D29	Unused	
D12	D28	Unused	
D11	D27	WFMSAVE (read only)	
D10	D26	Unused	
D9	D25	~FIFOFULL	Asserted when the FIFO is full. In this condition further writes to the FIFO result in lost data.
D8	D24	TMSKFIFOINT	Masks the interrupt from the FIFO to the 68020

Table 1–15: 68020 to DSP Instruction Memory Accesses

68020 Address	D31 – D24	D23 – D16
0700 0000	TSID23–TSID16	TSID15–TSID8
0700 0002	TSID7–TSID0	
0700 0004	TSID23–TSID16	TSID15–TSID8
0700 0006	TSID7–TSID0	
0700 0008	TSID23–TSID16	TSID15–TSID8
0700 000A	TSID7–TSID0	

Since the memory map is not fully decoded, unused addresses may map into real memory somewhere. Accessing unfilled address space can cause a bus error or over-write decoded address space.

Table 1–16: Display Memory Map

68020 Address	Description	Port Size
	PIXEL PROCESSOR	
075C0 000	Y Register	word
075C0 002	X Register	word
075F0 000 – 075F0 1FF	ALU Table	word
075F4 000 – 075F401F	Decay Table	word
075F8 000	Control Register 1	word
075F 8002	Intensity Register	word
075F 8004	Top Register	word
075F 8006	Bottom Register	word
075F 8008	Data Register	word
	RASTERIZER	
075E 8000	Register 1	word
075E 8002	Register 2	word
075E 8004	Mode Register	word
075E 8006	Window Register 1	word
075E 8008	Window Register 2	word
075E 800A	Line Count Register	word
075E 800C	Diagnostic Register	word
075E 800E	Start Line Saturated Pixel Count Register	word
075E 8010	End Line Saturated Pixel Count Register	word
075E 8012	Saturated Pixel Count Register	word
075E 8100 – 075E 811F	Bright Table	word
075E 8200 – 075E 83FF	Sum Table	word
	VECTOR LIST MEMORIES	
075E 9000 – 075E 9FFF	Vector List Memory 0	word
075E A000 – 075E AFFF	Vector List Memory 1	word
	MISCELLANEOUS	
075E C800 – 075E C80E	VGA RAMDAC	word
075E D000 – 075E D01E	LCS RAMDAC	word
075E D800 – 075E D383	LCS Controller	word
075E E000	FIFO write	

Table 1–16: Display Memory Map (Cont.)

68020 Address	Description	Port Size
075E B000	Display Control Register	word
0807 0018	VSC Base Address	word
0800 0000 – 0801 FFFF	Waveform Plane	word
0802 0000 – 0805 FFFF	Text Plane	byte
0806 0000 – 0806 FFFF	BIT – BLT plane	
0807 0000 – 0807 0010	BIT – BLT register	

Table 1–17: BDSACK Combinations For 68020 Memory Space

68020 Address	Memory Space Description	Bdsack
0000 0000–00FF FFFF	Kernel	~Bdsack0
0100 0000–01FF FFFF	System ROM	~Bdsack0 & ~Bdsack1
0400 0000–04FF FFFF	NVRAM	~Bdsack0
0500 0000–050F FFFF	System dynamic RAM	~Bdsack0 & ~Bdsack1
0600 0000–06FF FFFF	Floppy	~Bdsack0
0700 0000–07FF FFFF	DSP space	~Bdsack1
0800 0000–08FF FFFF	Display address space	~Bdsack0 or ~Bdsack1
0900 0000–09FF FFFF (except for 09C0 0000–09DF FFFF)	System memory mapped I/O	~Bdsack0
0D00 0000–0DFF FFFF	Dual parallel-to-serial interface to the Front Panel and Acquisition Processors	~Bdsack0

Table 1–18: A11 DRAM Processor/Display Wait State Generation

Name	a27	a26	a25	a24	# of wait states	size	enablebus
KERNEL	0	0	0	0	3	byte	no
SYS ROM	0	0	0	1	var	long	yes
OPTION1	0	0	1	0	n/a	n/a	n/a
OPTION2	0	0	1	1	n/a	n/a	n/a
NVRAM	0	1	0	0	1	byte	yes
SYSRAM	0	1	0	1	0 or 1	n/a	n/a
FLOPPY	0	1	1	0	9	byte	yes
DSP	0	1	1	1	n/a	word	yes
DISPLAY	1	0	0	0	n/a	word/byte	yes
SYSMMIO	1	0	0	1	0	byte	yes
XPANDRAM	1	0	1	0	n/a	n/a	n/a
SYS ROM II	1	0	1	1	VAR	LONG	YES SPARE
NA1	1	1	0	0	n/a	n/a	n/a
DUART	1	1	0	1	3	BYTE	YES
IOCUS	1	1	1	0	n/a	n/a	n/a
NA2	1	1	1	1	n/a	n/a	n/a

n/a = not applicable

var = depends on sysromwts0–1 (00 – 0 wait states, 01 – 1, 10 – 2, 11 – 3)

Table 1–19: A11 DRAM Processor/Display DUART Interface Signals

Signal	Serial Port	U1317 Pin	Definition
FPPRXD	Front Panel Processor	33	Received Data (transmitted by the 68020, received by the Front Panel Processor)
FPPTXD	Front Panel Processor	35	Transmit Data (by the Front Panel Processor)
ACQRXD	Acquisition Processor	13	Received Data (by the Acquisition Processor)
ACQTXD	Acquisition Processor	11	Transmit Data (by the Acquisition Processor)
FPPRXRDY	Front Panel Processor	8	Receive Ready (Front Panel Processor is ready to receive data)
ACQRXRDY	Acquisition Processor	5	Receive Ready
FPPTXRDY	Front Panel Processor	30	Transmit Ready (DUART is ready to receive from the Front Panel Processor)
ACQTXRDY	Acquisition Processor	16	Transmit Ready
TP49		15	Timer Frequency square wave
TP50		31	Receiver Clock

Table 1–20: A10 Acquisition Demultiplexer DB Memory Map

Address	R/W	Initialized	Use
0	R/W	Zero at power-up	Acquisition Memory DB addressing control
1	R/W	Zero at power-up	Acquisition done and point available control
2	R/W	—	Data for programmable inverter
3	R/W	—	Data for clip detector inverter
4	R/W	—	Trigger control
5	R/W	—	Pre-trigger count
6	R/W	—	Post-trigger count
7	R/W	—	Start value for address counter
8	R/W	—	Stop value for address counter
9	R/W	—	Decimator control
A	R/W	—	Decimator divider count
B	R/W	—	Hi-res decimator shift count
C	R	—	Roll data register
D	R	—	Status register 1
E	R	—	Status register 2
F	R	—	Value of address counter at acquisition done
10	R	—	Value of address counter at trigger
11	R	—	Value of trigger time (least significant word) at trigger
12	R	—	Value of trigger time (middle word) at trigger
13	R	—	Value of trigger time (most significant word) at trigger
14	R	—	Value of trigger synchronizer counter at trigger
15	R	—	Current pre-trigger count
16	R	—	Current post-trigger count
17	R/W	Zero at power-up	Input control / diagnostic counter
18	R/W	—	Hi-res decimator 20-bit incrementer and diagnostic control register 1
19	R/W	—	Hi-res decimator 20-bit incrementer and diagnostic control register 2

Table 1–21: Device Interrupt Levels

Interrupt Level	Device	Interrupt Signal
Level 0	None	
Level 1	Floppy	Floppy
Level 2	Duart Interrupt (Acquisition and Front Panel Processor Communications)	DUART
Level 3	FIFO Interrupt and DSP Interrupt	FIFO and TRISTAR
Level 4	GPIB Interrupt	GPIB
Level 5	Option 1 Interrupt, Option 2 Interrupt, and I/O Option Bus Interrupt	OPTION1, OPTION2, and IOBUS
Level 6	Display Interrupt to System Processor, Console Interrupt, and Timer (6.5536 ms periodic interrupt)	DISPLAY, CONSOLE, and TIMER
Level 7	50 Ω overload interrupt, and PFBAR Interrupt (power is going away in ~10 ms)	50OHMINT, POWERFAIL

Table 1–22: Interrupt Mask Register 0900 0000 (R/W)

68020 Data Bit	Signal Name	Description
D31	MSKFLOPPYINT	Masks floppy interrupt
D30	MSKOPTION2INT	Masks option board 2 interrupt
D29	MSKFIFO	Masks FIFO interrupt
D28	MSKIOINT	Masks I/O bus interrupt
D27	MSKDUART	Masks Duart interrupt
D26	MSKOPTION1INT	Masks option board 1 interrupt
D25	MSKTIMER	Masks timer interrupt
D24	MSKDISP	Masks display interrupt

Table 1–23: Miscellaneous Register 0920 0000 (R/W)

680020 Data Bit	Signal Name	Description
D31	~RESETACQP	Resets acquisition processor (not an interrupt mask)
D30	~020INTTS	If asserted, interrupts Tristar (not an interrupt mask)
D29	~TSRESET	Resets the DSP. Can be asserted to forcibly take the DSP bus. Deasserting restarts the DSP
D28	SYSROMWTS1	Most significant bit of the number of system ROM wait states
D27	SYSROMWTS0	Least significant bit of the number of system ROM wait states
D26	MASKTSINT020	Masks the DSP interrupts to the CPU
D25	BUSREQ	Requests the DSP bus (the nice mode of operation)
D24	TSPP = Write TSFO = Read	Bits for the DSP diagnostic testing

Table 1–24: Interrupt Read Register 1 0940 0000 (Read Only)

680020 Data Bit	Signal Name	Description
D31	~FLOPPYINT	Application memory card interrupt
D30	~OPTION2INT	Interrupt from option compartment number 2
D29	~FIFOINT	FIFO interrupt (the DSP has placed something in FIFO)
D28	~IOINTERRUPT	I/O bus interrupt
D27	~DUARTINT	DUART interrupt
D26	~OPTION1INT	Interrupt from option compartment number 1
D25	~TIMERINT	6.5536 ms timer interrupt
D24	~DISPINT020	Display interrupt 68020

Table 1–25: Interrupt Read Register 2 0960 0000 (Read Only)

680020 Data Bit	Signal Name	Description
D31	LOW	
D30	BUSGRANT	The DSP has relinquished the D1, D2, and IM busses. Automatically asserted during ~TSRESET.
D29	~PF	First indication that power is going away, in 10 ms
D28	~50OHMINT	50 Ω attenuator overload interrupt
D27	~CONSOLEINT	Interrupt from cardedge console port
D26	~TSINT020	DSP interrupt to the CPU
D25	~GPIBINT	GPIB interrupt
D24	~LOW	

Table 1–26: Troubleshooting Procedure For LED Display

Test Name	LED Display (a failed test is preceded by a flashing decimal)	A11 DRAM Processor/Display Troubleshooting Procedure
Bus Control Read	1	Bus Control Register
Kernel RAM 1	2	Kernel RAM
Kernel RAM 2	3	Kernel RAM
Kernel RAM 3	4	Kernel RAM
BootROM Check Sum	5	BootROM Control
Bus Error Timeout	6	CPU Bus Error
Write Bus Control	7	Bus Control Register
CPU Interrupt Mask Register	8	CPU Interrupt
CPU Miscellaneous Register	9	CPU Interrupt
Timer Interrupt	a	Timer Interrupt
NV Ram Dsacks	b	Bdsack
FlashROM programming voltage is applied. NVRam is write protected.	c	On the A11 DRAM Processor/Display board press S1002 towards the back of the oscilloscope and cycle power.
FlashROM DSACKS	d	Bdsack
FlashROM Check Sum	e	FlashROM
ID Register The LED displays the A11 DRAM Processor/Display ID in hex: the most significant nibble (4 bits) first and then the least significant nibble.		ID Register

The Columbia primitive input is an eight bit dip switch (S1001) on the A11 DRAM Processor/Display board. When the system powers up the system processor honors any special requests made by the dip switch. The eight switches are active in the open position.

Table 1–27: DIP Switch Options

DIP Selection (8–1)	Action
0010 0000	Enter SDM Monitor via the GPIB
0011 0000	Enter SDM Monitor via Console RS-232
0110 0000	Expand error log and increase diag messages
0101 0000	Do not attach the ethernet
0100 1000	Do not add extra ram to pool
0100 0100	Do not execute diagnostics
0100 0010	Do not execute higher level code
0100 0001	Do not execute system ram test
1X00 0000	Loop or Skip ALL bootrom Tests
1X00 0001	Bus Control Read
1X00 0010	Kernel Ram Test 1
1X00 0011	Kernel Ram Test 2
1X00 0100	Kernel Ram Test 3
1X00 0101	Bootrom Check Sum
1X00 0110	Bus Error Timeout Test
1X00 0111	Write Bus Control (open)
1X00 1000	Interrupt Mask Register 1
1X00 1001	Miscellaneous Register
1X00 1010	Timer Interrupt (Auto-Vector)
1X00 1011	NV Ram DSACKS
1X00 1100	Flashrom prog. voltage applied. NV Ram is write protected.
1X00 1101	Flashrom DSACKS
1X00 1110	Flashrom Check Sum
1X10 0000	Loop or Skip ALL Kernel Ram Tests
1X10 0001	Loop or Skip ALL Kernel Tests
1X10 0010	*Walk 7 Segment LED
1X10 0011	*Display Processor Version Number

If X = 1 (open) – *skip* (do not execute) test(s).

If X = 0 (closed) – *loop* on test(s).

*** executes forever – power must be cycled to stop test**

The Columbia primitive output consists of a 7 segment LED (DS1) on the A11 DRAM Processor/Display board.

Table 1–28: A11 DRAM Processor/Display LED (DS1)

LED Display	Explanation
Decimal Point (DP)	When this precedes one of the hex numbers, the particular test the number represents has failed.
.E	This indicates an exception
.11	This indicates an interrupt
.P	This indicates a non maskable interrupt
.8	Displayed at power-up or reset
0	First displayed after power up
1	Bus Control Read diagnostic
2	Kernel RAM 1 diagnostic
3	Kernel RAM 2 diagnostic
4	Kernel RAM 3 diagnostic
5	BootROM Check Sum diagnostic
6	Bus Error Timeout diagnostic
7	Write Bus Control diagnostic
8	CPU Interrupt Mask Register diagnostic
9	CPU Miscellaneous Register diagnostic
a	Timer Interrupt diagnostic
b	NV RAM Dsacks diagnostic
c	FlashROM programming voltage is applied. The NV RAM is write protected.
d	FlashROM Dsacks
e	FlashROM Checksum