

## • Measuring Logic

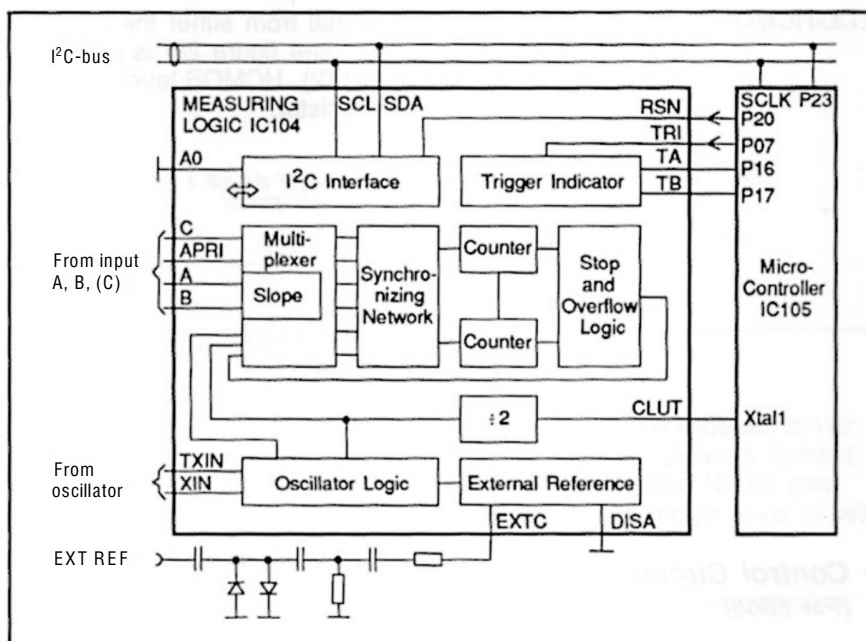


Figure 30. Measuring logic.

The Measuring Logic, which handles the actual measuring, is housed in a custom designed integrated circuit IC104.

Depending on the desired measuring input, the multiplexer selects A, B, C or APRI (APRI from the divider circuit).

The multiplexer receives the clock signal XIN via the Oscillator Logic. If the counter is equipped with an MTCXO oscillator, the signal TXIN is used for the input signal from the temperature oscillator.

If an external reference (EXT REF) is used, the clock signal is received via EXTC, then amplified and converted to HCMOS level in the External Reference circuit.

The clock signal is divided by two and is then fed to the Micro-Controller as CLUT.

The Synchronizing Network receives the selected input signal and the clock signal. The circuit synchronizes the clock signal to measuring start and measuring stop. This function prevents from the counting of incomplete input pulses at the start and stop of the measurement.

The input signal and the clock signal are counted in separate Counter registers. Some measuring modes only count one of the signals and then utilize the two registers connected in series.

The Stop and Overflow Logic tries to stop the measurement if the counter registers overflow. If it does not succeed, the counter indicates "Error OF".

The Measuring Logic and the Micro-Controller communicates via the I<sup>2</sup>C-bus.

A program flowchart, illustrating the program flow during a measuring cycle, is presented after the section on "Micro-Controller and I<sup>2</sup>C-bus".

# • Micro-Controller and I<sup>2</sup>C-Bus

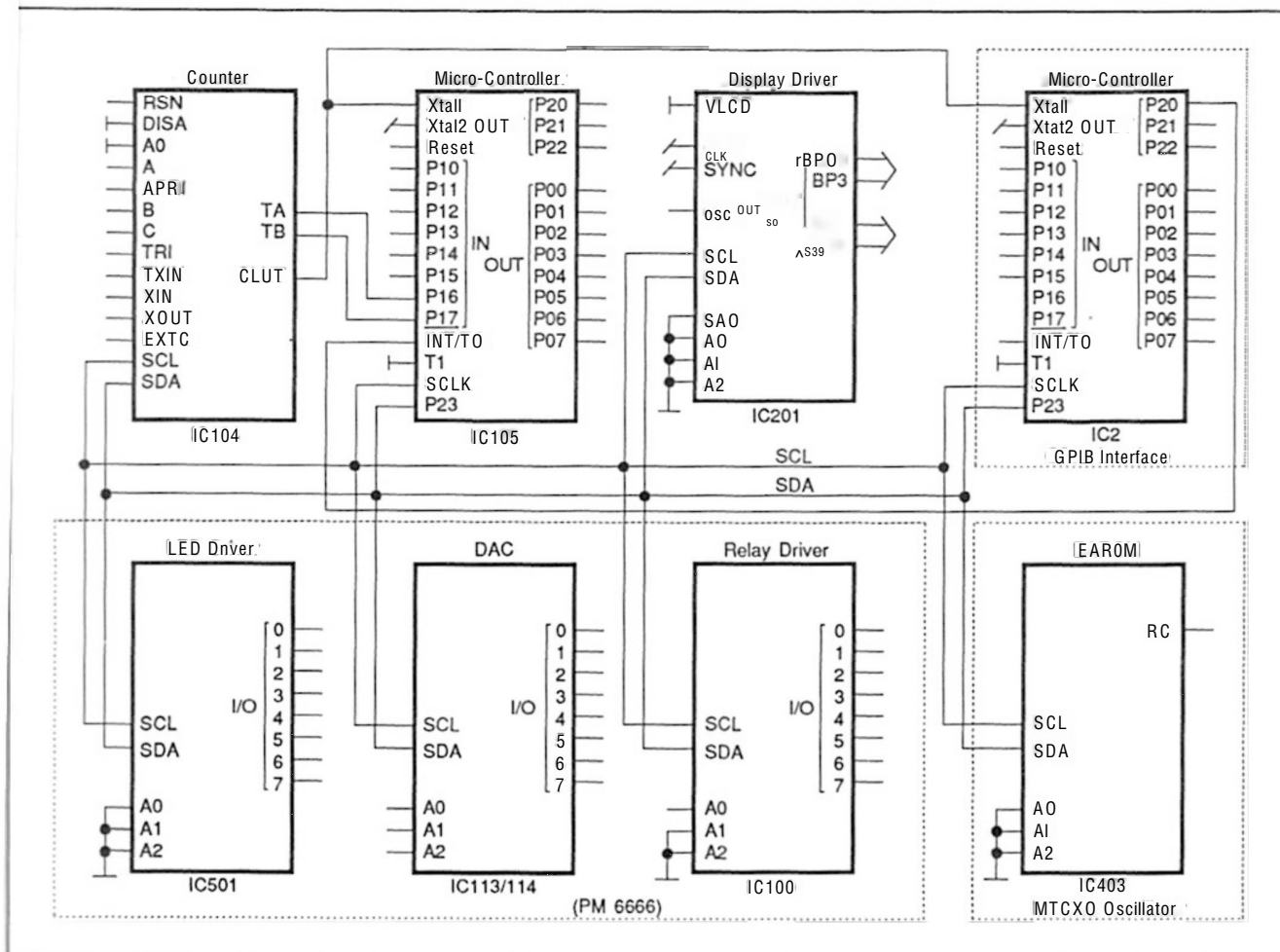


Figure 31. Micro-Controller and I<sup>2</sup>C-bus.

## Micro-Controller

The Micro-Controller is a single chip microcomputer, IC105, with an internal 128 byte RAM and 6 kbyte ROM. It has 19 I/O-ports.

The Micro-Controller communicates with the other counter circuits via the I<sup>2</sup>C-bus. When information is to be sent on the bus the Micro-Controller outputs a 100 kHz clock signal on the clock line SCL. Before transmitting or receiving data it also sends the unique 1-byte address of the receiving circuit on the data line SDA.

## I<sup>2</sup>C-bus

The I<sup>2</sup>C-bus is a 2-line serial bus for the communication between the ICs. The Micro-Controller, IC105, controls the communication with the clock-line SCL. One or more slaves can read or write on the data-line SDA.

The SDA and SCL are high at stand by. All ICs connected to the bus can sink SDA to low as they are connected via open collector outputs.

The Micro-Controller starts and stops the communication by sending terms of start and stop:

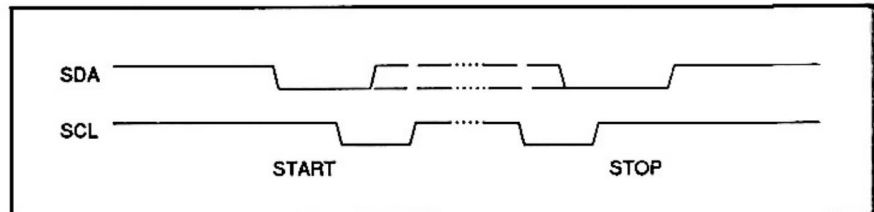


Figure 32. Terms of start and stop.

During transmission the SDA can be changed only when the SCL is low.

The Micro-Controller always begins to send the address information. The format of this address information is 7 address bits, one read/write bit, and one acknowledge bit.

Addressed slave accepts by keeping the SDA line low while the acknowledge bit (ACKN in figure 33) is sent by the Micro-Controller.

**Example of addressing (address 30H):**

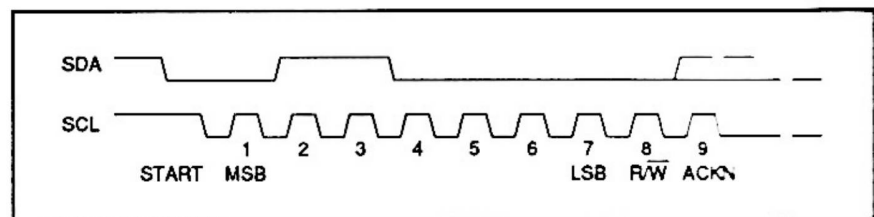


Figure 33. Addressing.

The read/write bit  $\overline{R/W}$  has the following meaning:

$\overline{R/W} = 1$  means information from the slave to the Micro-Controller.  
 $\overline{R/W} = 0$  means information from the Micro-Controller to the slave.

The data information is sent after the address information. The format of the data information is 8 data bits followed by one acknowledge bit. The receiver accepts by keeping the SDA line low while the acknowledge bit (ACKN in figure 34) is sent.

**Example of data transmission (data 9BH):**

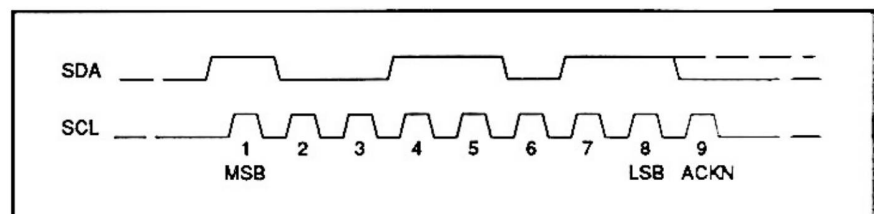


Figure 34. Data transmission.