SONY®

CXD7500M

Voltage Control Type Variable Resistor

Description

CXD7500M is a resistive gate type MOS FET featuring linear current vs voltage characteristics over a wide range of drain voltage low distortion and good linearity make this device suitable for use as a voltage controlled variable resistor.

Features

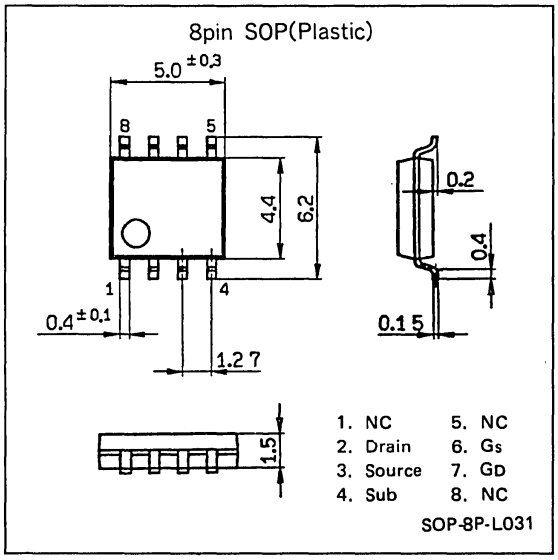
- Voltage controlled variable resistor
- Good linearity, low distortion variable resistor.
- As V_{DS}-I_{DS} characteristics are linear through a number of ±V, the dynamic range is wide.
- Signals up to VHF band can be handled.

Structure

Silicon P channel MOS FET

Package Outline

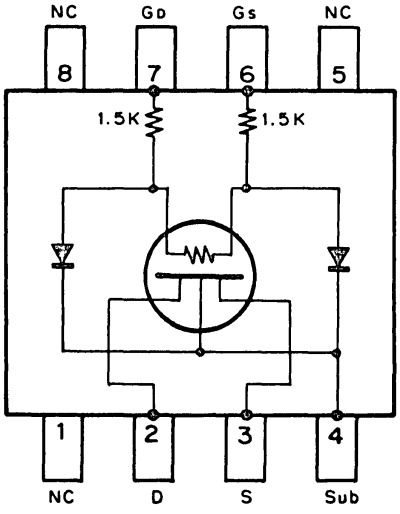
Unit: mm



Absolute Maximum Ratings (Ta=25°C)

∘ Drain to source voltage	V_{DS}	−20(V_{GB}=0V)	V
∘ Gate to substrate voltage	V_{GB}	−25	V
∘ Drain to substrate voltage	V_{DB}	−25	V
∘ Drain current	I_D	±15	mA
∘ Channel temperature	T_{ch}	80	°C
∘ Storage temperature	T_{stg}	−55 to +150	°C
∘ Allowable power dissipation	P_D	150	mW

Equivalent Circuit and Pin Configuration (Top View)



80961-HP

Electrical Characteristics

(Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain to source voltage	V_{DSS}	$I_{DS}=-10\mu A$	−20			V
Drain current	I_{DS}	* $V_{GS}-V_{THE}=-10V$ $V_{DS}=-2V$, * $V_{BS}=10V$	−6	−10		mA
Threshold voltage	V_{THO}	* $V_{BS}=0V$, $I_{DS}=-1\mu A$, $V_{DS}=-1V$,	−0.4	−1.0	−2.5	V
Effective threshold voltage	V_{THE}	* $V_{BS}=10V$, $I_{DS}=-1\mu A$, $V_{DS}=-1V$,	−0.4	−1.2	−3.0	V
Min. channel resistance	R_{cho}	* $V_{GS}-V_{THE}=-10V$, * $V_{BS}=10V$, $V_{DS}=-1V$,	150	200	300	Ω
Low frequency distortion	L_{THD}	V_{in}=0dBm $V_{out}=-6$dBm f_{in}=20Hz, * $V_{BS}=10V$,		0.6		%
Standard distortion	S_{THD}	V_{in}=0dBm $V_{out}=-6$dBm f_{in}=1kHz, * $V_{BS}=10V$,		0.4		%
Gete resistance	$R_{(GS-GD)}$	$V_{(GS-GD)}=-10V$	50		1000	MΩ
Gete cutoff current	I_{GSS}	* $V_{GS}=-5V$, $V_{DS}=0V$, $V_{BS}=0V$, * $V_{BS}=0V$			−0.2	μA

* V_{BS}: Substrate (Base) -to Source Supply Voltage
* G_D, G_S Shorted and tested.

Electrical Characteristics Test Circuit
Distortion
Channel Resistance

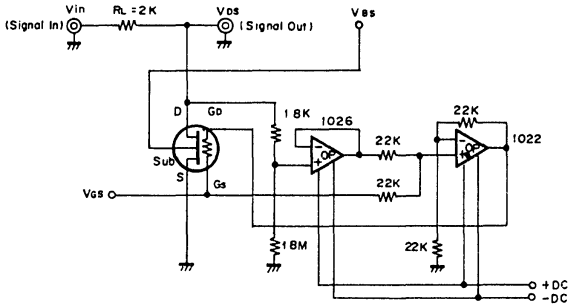


Fig. 1

Parallel Equivalent Capacitance
Parallel Equivalent Resistance

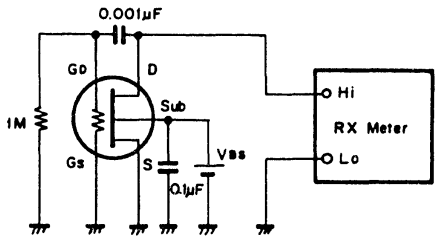
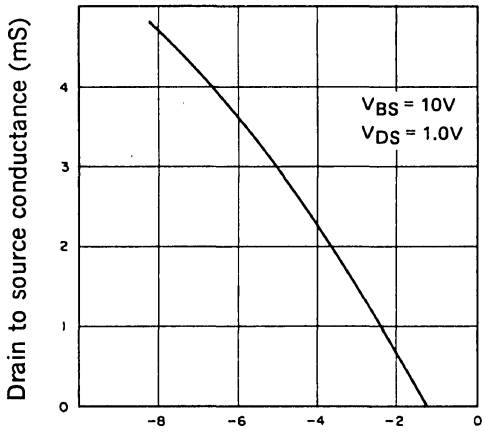


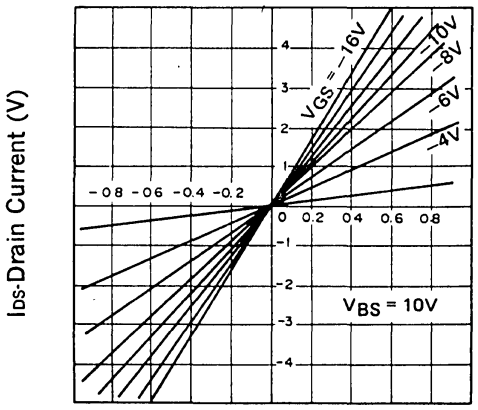
Fig. 2

Drain to source conductance vs. Gate to source voltage



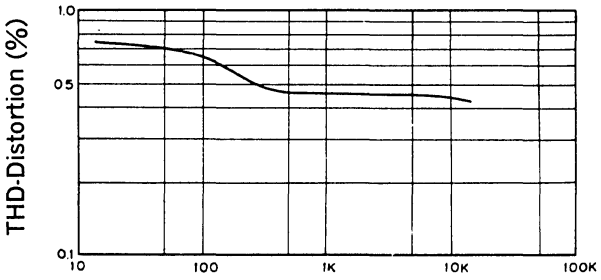
V_{GS}-Gate to source voltage (V)

Drain current vs. Drain to source voltage



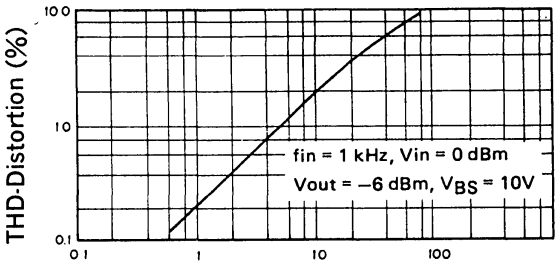
V_{DS}-Drain to source voltage (V)

Distortion vs. Frequency



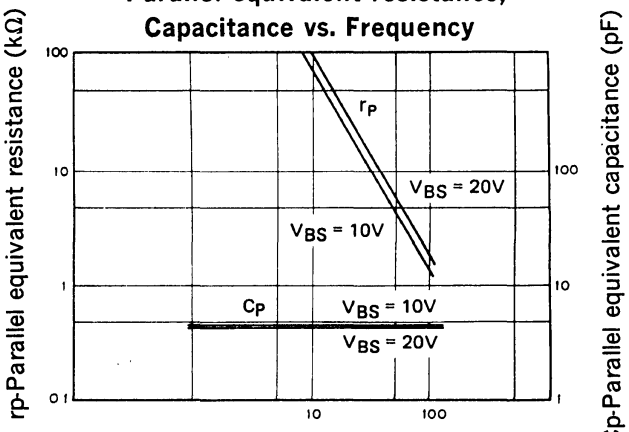
f-Frequency

Distortion vs. Load resistance



R_L-Load resistance (kΩ)

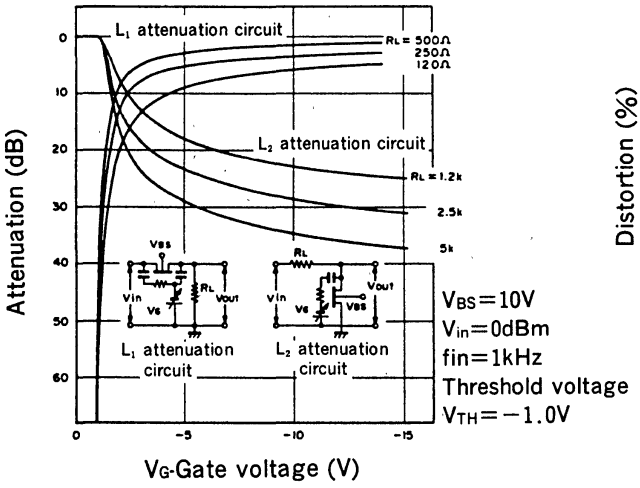
Parallel equivalent resistance, Capacitance vs. Frequency



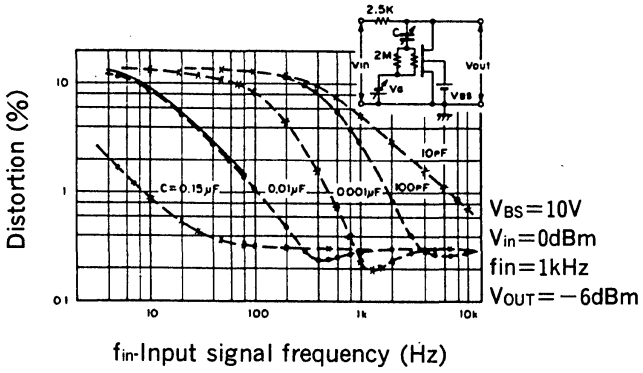
f-Frequency (MHz)

• Example of characteristics at L attenuator circuit

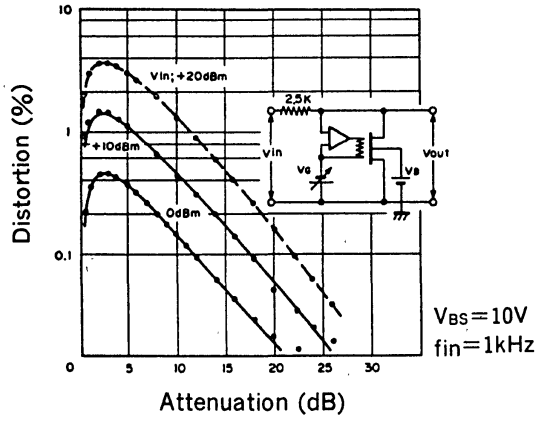
Attenuation vs. Gate voltage



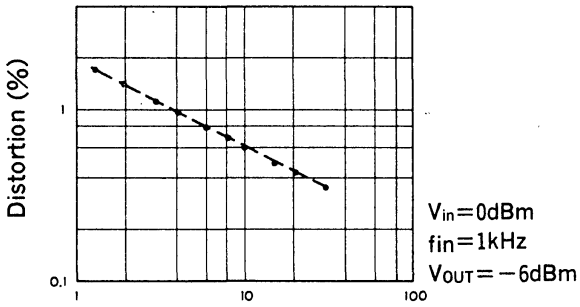
Distortion vs. Input signal frequency



Distortion vs. Attenuation



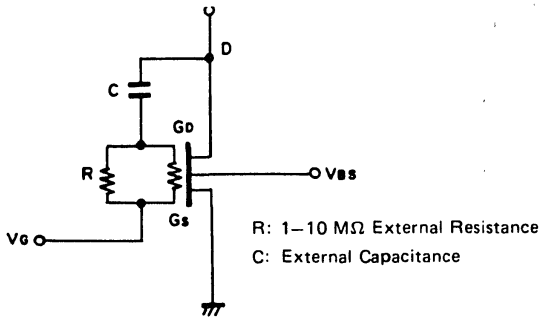
Distortion vs. Substrate impressed voltage

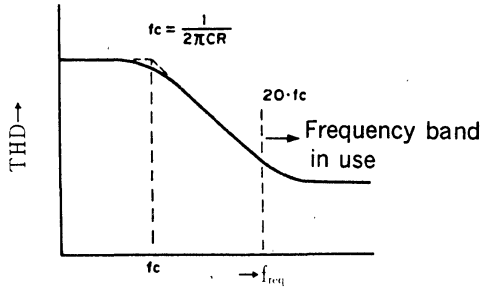


• Circuit for Practical Use

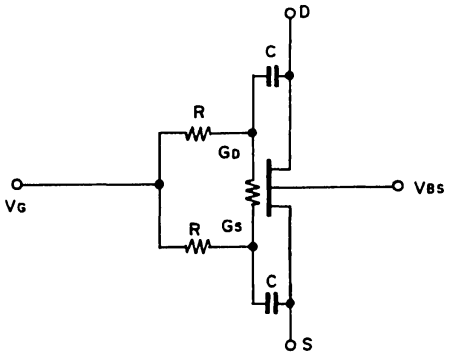
1) When used with source grounded

As the gate resistor is extremely high at several hundred MΩ and the resistance values uneven, it is advisable to attach a 1 to 10 MΩ external resistor. Moreover, the value of the coupled capacitance C is determined according to frequency band in use. As a guideline, use a cut off frequency less than 1/20 the lower limit value of the frequency in use.

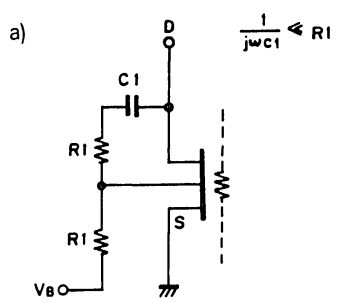


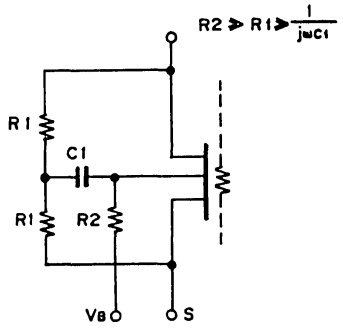


2) For source to drain floating usage
Should the frequency of the control voltage be comparatively high and the transient distortion grow problematically worse, source to drain is used floating.



3) Attenuation of the spacecharge effect
To attenuate non-linearity caused by the effects of Sub spacecharge effect, feedback 1/2 the drain to source voltage. This should improve the distortion ratio.





4) Attenuator circuit examples