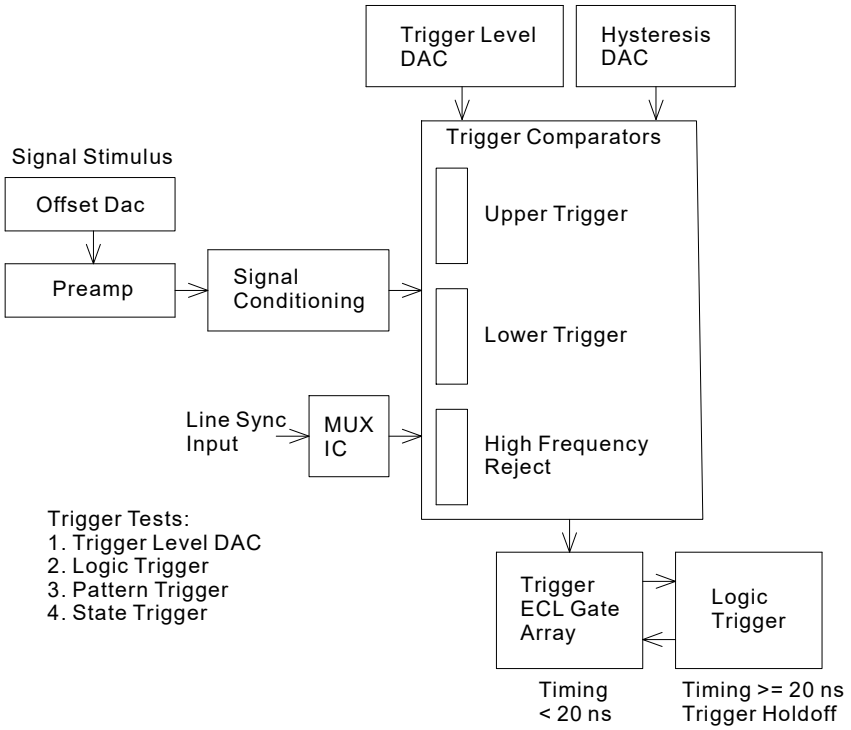
Trigger System Self Tests Overview

The Trigger System Self Tests Diagram (Figure 1) gives an overview of the components of the trigger system. The system can be broken down into five major blocks:

Figure 1



1 Signal Stimulus - The vertical offset dac is used to create a voltage that can be slewed through a trigger threshold for channel edge trigger and violation trigger tests or to act as a clock transition for state trigger tests. The offset dac may also be held at a fixed value to give a high or low setting for state and pattern trigger testing.

2 Signal Conditioning - The signal conditioning circuitry is only exercised in the normal and high frequency reject path settings.

3 Trigger Comparators - There are three trigger comparators associated with each trigger channel. The upper trigger level comparator is used for edge trigger mode and the upper trigger level of the violation trigger mode. The lower trigger comparator is the second trigger for the violation trigger mode. The upper and lower level comparators are contained in a single package for each channel. A third comparator is used exclusively for the high frequency reject trigger mode. The line sync trigger has a completely separate path. The line signal is run through a 500hz low pass filter to the line sync comparator. The output of the line sync comparator is multiplexed into an external input of the trigger ECL gate array.

4 The trigger ECL gate array - Contains the circuitry for managing the trigger system. The ECL gate array handles state triggering and glitch triggering and timing modes < 20ns.

5 Logic trigger - Contains a system of counters to handle pattern triggering and holdoff. Timing > 20ns is handled in the logic trigger.

Trouble Shooting the Trigger System

The problem in trouble shooting the trigger system is to be able to isolate a specific portion of the circuit with a self test. The logic trigger self test with the exception of the 100Mhz startable oscillator is very self contained within the logic trigger IC If the logic trigger self test fails, either the logic trigger IC,

100Mhz startable oscillator or serial data interface is likely to be at fault.

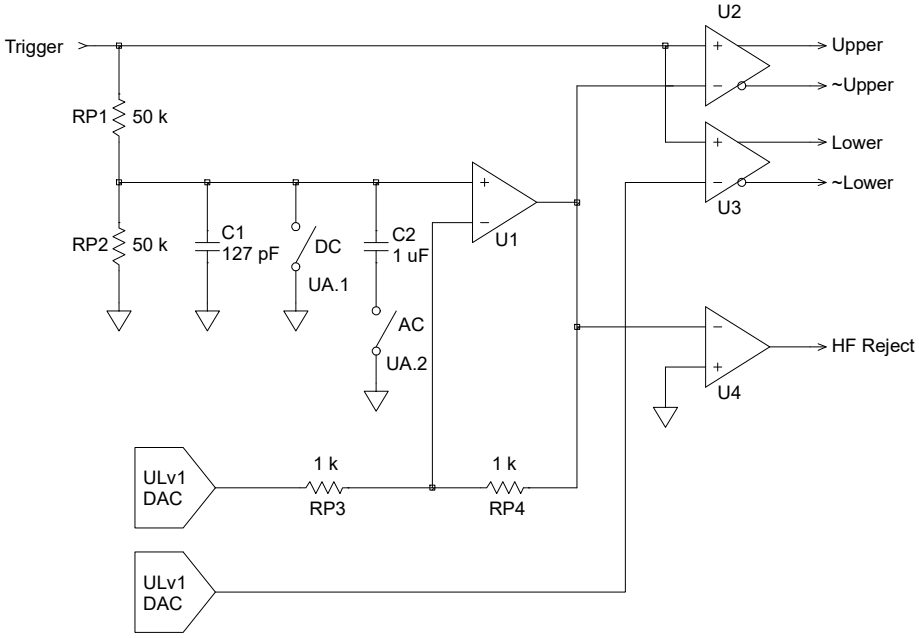
The trigger ECL gate array is more difficult since it doesn't have the capability of being tested as an integral unit. Since there are a variety of comparators in the system, if any channel triggers in any configuration then the trigger ECL gate array has at least some chance of being functional.

A particular comparator on an individual channel can be considered suspect if that channel will trigger in a configuration using a different comparator.

Trigger Conditioning Circuits and Trigger Comparators

The trigger conditioning circuit is shown in the simplified block diagram (Figure 2).

Figure 2



The following is a brief circuit description:

1 DC mode - analog switch UA.1 is closed, U1 acts as an inverting gain of 1 amplifier for the upper level trigger dac signal.

2 AC mode - analog switch UA.1 is open and UA.2 is closed. The trigger signal is divided by 2 through precision resisters Rp1 and Rp2. C2 produces a 7hz corner. For frequencies below 7hz, U1 restores the amplitude to the non-inverting input of comparator U2. Due to the comparator hysteresis, triggering will not occur. Frequencies above 7hz are attenuated and don't get through U1. The high frequencies will only appear at the non-inverting input of U2 and triggering can occur if the proper trigger level is set.

3 Low Freq. Reject mode - analog switch UA.1 is open and UA.2 is open. C1 causes a 50khz corner. Frequencies below 50khz are amplified and applied to the inverting input of the upper trigger level comparator. Due to hysteresis, the comparator will not trigger on the frequencies below 50khz. Frequencies above 50khz will be attenuated. They will only appear at the non-inverting input and triggering can occur if the proper trigger level is set.

4 High Freq. Reject - analog switch UA.1 is open and UA.2 is open. C1 causes a 50khz corner. Signals below 50khz are amplified and applied to comparator U4.

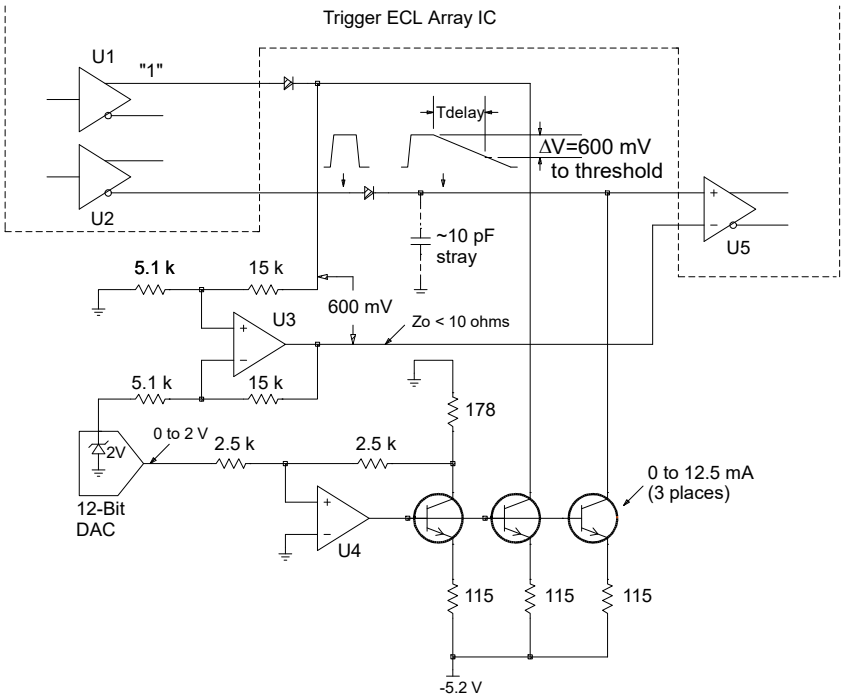
5 Violation Trigger - Only available in DC mode. Lower level trigger dac signal controls comparator U3.

Trigger ECL Array Support Circuitry

The trigger ECL Array IC requires some support circuitry to accomplish trigger timing that the logic trigger cannot perform. i.e. < 20ns. There are two identical timers, FFData Delay and FFClk Delay. Their function is to take the rising edge of the high performance ECL signals from the trigger ECL gate array IC, FFD and FFCK, and pass them through, but delay the falling edge by a programmed amount of time from 1 to 20ns.

A simplified block diagram of the data delay circuit is shown in Figure 3.

Figure 3



The delay technique used is to charge a small capacitance (stray capacitance of ~10pf in this case) through a rectifier and then discharge the capacitor through a controlled current source. To get accurate timing over temperature, U1 is used to establish a reference (output always 1 and similar loading for all time settings). A precise 600mV reference U3 is differentially referenced to the output of U1. The timing is the time it takes the rectified signal from U2 to decay 600mV. A 12 bit dac is used to control the capacitor discharge current to control the timing.