Ref.: Electronics Measurements and Instrumentation
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8-4 Normal-mode Rejection

During the discussion of the theory of operation of integrating DVMs, reference was made to their ability to reject signals that are in series with the input signal. These signals are called *normal-mode* or *superimposed noise signals*. This type of signal can be caused by electromagnetic pickup in the input leads to the DVM, or by an inherent component of the unknown signal, i.e., ripple at the output of a power supply. Typically, the frequency of these signals is an integer multiple of the power-line frequency, but in practice any type of disturbance may be present.

There are many applications where fast readings are required to characterize the unknown signal adequately. The removal of superimposed high-frequency components would be unacceptable. However, in the following discussion, assume that only the average value of a signal is desired.

In the description of the successive-approximation technique above, it was observed that the reading is achieved only after a number of successful decisions by the logic circuitry. Any incorrect decision along the way can cause a completely erroneous reading of the unknown signal. Superimposed noise is the most common cause for bad decisions of this kind.

If the dc value of the unknown is somewhat above 8.000 V in value but noise causes it to drop just below this level when the digital-to-analog feedback is generating 8.000 V, the reading will be incorrect.

It is obvious that the severity of such errors is more or less proportional to the amount of noise present. The same is true of the linear- and digital-ramp techniques. Superimposed noise can cause bad comparisons between the input signal and the internally generated ramp. The usual solution to such problems is the inclusion of a low-pass filter at the input of the DVM. The presence of such a filter does reduce the amount of noise presented to the digitizing circuitry, but it also increases the time of response of such instruments. Any filter that reduces the amount of noise significantly has a typical settling time on the order of 500 msec to 1.0 sec. This settling time has to be added to the digitizing time of the instrument in determining the true reading rate.

All the integrating DVMs discussed above employ techniques that make use of a specific period of time called either a *gate length* or an *integrating period*. During this period of time, the signal present at the input of the DVM is truly integrated and the average signal present is indicated on the front panel. A good example of this is the waveform used in Fig. 8-9. Although this example was used in conjunction with the technique using voltage-to-frequency conversion, the same would be true of the dual-slope technique.

Assume the input to an integrating DVM can be presented by

$$v(t) = V_1 \sin \omega t \tag{8-4-1}$$

In this example, it is assumed that there is no dc component present in the input signal. In developing this general case, it will be assumed that the integration interval begins at $t - t_1$ and ends at $t - t_1 + T$, where T is the period of integration or the gate length. The average voltage during this integration period is

$$\begin{aligned} V_{av} &= \frac{V_1}{T} \int_{t_1}^{t_1+T} \sin \omega t \, dt \\ &= -\frac{V_1}{\omega T} \cos \omega t \Big]_{t=t_1}^{t=t_1+T} \\ &= -\frac{V_1}{\omega T} [\cos \omega(t_1 + T) - \cos \omega t_1] \end{aligned} \tag{8-4-2}$$

By expansion of Eq. (8-4-2), the average value is

$$V_{av} = -\frac{V_1}{\omega T} [-2 \sin \tfrac{1}{2} (2\omega t_1 + \omega T) \sin \tfrac{1}{2} (\omega T)] \tag{8-4-3}$$

where V_{av} can be maximized by choosing t_1 so that

$$\sin \tfrac{1}{2}(2\omega t_1 + \omega T) = 1 \tag{8-4-4}$$

Substituting Eq. (8-4-4) in Eq. (8-4-3) gives the expression

$$\begin{aligned} V_{av}(\max) &= \frac{2V_1}{\omega T} \sin \frac{1}{2}\omega T \Big]_{\omega = 2\pi f} \\ &= \frac{V_1}{\pi f T} \sin \pi f T \end{aligned} \tag{8-4-5}$$

As the frequency of the superimposed noise approaches zero, V_{av} (max) approaches V_1. In order to develop an expression for attenuation as a function of frequency, it is necessary to establish the ratio of the value of the signal at 0 Hz to its value at a specific frequency.

$$\left| \frac{V_1}{(V_1/\pi f T) \sin \pi f T} \right| = \frac{\pi f T}{\sin \pi f T} \tag{8-4-6}$$

A plot of Eq. (8-4-6) is shown in Fig. 8-14. As seen in this figure, infinite cusps of rejection occur at intervals determined by $fT = n$, where $n = 1, 2, \ldots, K$. In this instance, the gate length is 1.0 sec.

By the appropriate choice of the integration interval, maximum rejection of line-related frequencies can be obtained. This is why many gate lengths are 16.67 msec, 100 msec, or other multiples of 16.67 msec in length. For use in Europe where the predominant line frequency is 50 Hz, 20.0 msec gate lengths should be used in place of 16.67 msec.

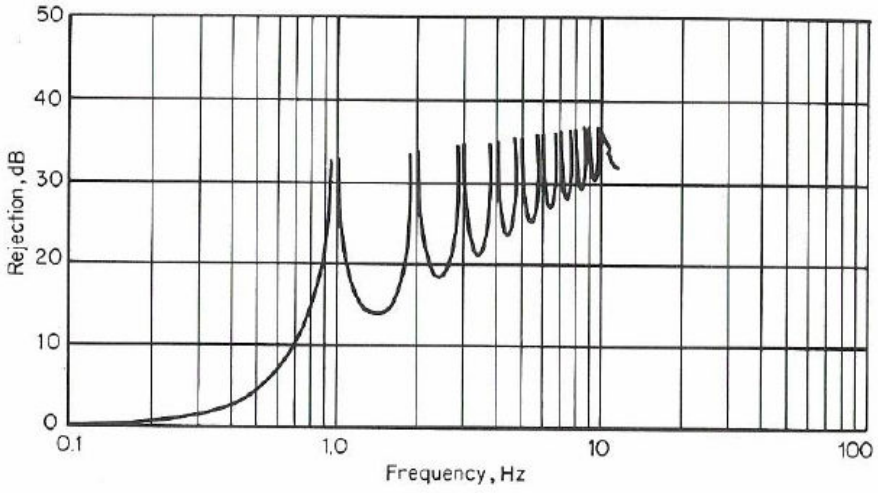

FIG 8-14 Normal-mode rejection characteristics of integrating DVM.