



HY313X

Configurations

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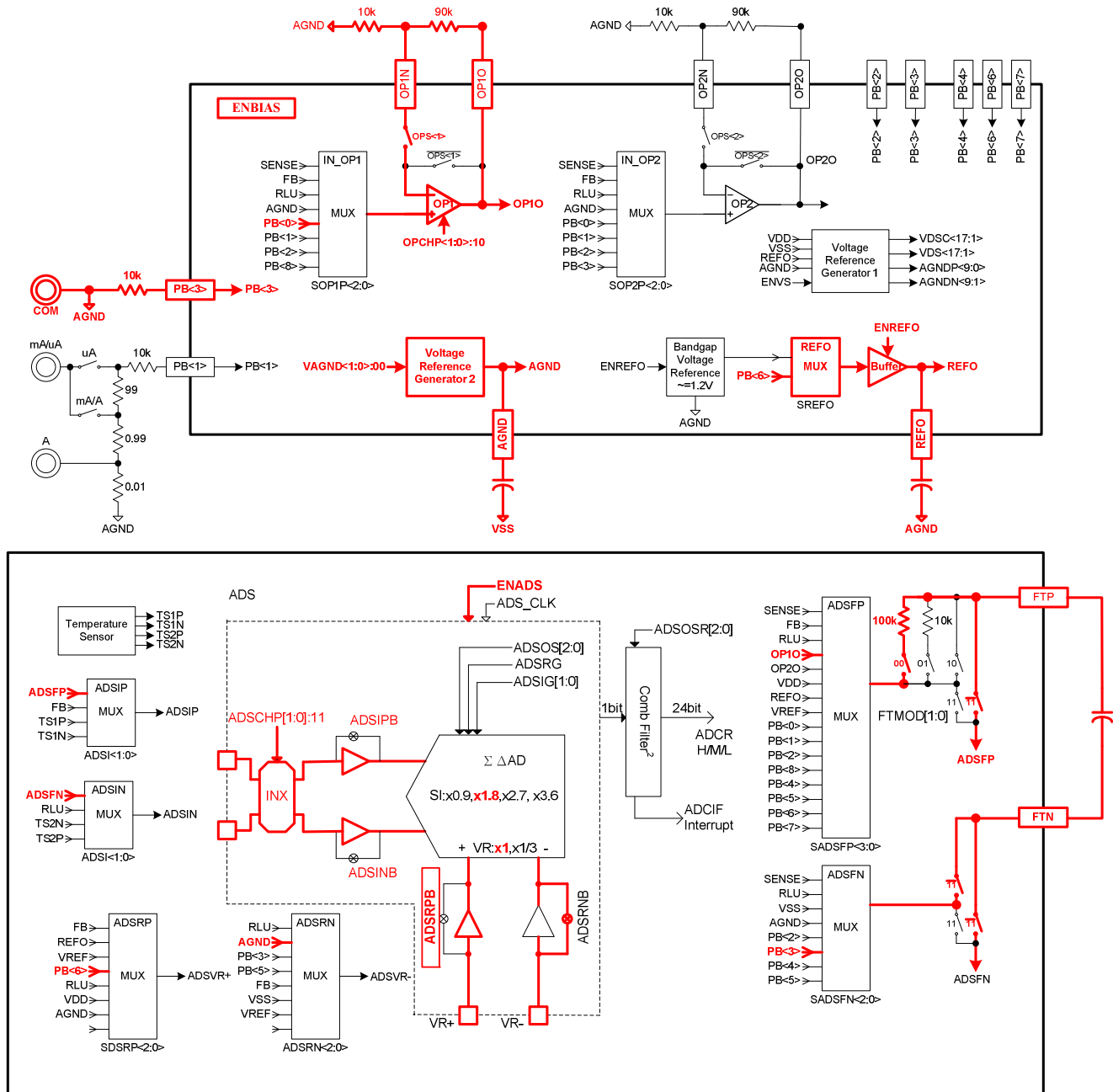
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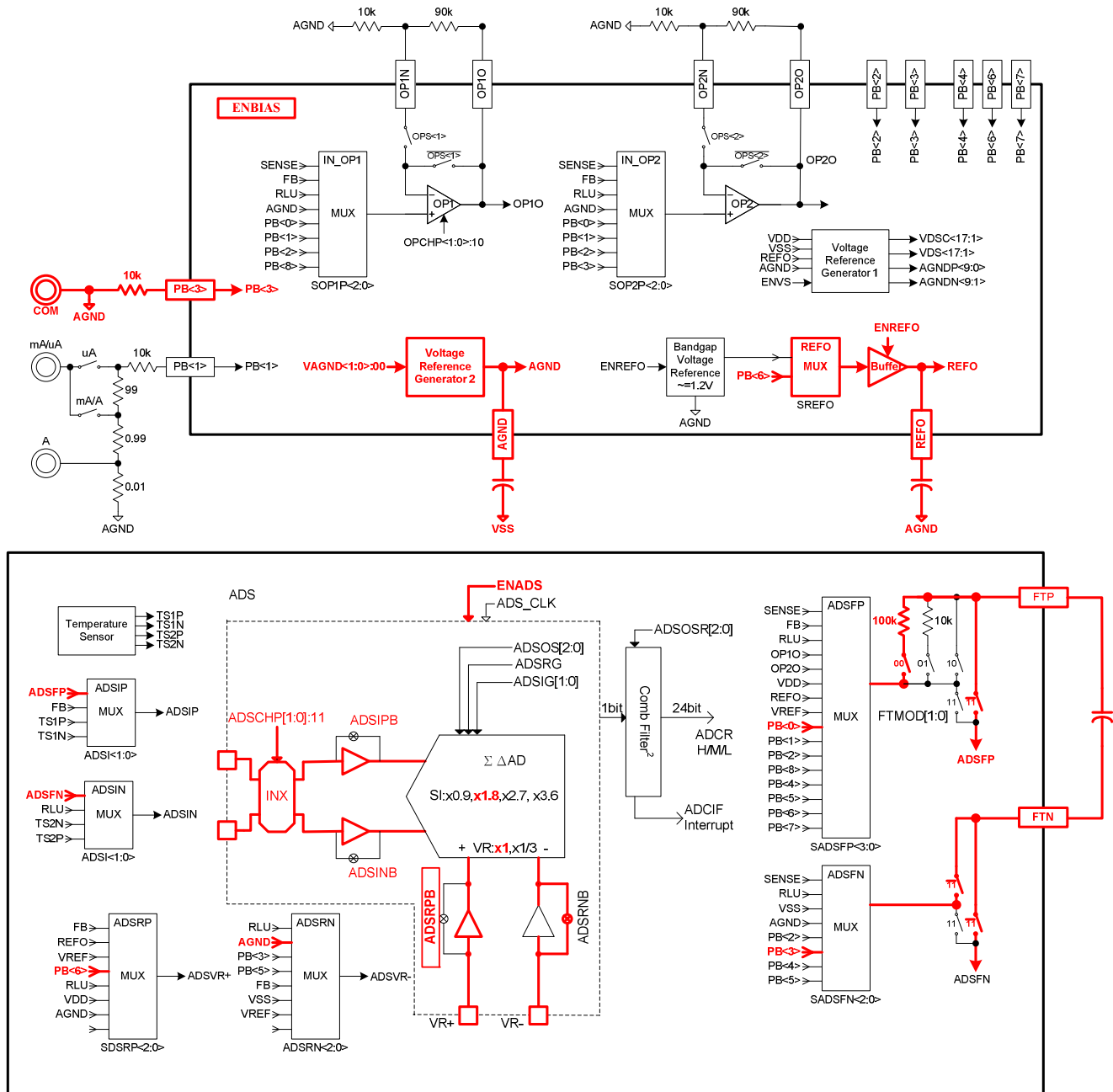
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1.2. DC50mV Measurement Network Configuration



1.3. DC500mV Measurement Network Configuration

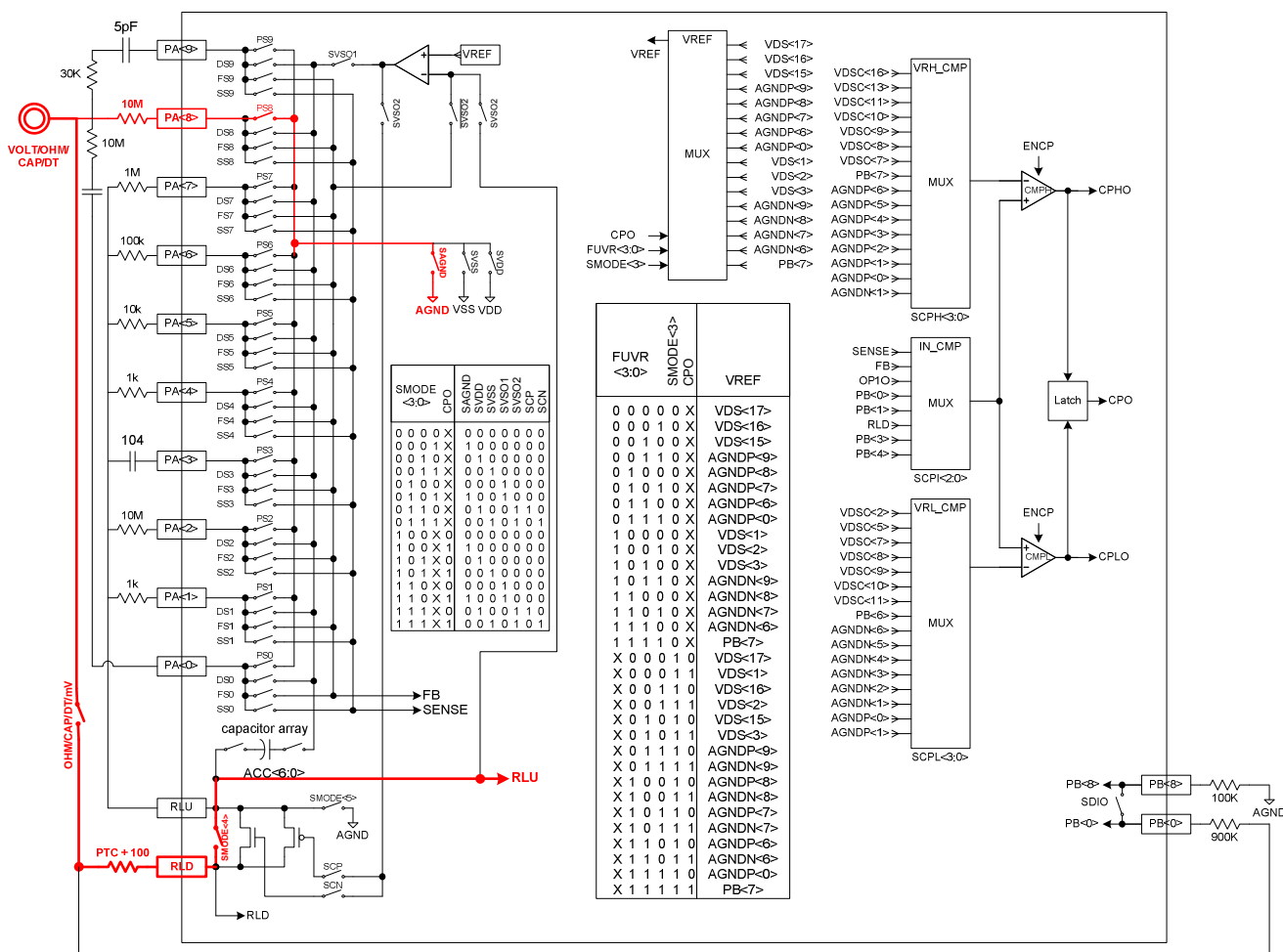


2. ACmV

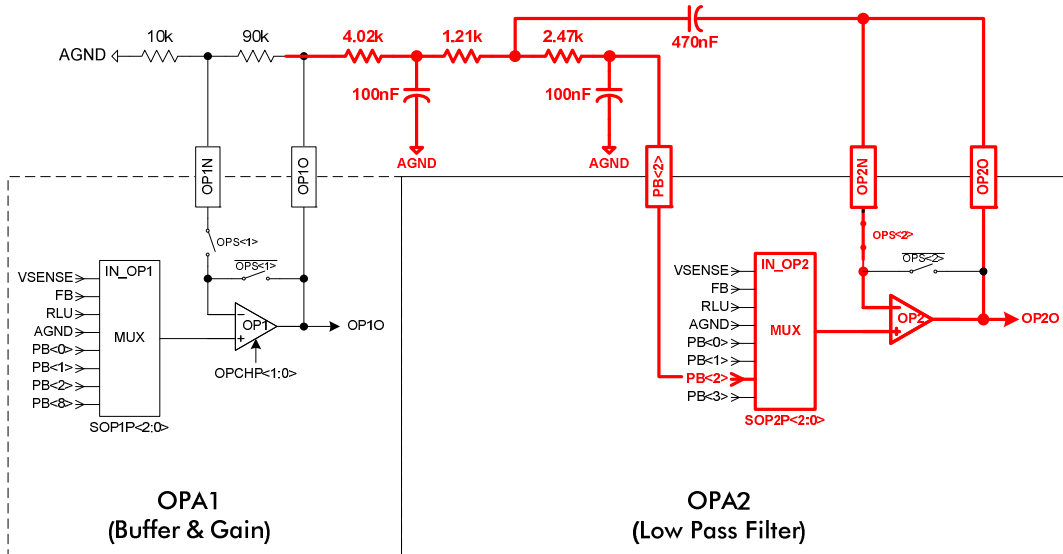
Due to high ADC input impedance, it is easily to sense 50/60Hz signal of the air that leads to unstable reading value after the testing probe was connected. It is recommended to connect input $10M\Omega$ to ground to reduce input impedance of DMM mV range.

The network configuration of 50mV and 500mV is similar. When measuring 50mV, it uses built-in OPA to amplify signal for 10 times then processing it in ADC.

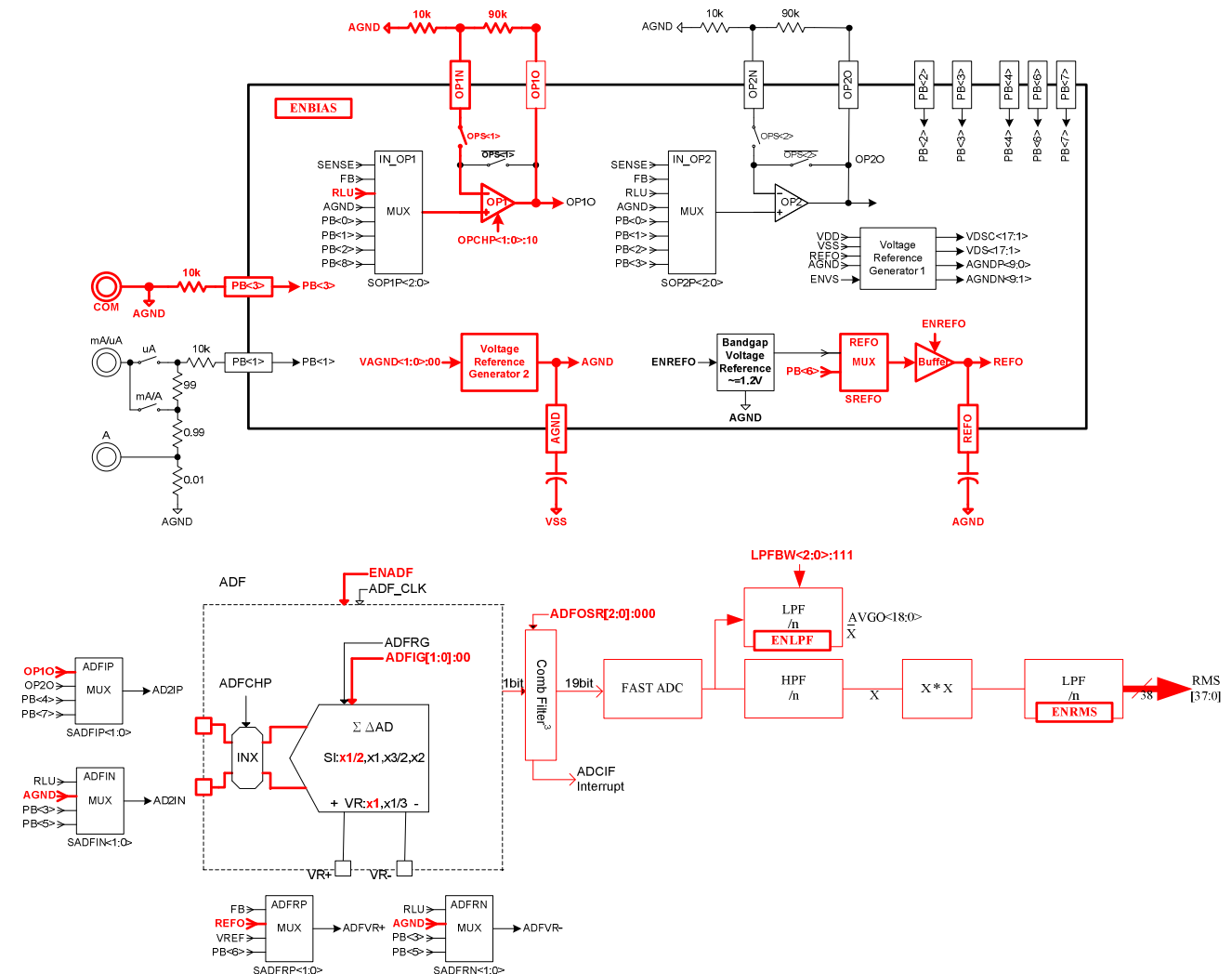
2.1. Input Network Configuration



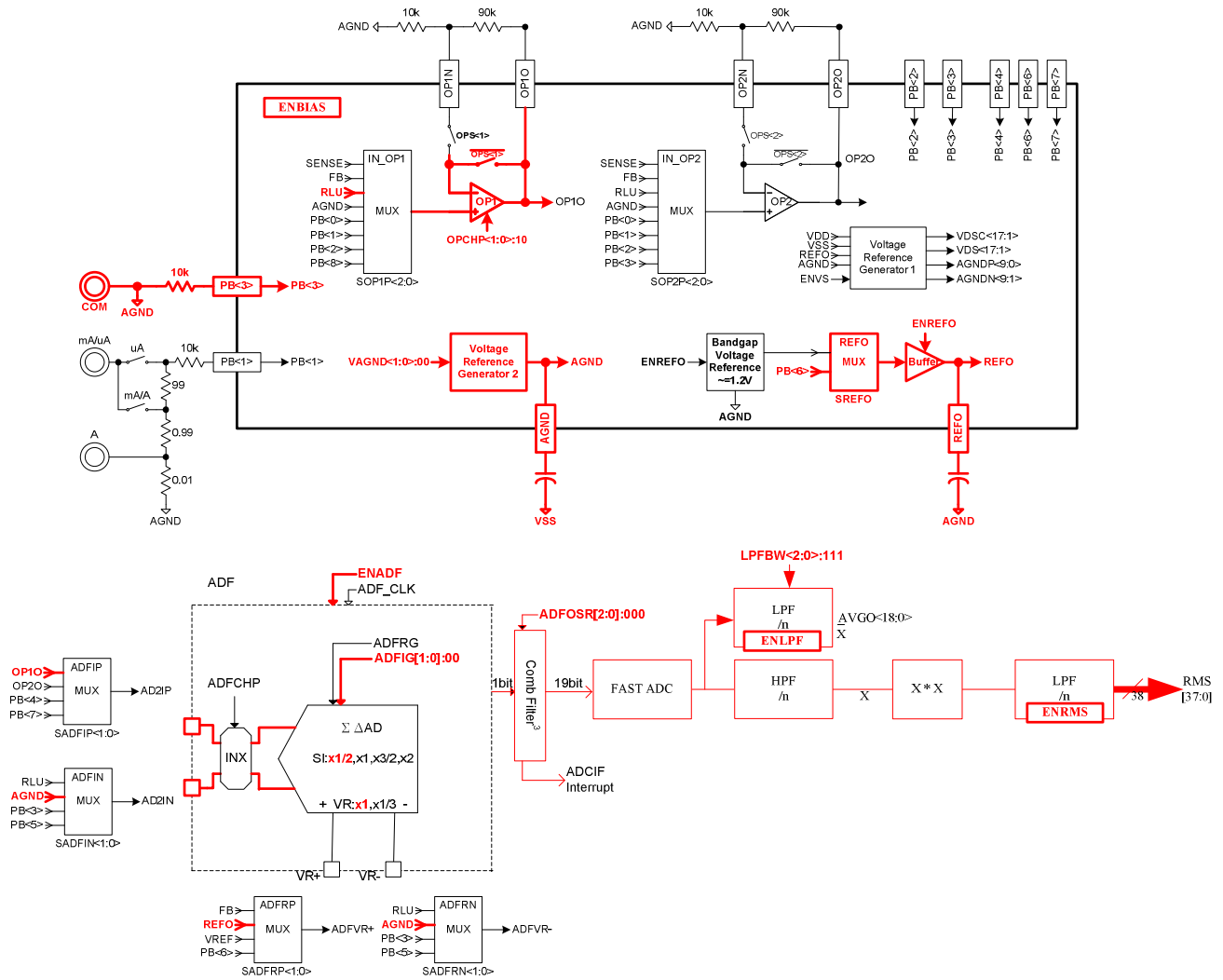
2.2. AC Low Pass Filter Measurement Network Configuration



2.3. AC50mV Measurement Network Configuration



2.4. AC500mV Measurement Network Configuration



3. DCV

30KΩ resistor and 5pF capacitor of the input end is for the use of ACV frequency compensation. When DCV is not in use, it is recommended to connect to ground and its input divider of voltage range is shown in below equation :

$$5V_Range \Rightarrow V_{IN} \times \frac{1.111M\Omega}{10M\Omega + 1.111M\Omega} = \frac{V_{IN}}{10}$$

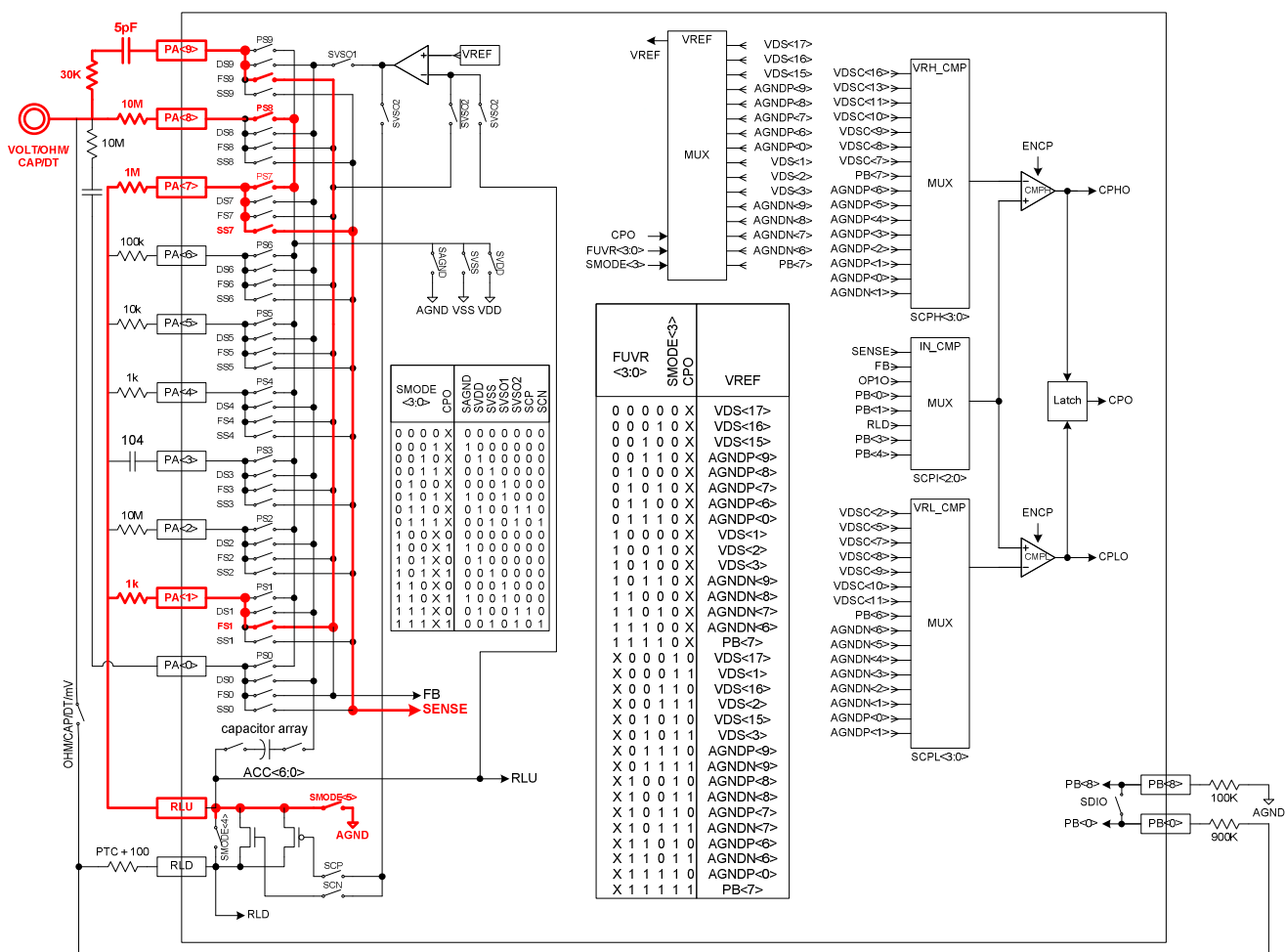
$$50V_Range \Rightarrow V_{IN} \times \frac{101.01K\Omega}{10M\Omega + 101.01K\Omega} = \frac{V_{IN}}{100}$$

$$500V_Range \Rightarrow V_{IN} \times \frac{10.01K\Omega}{10M\Omega + 10.01K\Omega} = \frac{V_{IN}}{1000}$$

$$1000V_Range \Rightarrow V_{IN} \times \frac{1K\Omega}{10M\Omega + 1K\Omega} = \frac{V_{IN}}{10000}$$

HY313x has two sets OPA that can be used to amplify 10 times of signal, realizing 500mV measurement by collocating with 5V network configurations.

3.1. 5V Input Network Configuration



The schematic diagram illustrates the VOLTIOHM CAPIDT circuit, which is designed for multi-channel measurement. The input bus is connected to a series of resistors and a capacitor array. The circuit includes a common input bus, a series of multiplexers (MUX), and comparators (CMP). The output of the comparators is connected to a latch and then to the CPO and CPHO pins. The diagram also includes a table for the SENSE pin configuration and a truth table for the SENSE pin.

SENSE	FB	OPIO	PB<0>	PB<1>	PB<2>	PB<3>	PB<4>
VDS<17>	0	0	0	0	0	0	0
VDS<16>	0	0	0	0	0	0	0
VDS<15>	0	0	0	0	0	0	0
AGNDP<9>	0	0	0	1	0	0	0
AGNDP<8>	0	0	1	0	0	0	0
AGNDP<7>	0	0	1	0	0	0	0
AGNDP<6>	0	0	1	0	0	0	0
AGNDP<5>	0	0	1	0	0	0	0
VDS<1>	1	0	0	0	0	0	0
VDS<2>	1	0	0	0	0	0	0
VDS<3>	1	0	1	0	0	0	0
AGNDN<9>	1	0	1	0	0	0	0
AGNDN<8>	1	0	1	0	0	0	0
AGNDN<7>	1	0	1	0	0	0	0
AGNDN<6>	1	0	1	0	0	0	0
PB<7>	1	1	1	0	0	0	0
VDS<17>	X	0	0	0	1	0	0
VDS<16>	X	0	0	0	1	0	0
VDS<15>	X	0	0	1	0	0	0
VDS<2>	X	0	0	1	0	0	0
VDS<15>	X	0	1	0	1	0	0
VDS<3>	X	0	1	0	1	0	0
AGNDP<9>	X	0	1	1	0	0	0
AGNDN<9>	X	0	1	1	0	0	0
AGNDP<8>	X	1	0	0	1	0	0
AGNDN<8>	X	1	0	0	1	0	0
AGNDP<7>	X	1	0	1	0	0	0
AGNDN<7>	X	1	0	1	0	0	0
AGNDP<6>	X	1	1	0	1	0	0
AGNDN<6>	X	1	1	0	1	0	0
PB<7>	X	1	1	1	1	1	1

The schematic diagram illustrates the VOLTIOHM CAPIDT module, which is designed for precise voltage and current measurements. It features a series of input channels (PA<0> to PA<15>) connected to a capacitor array. The circuit includes a table for FUVR, SMODE, and CPO settings, and a table for VREF settings. The module also includes a VREF input, a MUX, and various output signals like CPO, CPHO, and CPLD.

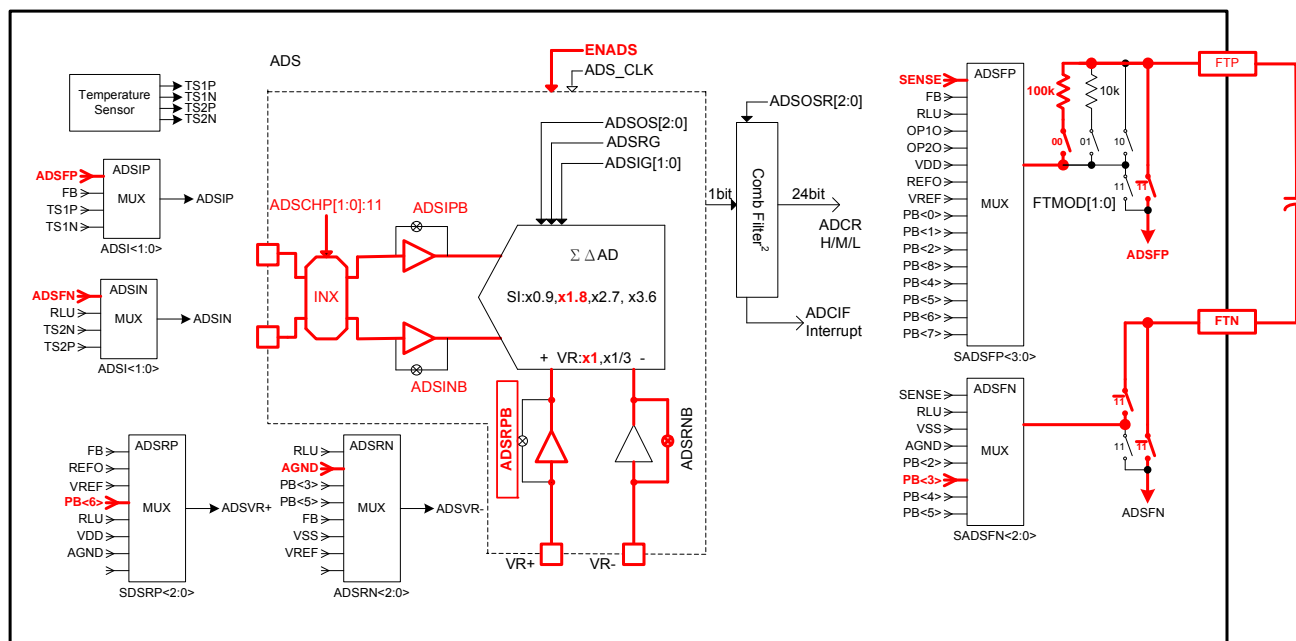
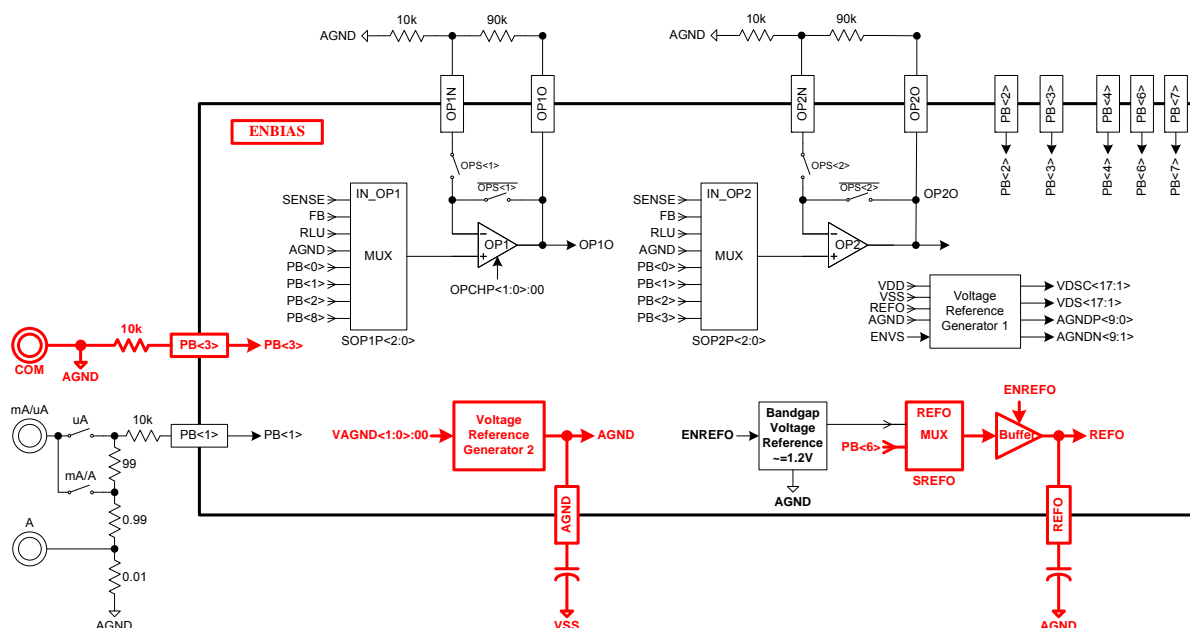
FUVR <3:0>	SMODE <3>	CPO	VREF
0 0 0 0	X	X	VDS<17>
0 0 0 1	X	X	VDS<16>
0 0 1 0	X	X	VDS<15>
0 0 1 1	X	X	AGNDP<9>
0 1 0 0	X	X	AGNDP<8>
0 1 0 1	X	X	AGNDP<7>
0 1 1 0	X	X	AGNDP<6>
0 1 1 1	X	X	AGNDP<0>
1 0 0 0	X	X	VDS<1>
1 0 0 1	X	X	VDS<2>
1 0 1 0	X	X	VDS<3>
1 0 1 1	X	X	AGNDN<9>
1 1 0 0	X	X	AGNDN<8>
1 1 0 1	X	X	AGNDN<7>
1 1 1 0	X	X	AGNDN<6>
1 1 1 1	X	X	PB<7>
X 0 0 0	1 0	X	VDS<17>
X 0 0 1	1 1	X	VDS<1>
X 0 1 0	1 0	X	VDS<16>
X 0 1 1	1 1	X	VDS<2>
X 1 0 0	1 0	X	VDS<15>
X 1 0 1	1 1	X	VDS<3>
X 1 1 0	1 0	X	AGNDP<9>
X 1 1 1	1 1	X	AGNDN<9>
X 1 0 0	1 0	X	AGNDP<8>
X 1 0 1	1 1	X	AGNDN<8>
X 1 1 0	1 0	X	AGNDP<7>
X 1 1 1	1 1	X	AGNDN<7>
X 1 0 0	1 0	X	AGNDP<6>
X 1 0 1	1 1	X	AGNDN<6>
X 1 1 0	1 0	X	PB<7>
X 1 1 1	1 1	X	PB<7>

FUVR <3:0>	SMODE <3>	CPO	VREF
0 0 0 0	X	X	VDS<17>
0 0 0 1	X	X	VDS<16>
0 0 1 0	X	X	VDS<15>
0 0 1 1	X	X	AGNDP<9>
0 1 0 0	X	X	AGNDP<8>
0 1 0 1	X	X	AGNDP<7>
0 1 1 0	X	X	AGNDP<6>
0 1 1 1	X	X	AGNDP<0>
1 0 0 0	X	X	VDS<1>
1 0 0 1	X	X	VDS<2>
1 0 1 0	X	X	VDS<3>
1 0 1 1	X	X	AGNDN<9>
1 1 0 0	X	X	AGNDN<8>
1 1 0 1	X	X	AGNDN<7>
1 1 1 0	X	X	AGNDN<6>
1 1 1 1	X	X	PB<7>
X 0 0 0	1 0	X	VDS<17>
X 0 0 1	1 1	X	VDS<1>
X 0 1 0	1 0	X	VDS<16>
X 0 1 1	1 1	X	VDS<2>
X 1 0 0	1 0	X	VDS<15>
X 1 0 1	1 1	X	VDS<3>
X 1 1 0	1 0	X	AGNDP<9>
X 1 1 1	1 1	X	AGNDN<9>
X 1 0 0	1 0	X	AGNDP<8>
X 1 0 1	1 1	X	AGNDN<8>
X 1 1 0	1 0	X	AGNDP<7>
X 1 1 1	1 1	X	AGNDN<7>
X 1 0 0	1 0	X	AGNDP<6>
X 1 0 1	1 1	X	AGNDN<6>
X 1 1 0	1 0	X	PB<7>
X 1 1 1	1 1	X	PB<7>

The schematic diagram illustrates the test setup for the VOLTIOHM CAPIDT module. It features a series of precision resistors (30k, 10M, 1M, 100k, 10k, 1k) and capacitors (5pF, 104) connected to various input pins of the module. The module's internal architecture includes multiple comparators (VREF), multiplexers (MUX), and logic gates (CMPT). A table defines the signal mappings for FUVVR, SMODE, CPO, and VREF.

FUVVR <3:0>	SMODE <3>	CPO	VREF
0 0 0 0	X	X	VDS<17>
0 0 0 1	X	X	VDS<16>
0 0 1 0	X	X	VDS<15>
0 0 1 1	X	X	AGNDP<9>
0 1 0 0	X	X	AGNDP<8>
0 1 0 1	X	X	AGNDP<7>
0 1 1 0	X	X	AGNDP<6>
0 1 1 1	X	X	AGNDP<0>
1 0 0 0	X	X	VDS<1>
1 0 0 1	X	X	VDS<2>
1 0 1 0	X	X	VDS<3>
1 0 1 1	X	X	AGNDN<9>
1 1 0 0	X	X	AGNDN<8>
1 1 0 1	X	X	AGNDN<7>
1 1 1 0	X	X	AGNDN<6>
1 1 1 1	X	X	PB<7>
X 0 0 0	1 0	X	VDS<17>
X 0 0 1	1 1	X	VDS<1>
X 0 1 0	1 0	X	VDS<16>
X 0 1 1	1 1	X	VDS<2>
X 1 0 0	1 0	X	VDS<15>
X 1 0 1	1 1	X	VDS<3>
X 1 1 0	1 0	X	AGNDP<9>
X 1 1 1	1 1	X	AGNDN<9>
X 1 0 0	1 0	X	AGNDP<8>
X 1 0 1	1 1	X	AGNDN<8>
X 1 1 0	1 0	X	AGNDP<7>
X 1 1 1	1 1	X	AGNDN<7>
X 1 0 0	1 0	X	AGNDP<6>
X 1 0 1	1 1	X	AGNDN<6>
X 1 1 0	1 0	X	AGNDP<0>
X 1 1 1	1 1	X	PB<7>

Main function of Chopper is to reduce DC Offset.



4. ACV

30K Ω resistor and 5pF capacitor of the input end is to compensate ACV frequency. When a part of ranges are not in use, it is recommended to connect to ground and its input divider of voltage range is shown in below equation :

$$5V_Range \Rightarrow V_{IN} \times \frac{1.111M\Omega}{10M\Omega + 1.111M\Omega} = \frac{V_{IN}}{10}$$

$$50V_Range \Rightarrow V_{IN} \times \frac{101.01K\Omega}{10M\Omega + 101.01K\Omega} = \frac{V_{IN}}{100}$$

$$500V_Range \Rightarrow V_{IN} \times \frac{10.01K\Omega}{10M\Omega + 10.01K\Omega} = \frac{V_{IN}}{1000}$$

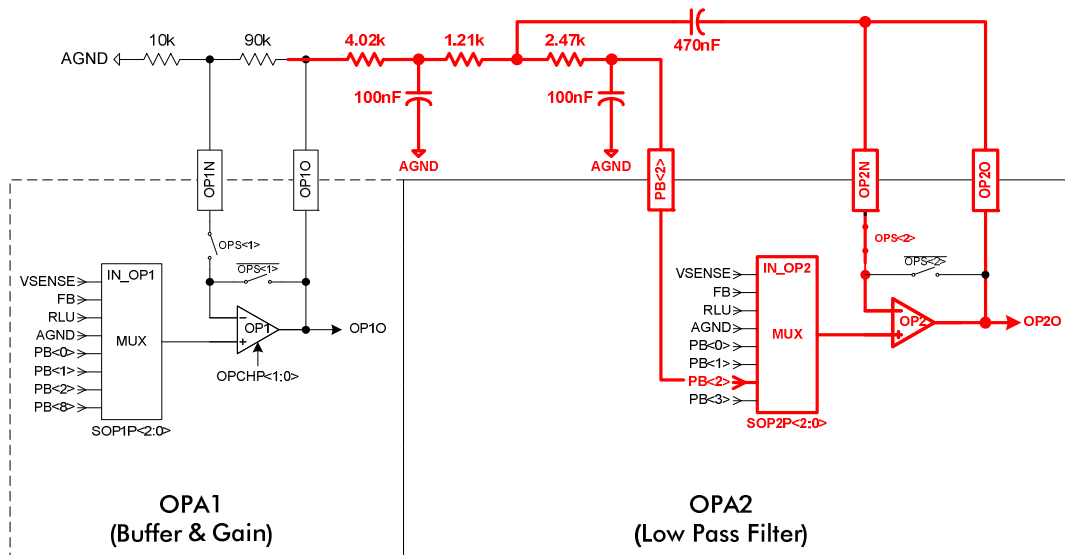
$$1000V_Range \Rightarrow V_{IN} \times \frac{1K\Omega}{10M\Omega + 1K\Omega} = \frac{V_{IN}}{10000}$$

HY313x has two sets OPA that can be used to amplify 10 times of signal, realizing 500mV measurement by collocating with 5V network configurations.

Digital ACV bandwidth compensation capacitor equation is as follows :

$$Capacitor\ array = \sum_{n=0}^6 ACC < n > \times 2^n \times 0.2\ pF$$

4.1. AC Low Pass Filter Measurement Network Configuration



The schematic diagram illustrates the VREF and CPO circuit. It features a capacitor array (ACC<6:0>) connected to a VREF input. The circuit includes a VREF block with a table of inputs and outputs, and a CPO block with a table of inputs and outputs. The output of the CPO block is connected to a VREF input of another block. The diagram also shows a VREF input connected to a VREF block, and a CPO input connected to a CPO block. The output of the CPO block is connected to a VREF input of another block. The diagram also shows a VREF input connected to a VREF block, and a CPO input connected to a CPO block. The output of the CPO block is connected to a VREF input of another block.

FUVR <3:0>	SMODE <3>	CPO	VREF
0 0 0 0	X	0	VDS<17>
0 0 0 1	X	0	VDS<16>
0 0 1 0	X	0	VDS<15>
0 0 1 1	X	0	AGNDP<9>
0 1 0 0	X	0	AGNDP<8>
0 1 0 1	X	0	AGNDP<7>
0 1 1 0	X	0	AGNDP<6>
0 1 1 1	X	0	AGNDP<0>
1 0 0 0	X	0	VDS<1>
1 0 0 1	X	0	VDS<2>
1 0 1 0	X	0	VDS<3>
1 0 1 1	X	0	AGNDN<9>
1 1 0 0	X	0	AGNDN<8>
1 1 0 1	X	0	AGNDN<7>
1 1 1 0	X	0	AGNDN<6>
1 1 1 1	X	0	PB<7>
X 0 0 0	1	0	VDS<17>
X 0 0 1	1	0	VDS<16>
X 0 1 0	1	0	VDS<15>
X 0 1 1	1	0	AGNDP<9>
X 1 0 0	1	0	AGNDP<8>
X 1 0 1	1	0	AGNDP<7>
X 1 1 0	1	0	AGNDP<6>
X 1 1 1	1	0	AGNDP<0>
X 0 0 0	1	1	VDS<1>
X 0 0 1	1	1	VDS<2>
X 0 1 0	1	1	VDS<3>
X 0 1 1	1	1	AGNDN<9>
X 1 0 0	1	1	AGNDN<8>
X 1 0 1	1	1	AGNDN<7>
X 1 1 0	1	1	AGNDN<6>
X 1 1 1	1	1	PB<7>

The diagram illustrates the VOLT_OHM_CAP_IDT circuit, which is a multi-range input circuit. It features a series of resistors and capacitors that allow for a wide range of input values. The circuit is controlled by a microcontroller (MCU) through a series of pins (FUV, SMODE, CPO). The output of the circuit is a 12-bit digital value (CPO) that represents the input voltage or resistance.

The circuit includes a capacitor array, a resistor ladder, and a feedback network. The input range is determined by the value of the input resistor (R_{IN}). The output is a 12-bit digital value (CPO) that represents the input voltage or resistance.

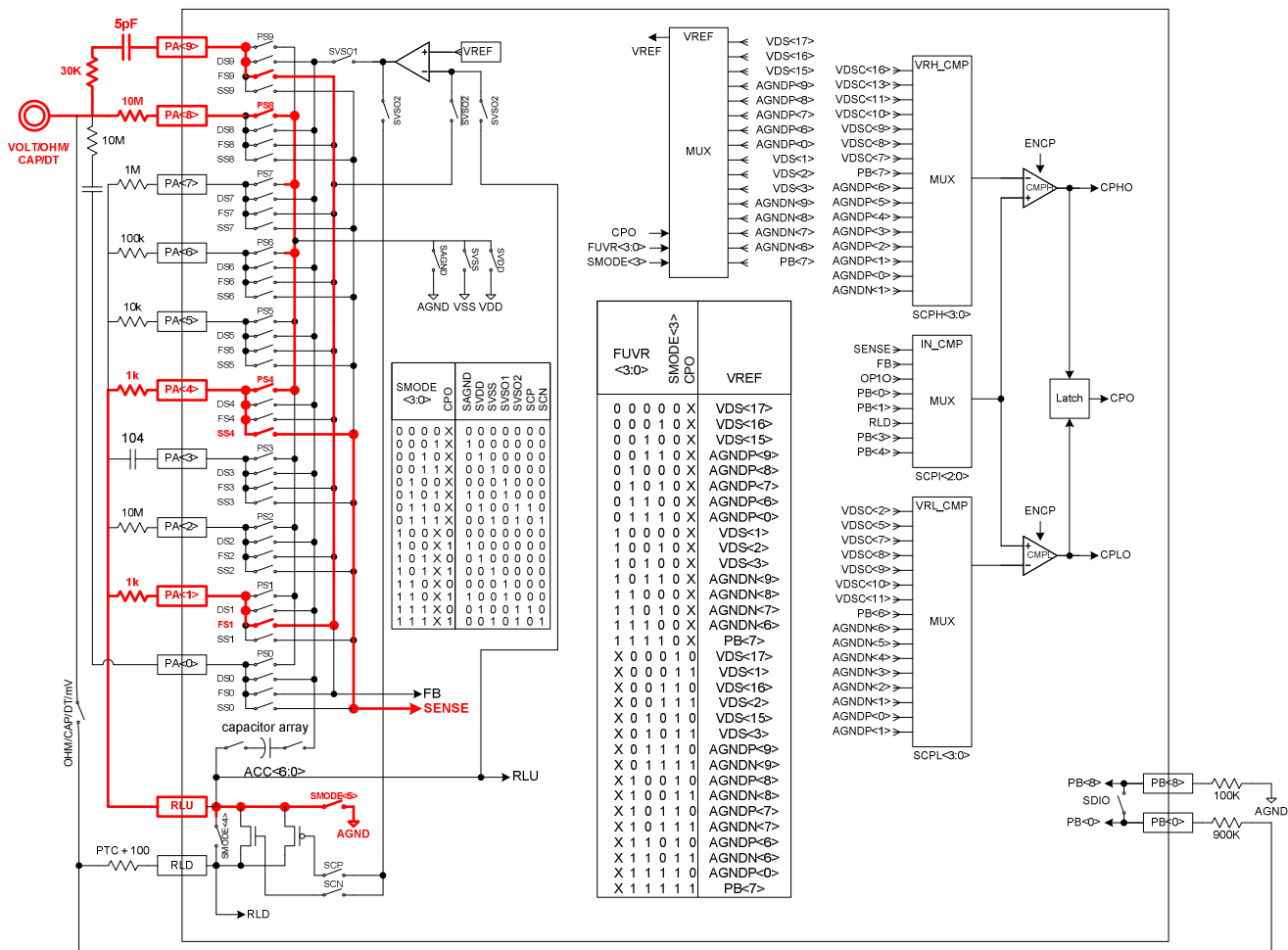
The table below shows the bit patterns for FUV, SMODE, and CPO for each input range.

FUV	SMODE	CPO	VREF		
0	0	0	0	X	VDS<17>
0	0	0	1	X	VDS<16>
0	0	1	0	X	VDS<15>
0	0	1	1	X	AGNDP<9>
0	0	1	1	0	AGNDP<8>
0	1	0	1	X	AGNDP<7>
0	1	1	0	X	AGNDP<6>
0	1	1	1	0	AGNDP<5>
0	1	1	1	1	VDS<1>
1	0	0	1	X	VDS<2>
1	0	1	0	X	VDS<3>
1	0	1	1	0	AGNDN<9>
1	1	0	1	X	AGNDN<8>
1	1	1	0	X	AGNDN<7>
1	1	1	1	0	AGNDN<6>
1	1	1	1	1	PB<7>
X	0	0	0	1	VDS<17>
X	0	0	0	1	VDS<16>
X	0	0	1	1	VDS<15>
X	0	0	1	1	AGNDN<9>
X	0	1	0	1	AGNDP<8>
X	0	1	1	0	AGNDP<7>
X	0	1	1	1	AGNDP<6>
X	1	0	1	1	AGNDN<9>
X	1	0	1	1	AGNDN<8>
X	1	1	0	1	AGNDN<7>
X	1	1	1	0	AGNDN<6>
X	1	1	1	1	PB<7>

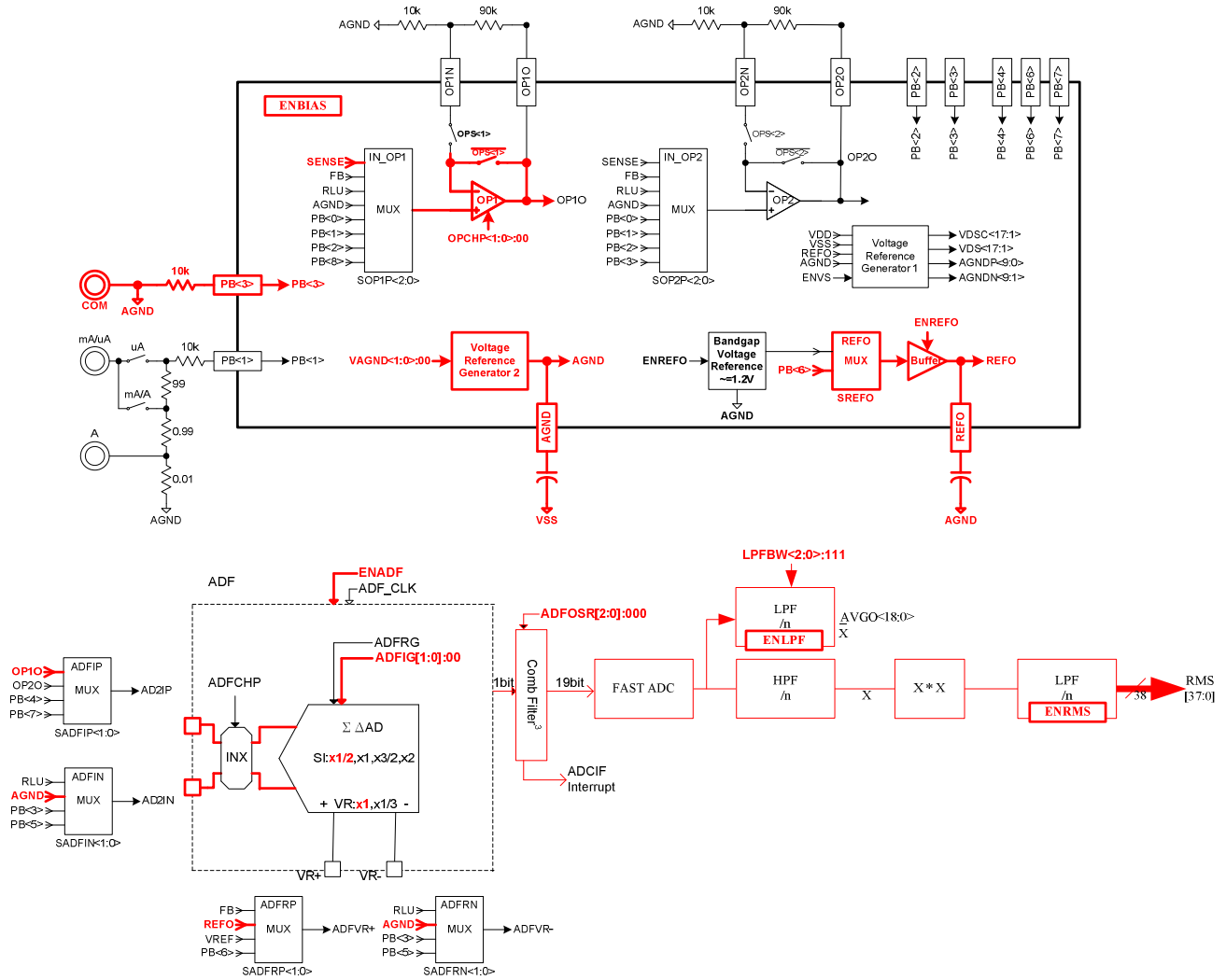
The schematic diagram illustrates the VOLTIOHM CAPIDT module, which is designed for precise voltage and current measurements. It features a series of input channels (PA<0> to PA<15>) connected to a capacitor array. The circuit includes a VREF block, a MUX, and various control signals like SENSE, FB, and RLU. A table of control signals (FUVVR, SMODE, CPO, VREF) is provided. The output is connected to a Latch and a CPO signal.

FUVVR <3:0>	SMODE <3>	CPO	VREF
0 0 0 0	X	X	VDS<17>
0 0 0 1	X	X	VDS<16>
0 0 1 0	X	X	VDS<15>
0 0 1 1	X	X	AGNDP<9>
0 1 0 0	X	X	AGNDP<8>
0 1 0 1	X	X	AGNDP<7>
0 1 1 0	X	X	AGNDP<6>
0 1 1 1	X	X	AGNDP<0>
1 0 0 0	X	X	VDS<1>
1 0 0 1	X	X	VDS<2>
1 0 1 0	X	X	VDS<3>
1 0 1 1	X	X	AGNDN<9>
1 1 0 0	X	X	AGNDN<8>
1 1 0 1	X	X	AGNDN<7>
1 1 1 0	X	X	AGNDN<6>
1 1 1 1	X	X	PB<7>
X 0 0 0	1 0	X	VDS<17>
X 0 0 1	1 1	X	VDS<1>
X 0 1 0	1 0	X	VDS<16>
X 0 1 1	1 1	X	VDS<2>
X 1 0 0	1 0	X	VDS<15>
X 1 0 1	1 1	X	VDS<3>
X 1 1 0	1 0	X	AGNDP<9>
X 1 1 1	1 1	X	AGNDN<9>
X 1 0 0	1 0	X	AGNDP<8>
X 1 0 1	1 1	X	AGNDN<8>
X 1 1 0	1 0	X	AGNDP<7>
X 1 1 1	1 1	X	AGNDN<7>
X 1 0 0	1 0	X	AGNDP<6>
X 1 0 1	1 1	X	AGNDN<6>
X 1 1 0	1 0	X	AGNDP<0>
X 1 1 1	1 1	X	PB<7>

4.5. 1000V Input Network Configuration

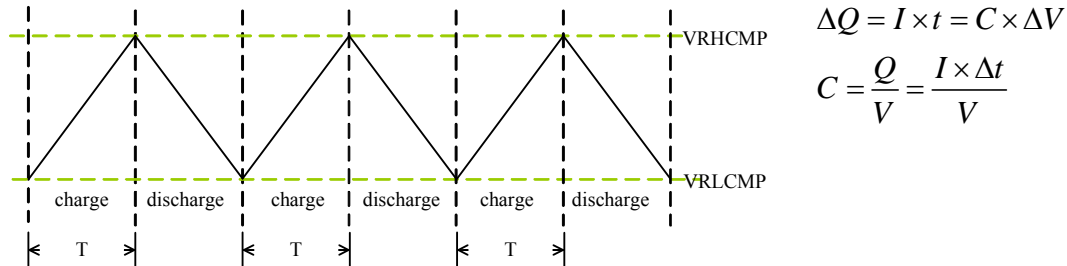


4.6. AC5V~1000V Measurement Network Configuration



5. Capacitor

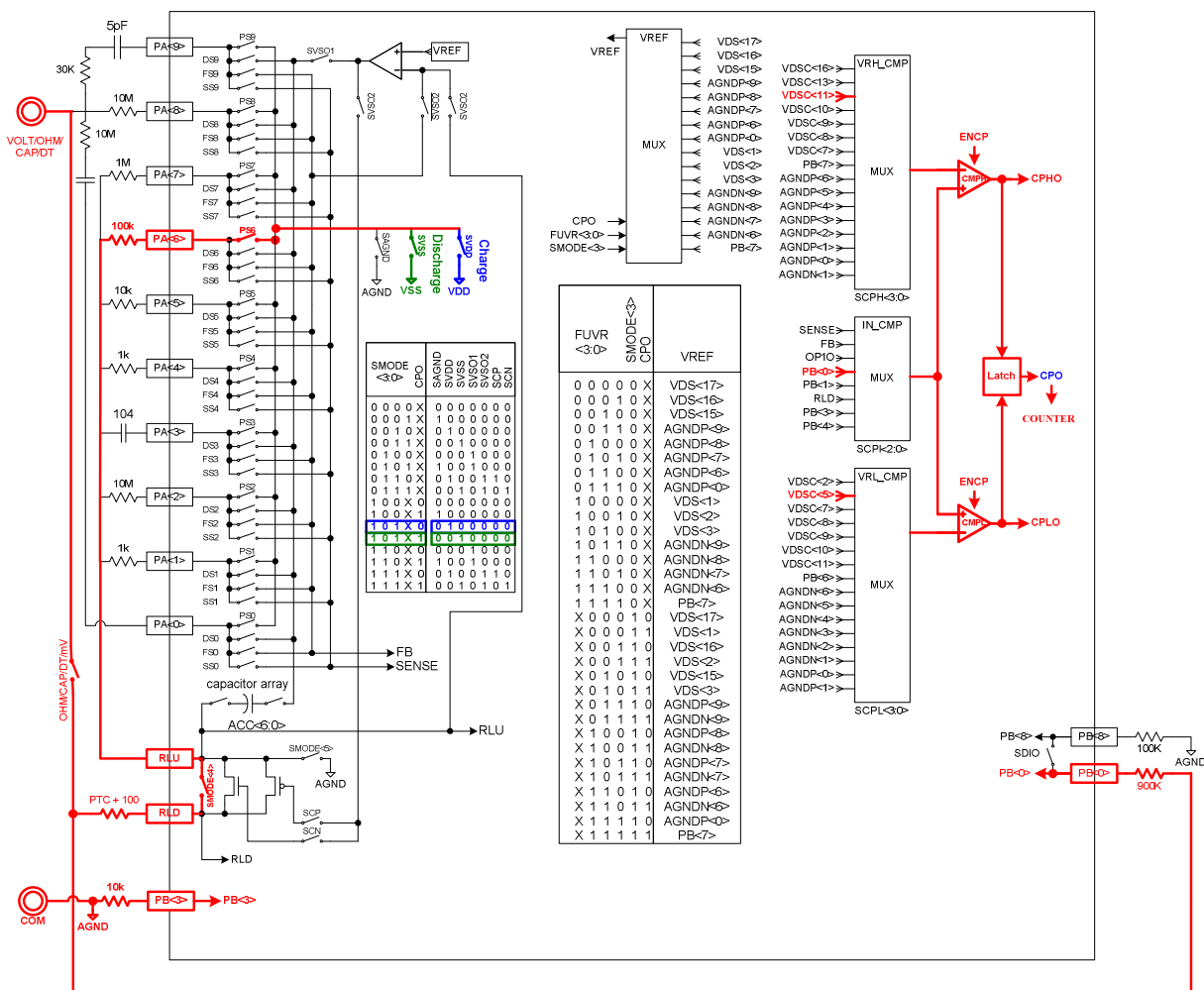
There are two ways to measure capacitor, constant voltage and constant current output mode. Under low capacitor ($<1 \mu F$), users need to use constant voltage output mode for testing whereas using constant current output mode to test high capacitor ($>1 \mu F$). Capacitor measurement uses charge/discharge test cycle to gain the value.



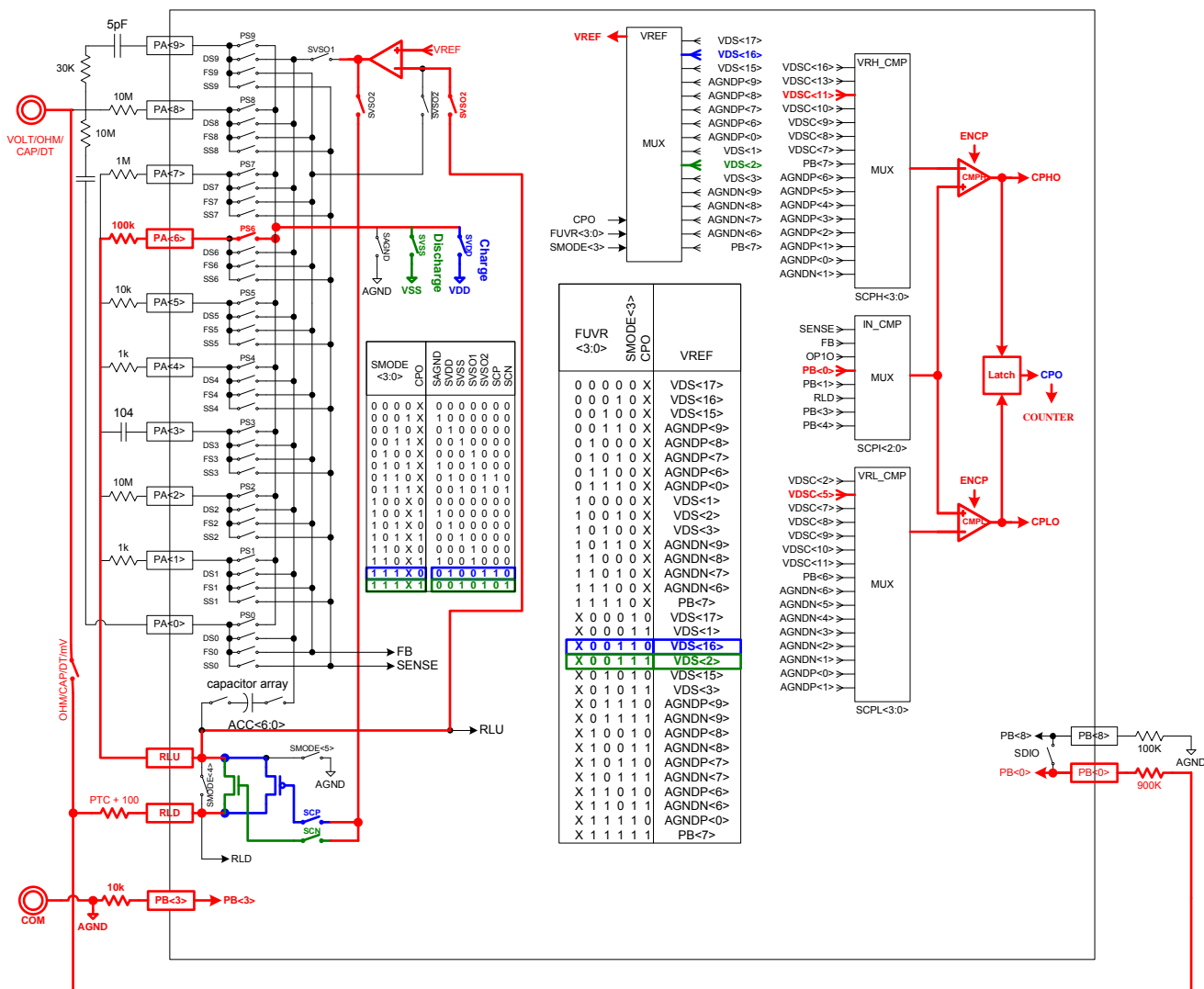
Capacitor measurement test procedure :

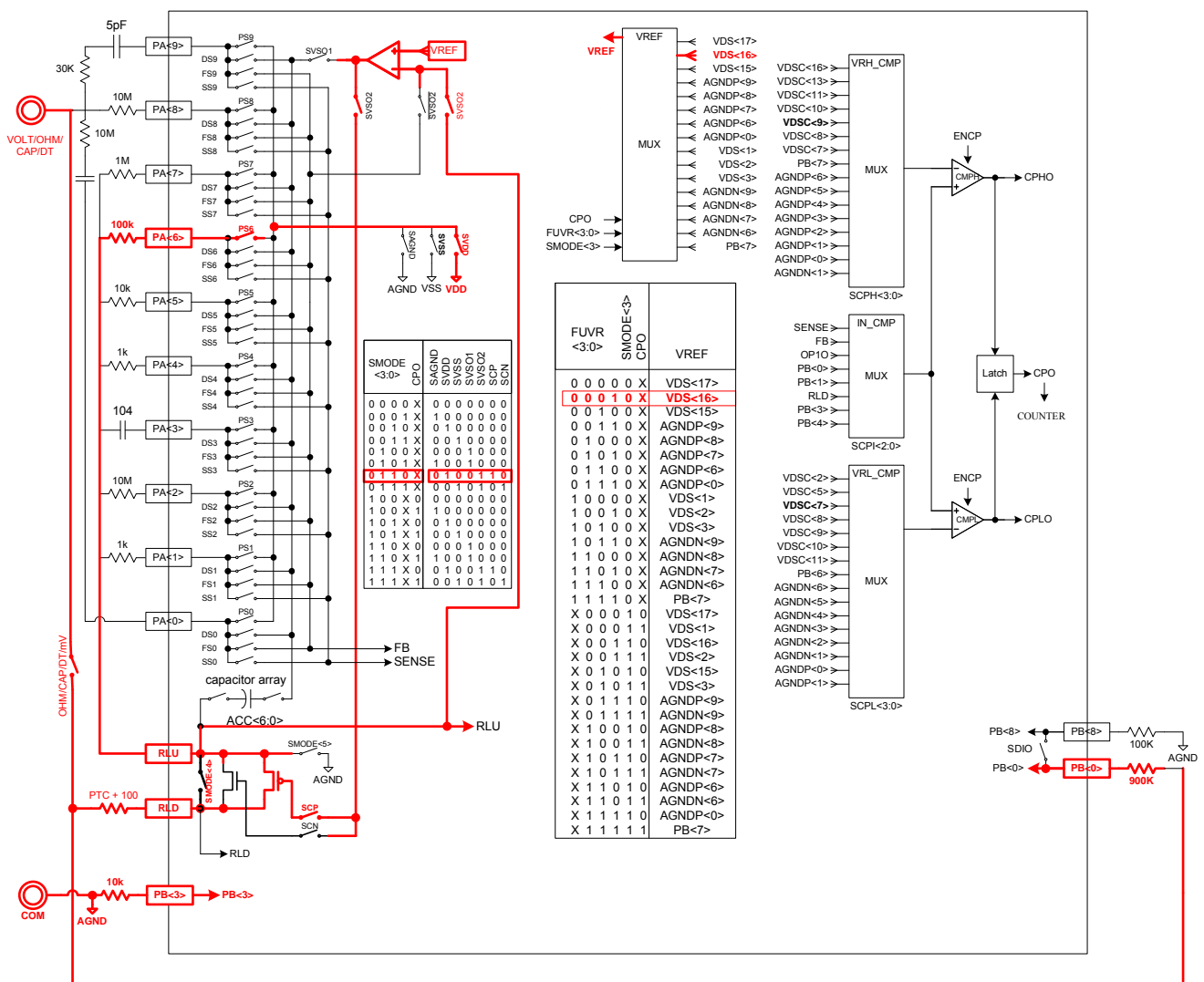
1. Select constant voltage (SMODE<7:0>=01110b) and constant current (SMODE<7:0>=11010b) test mode output.
2. Configure capacitor charge/discharge comparison voltage (VRHCMP 、VRLCMP) and the actual charge/discharge of capacitor is decided by comparator, ACPO.
3. Configure CTA<23:8> initial value of Frequency Counter. When INTF2 register, CTF bit is 1, CTC<23:0> divided by CTB<23:0> to gain the cycle length.

5.1. 50-500nF (Constant Voltage Charge/Discharge Measurement)

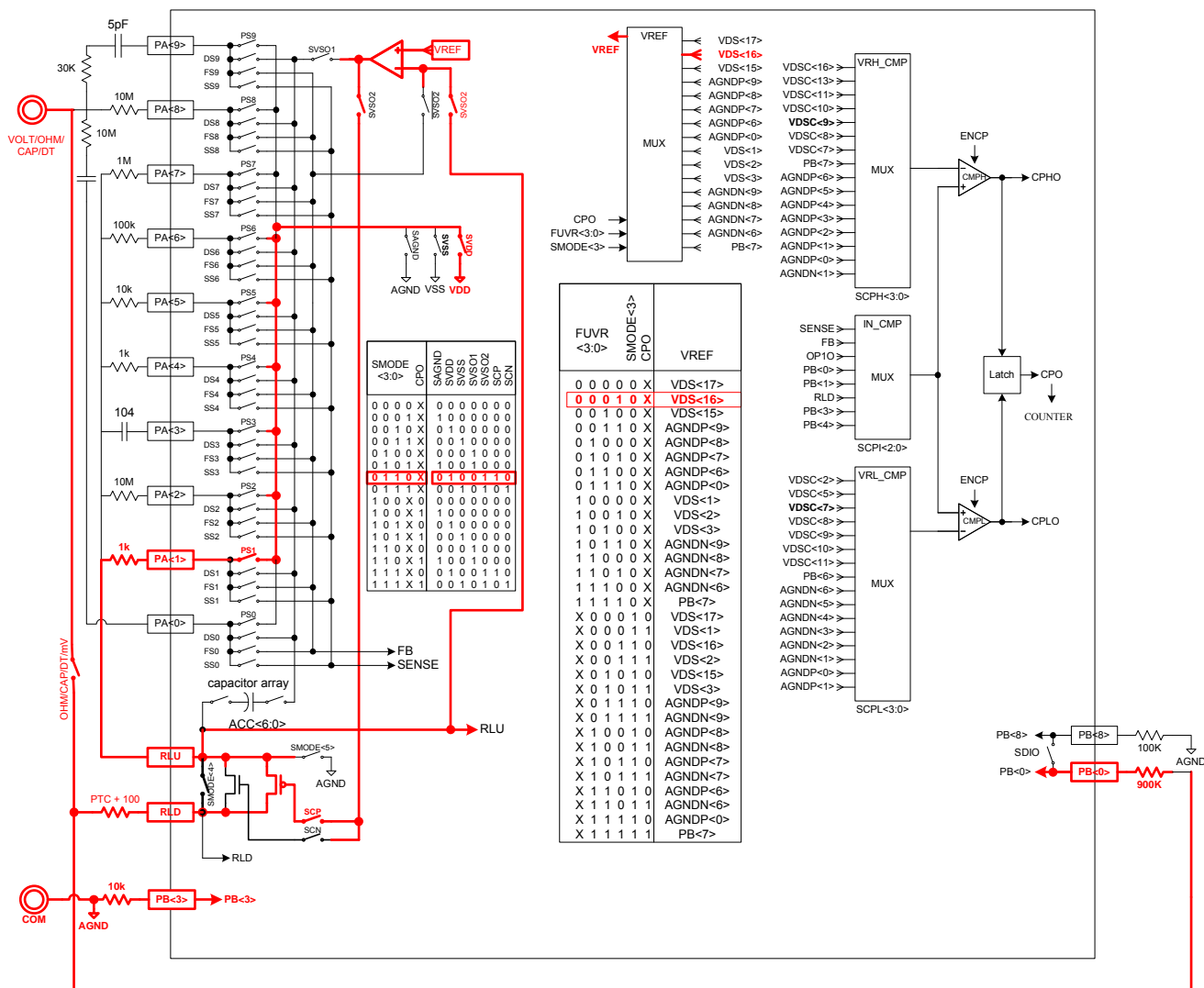


5.2. 5uF-50uF (Constant Current Charge/Discharge Measurement)



$$C = \frac{Q}{V} = I \times \frac{\Delta t}{\Delta V}$$


5.4. 5mF-50mF(Charge)



The schematic diagram illustrates the ENBIAS module, which consists of two main channels, OP1 and OP2, each featuring a multiplexer (MUX), an operational amplifier (OP), and various reference generators.

Channel OP1:

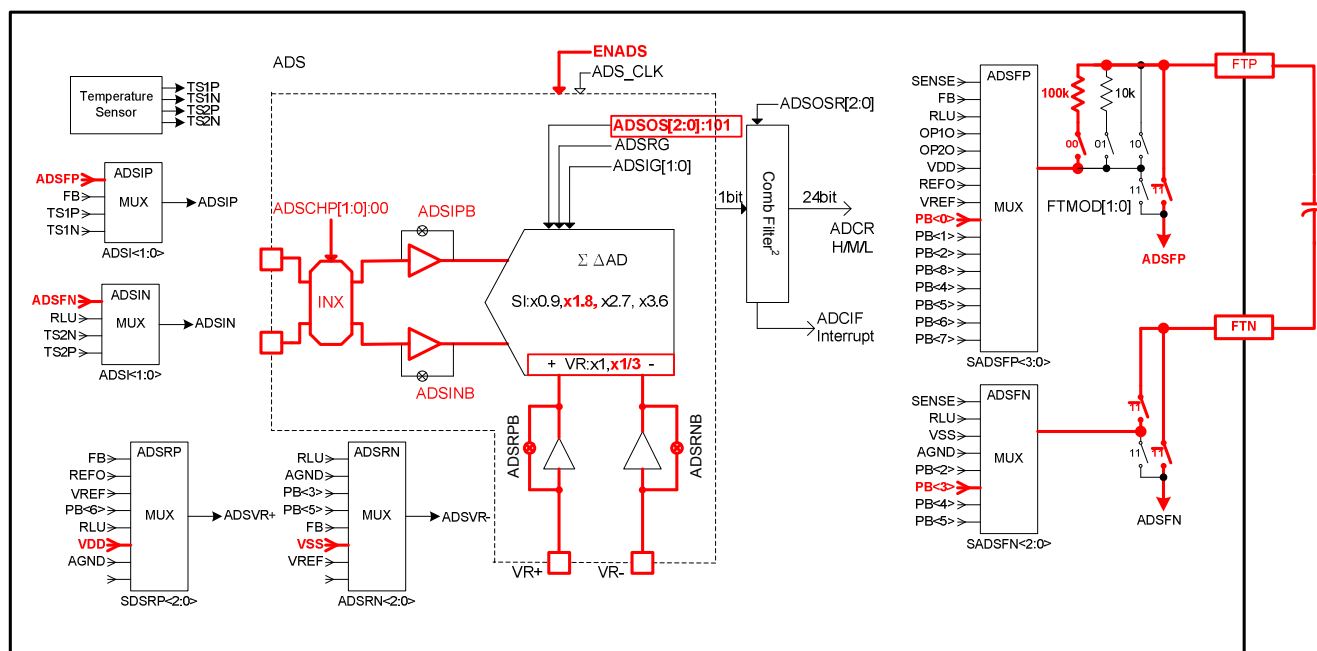
- MUX:** Selects between SENSE, FB, RLU, AGND, PB<0>, PB<1>, PB<2>, and PB<6> for the IN_OP1 input.
- OP1:** An operational amplifier with feedback (FB) and output (OP10). It is configured with a gain of 10 (OPCHP<1.0>:1.0).
- Reference Generators:**
 - Voltage Reference Generator 2:** Provides a reference voltage (VAGND<1.0>:0.1) to the AGND input of OP1.
 - Bandgap Voltage Reference (~1.2V):** Provides a reference voltage (ENREFO) to the REFO input of OP1.
 - REFO MUX:** Selects between SREFO and ENREFO for the REFO input of OP1.
 - Buffer:** Buffers the REFO signal to the REFO output.

Channel OP2:

- MUX:** Selects between SENSE, FB, RLU, AGND, PB<0>, PB<1>, PB<2>, and PB<6> for the IN_OP2 input.
- OP2:** An operational amplifier with feedback (FB) and output (OP20). It is configured with a gain of 10 (OPCHP<1.0>:1.0).
- Reference Generators:**
 - Voltage Reference Generator 1:** Provides a reference voltage (VDS<17.1>) to the AGND input of OP2.
 - Bandgap Voltage Reference (~1.2V):** Provides a reference voltage (ENREFO) to the REFO input of OP2.
 - REFO MUX:** Selects between SREFO and ENREFO for the REFO input of OP2.
 - Buffer:** Buffers the REFO signal to the REFO output.

ENBIAS Module:

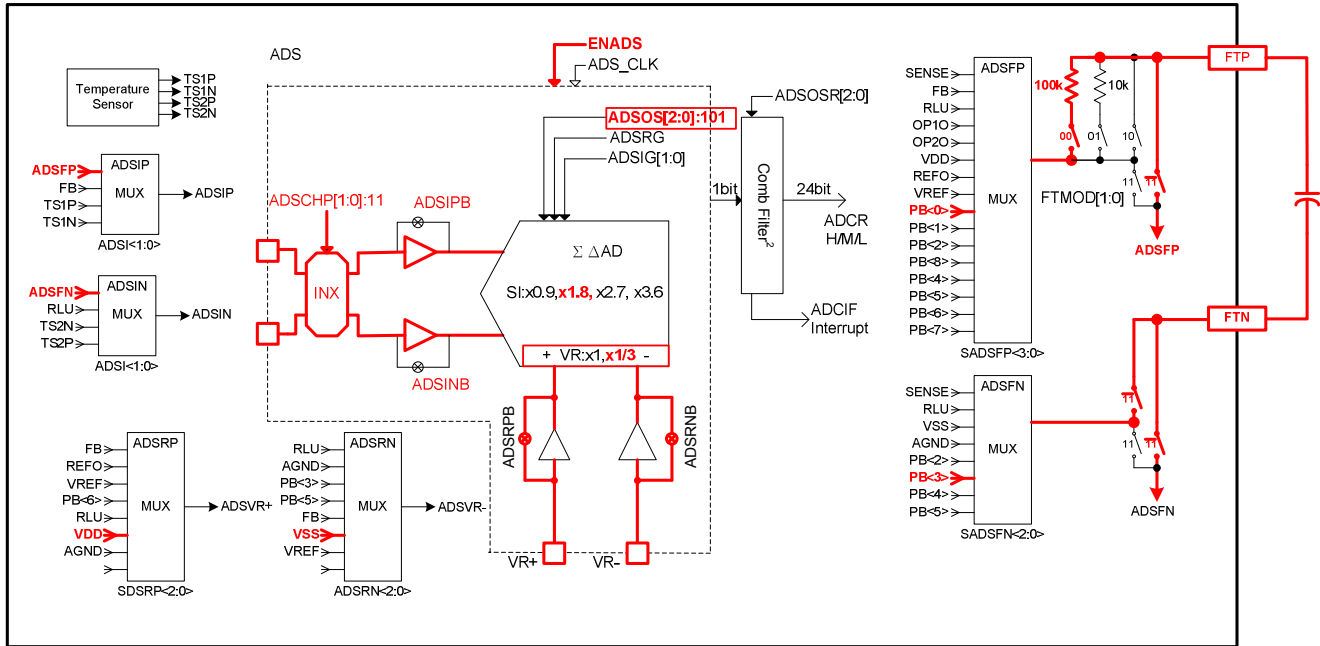
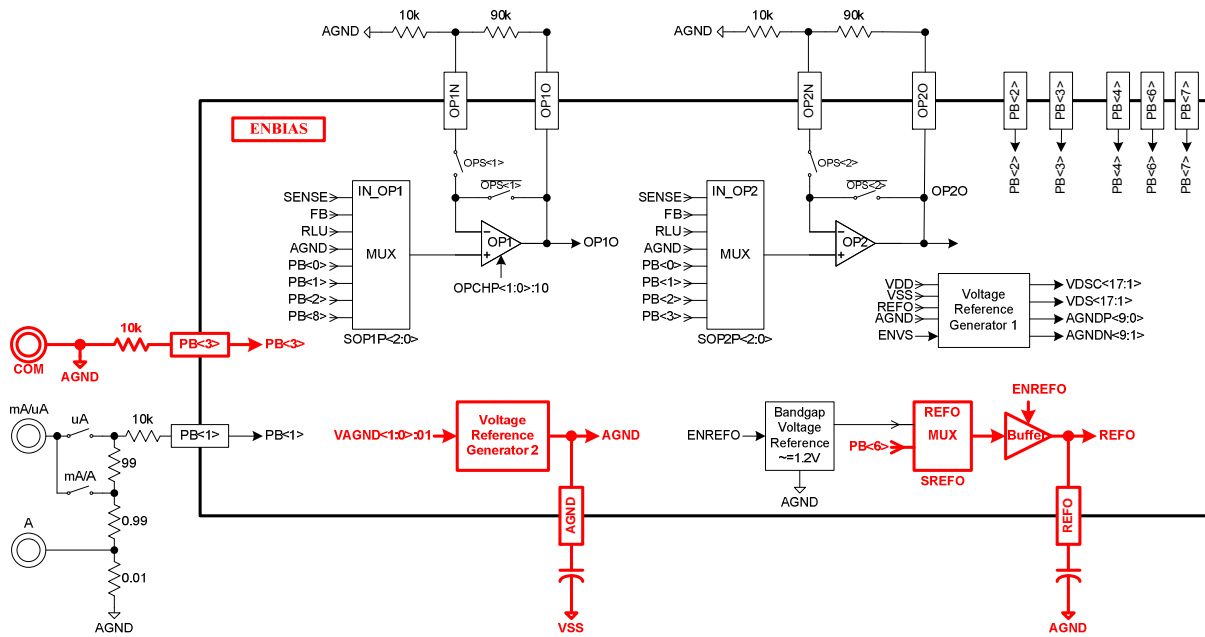
- ENBIAS:** A control signal that enables the module.
- AGND:** Analog Ground, connected to the AGND inputs of both channels.
- REFO:** Reference Output, connected to the REFO inputs of both channels.
- OP10 and OP20:** The outputs of the operational amplifiers.
- PB<0> to PB<7>:** Port Bits, used for selecting inputs and outputs.



The schematic diagram illustrates the VREF and CPO circuit. It includes a voltage divider network for VREF, a capacitor array, and a CPO circuit with a latch. The truth table for the CPO circuit is as follows:

FUVR <3:0>	SMODE<3> CPO	VREF
0 0 0 0	X	VDS<17>
0 0 0 1	X	VDS<16>
0 0 1 0	X	VDS<15>
0 0 1 1	X	AGNDP<9>
0 1 0 0	X	AGNDP<8>
0 1 0 1	X	AGNDP<7>
0 1 1 0	X	AGNDP<6>
0 1 1 1	X	AGNDP<5>
1 0 0 0	X	AGNDP<4>
1 0 0 1	X	AGNDP<3>
1 0 1 0	X	AGNDP<2>
1 0 1 1	X	AGNDP<1>
1 1 0 0	X	AGNDP<0>
1 1 0 1	X	AGNDN<9>
1 1 0 1	X	AGNDN<8>
1 1 0 1	X	AGNDN<7>
1 1 1 0	X	AGNDN<6>
1 1 1 1	X	PB<7>
X 0 0 0	10	VDS<17>
X 0 0 1	11	VDS<16>
X 0 1 0	10	VDS<15>
X 0 1 1	10	AGNDP<9>
X 1 0 0	11	AGNDP<8>
X 1 0 1	11	AGNDP<7>
X 1 0 1	11	AGNDP<6>
X 1 0 1	11	AGNDP<5>
X 1 1 0	11	AGNDP<4>
X 1 1 0	11	AGNDP<3>
X 1 1 0	11	AGNDP<2>
X 1 1 0	11	AGNDP<1>
X 1 1 0	11	AGNDP<0>
X 1 1 1	11	PB<7>

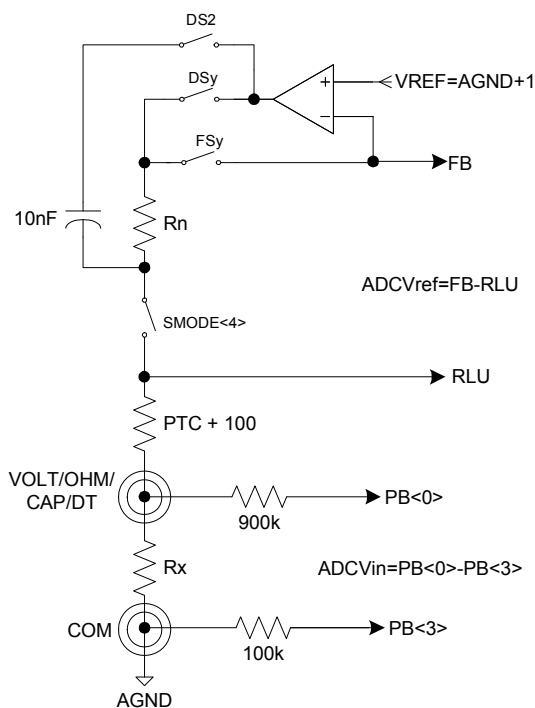
HY313X Configurations



6. Resistor

The chip offers two ways to measure resistor, constant voltage and constant current measurement and different methods lead to diverse results.

Constant voltage or ratio resistor measurement design must input ADC signal and open reference voltage input buffer when measuring high resistor. 3MΩ parallel connection impedance will be generated if ADC input was not opened. It is suggested to use constant current resistor measurement when design 500kΩ to 50MΩ application. The measurement equation is given below :

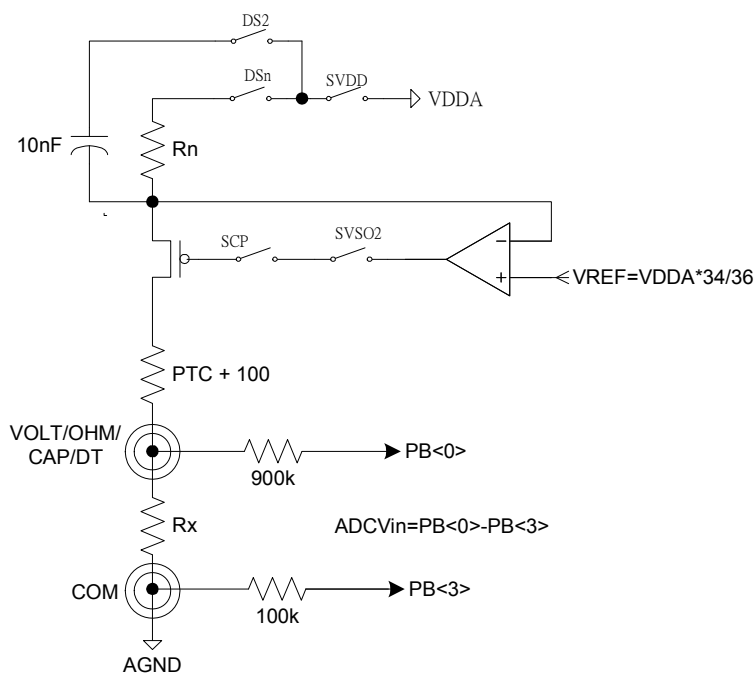


$$I_{Rx} = I_{Rn}$$

$$V_{Rx} = I_{Rx} \times Rx = \frac{V_{Rn}}{Rn} \times Rx$$

$$R_{READ} = \frac{V_{Rx}}{V_{Rn}} \times Full\ Scale = \frac{ADCV_{in}}{ADCV_{ref}} \times Full\ Scale$$

Constant current resistor measurement design has higher internal impedance of DS_n and SVDD electrical switches; it will have parallel connection with R_n resistor and to cause output current deviation. It is recommended to use constant voltage resistor measurement when designing 500kΩ or below applications. The measurement equation is given below :



$$I_{Rx} = I_{Rn} = \frac{VDDA - VREF}{Rn}$$

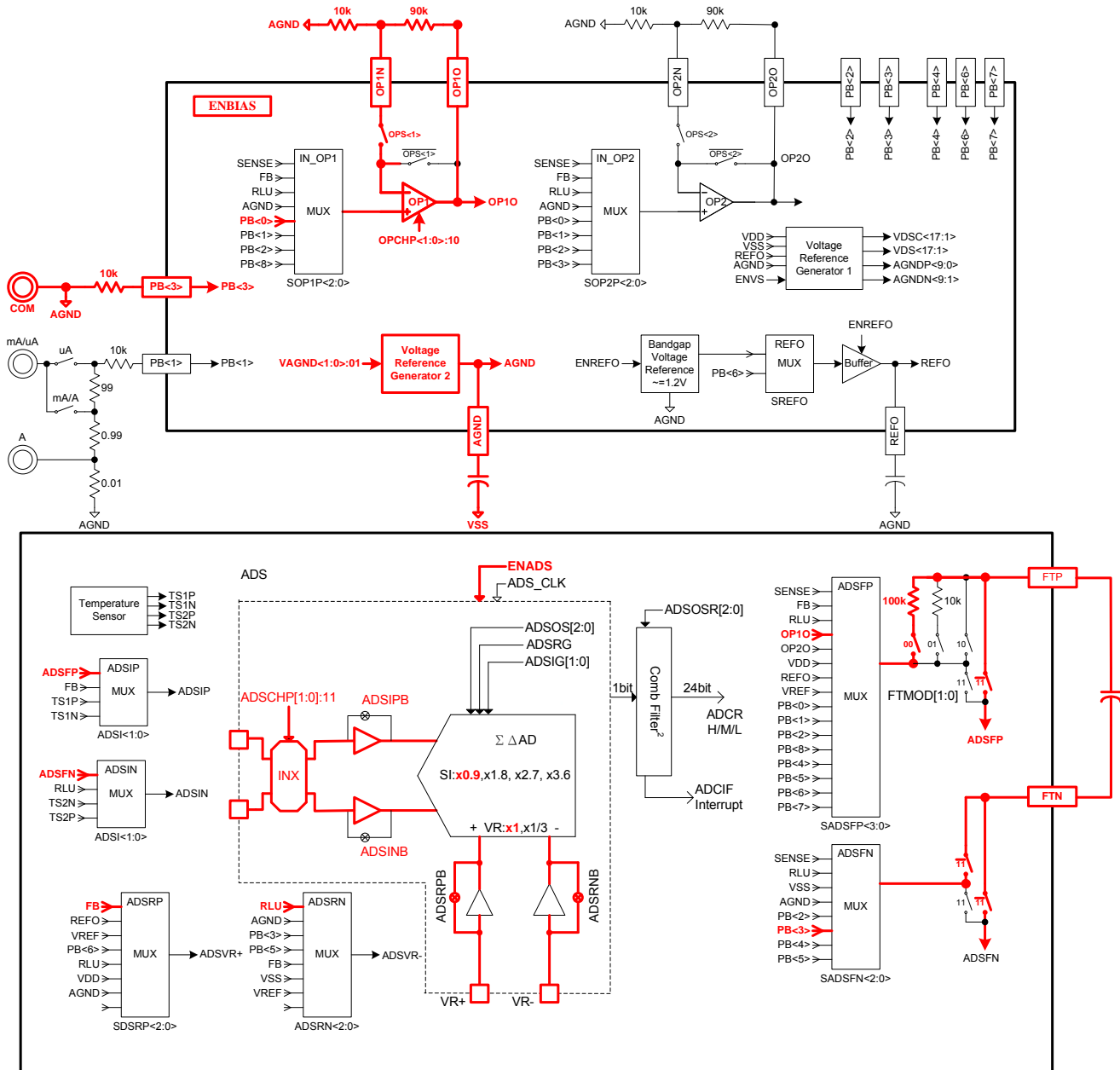
$$R_{READ} = \frac{ADCV_{in}}{ADCV_{ref}} \times Full\ Scale$$

$$R_{READ} = \frac{Rx \times I_{Rx}}{ADCV_{ref}} \times Full\ Scale$$

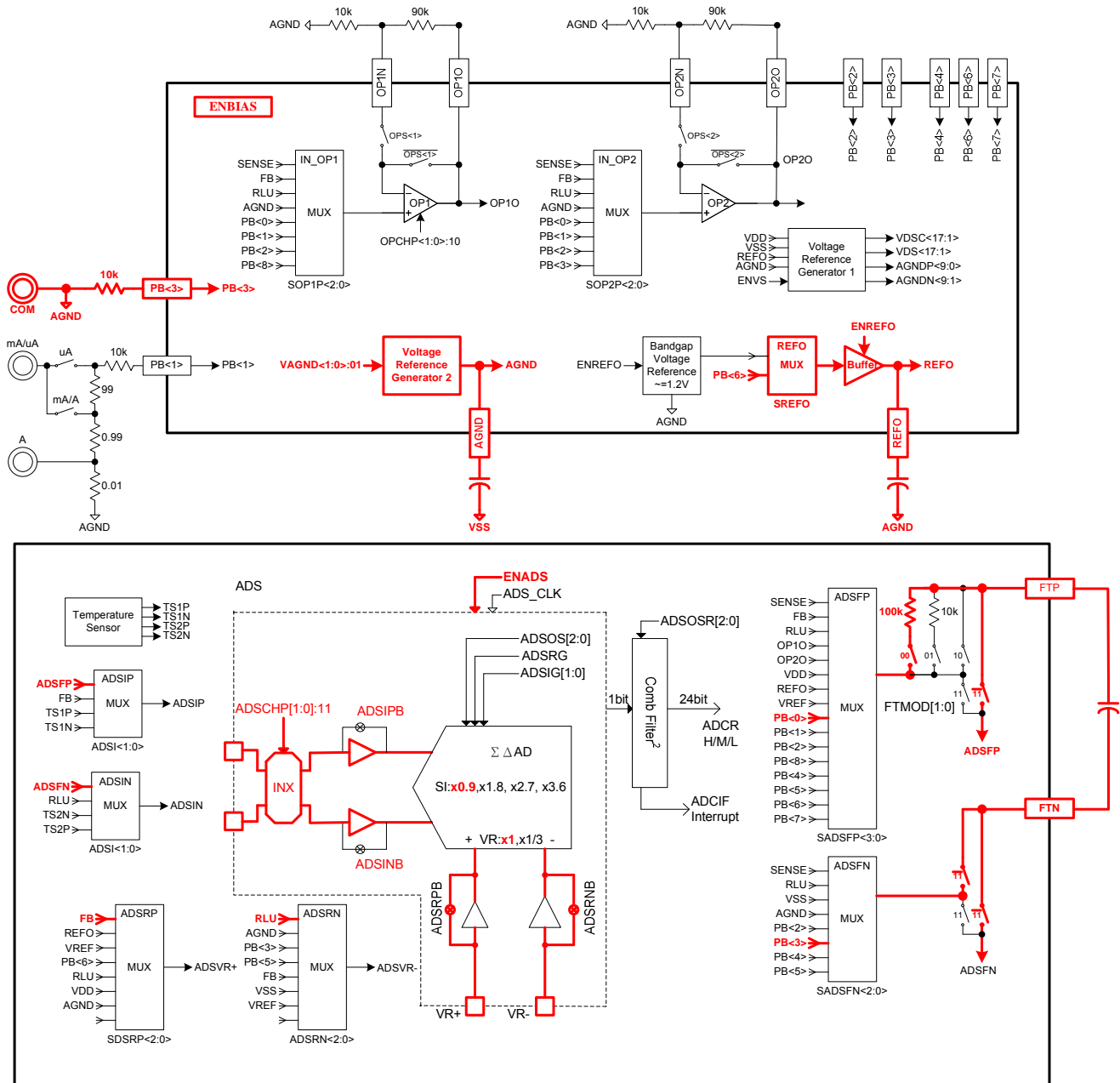
[illegible]

[illegible]

6.3. 50ohm Measurement Network Configuration



6.4. 500 ohm~50K ohm Measurement Network Configuration

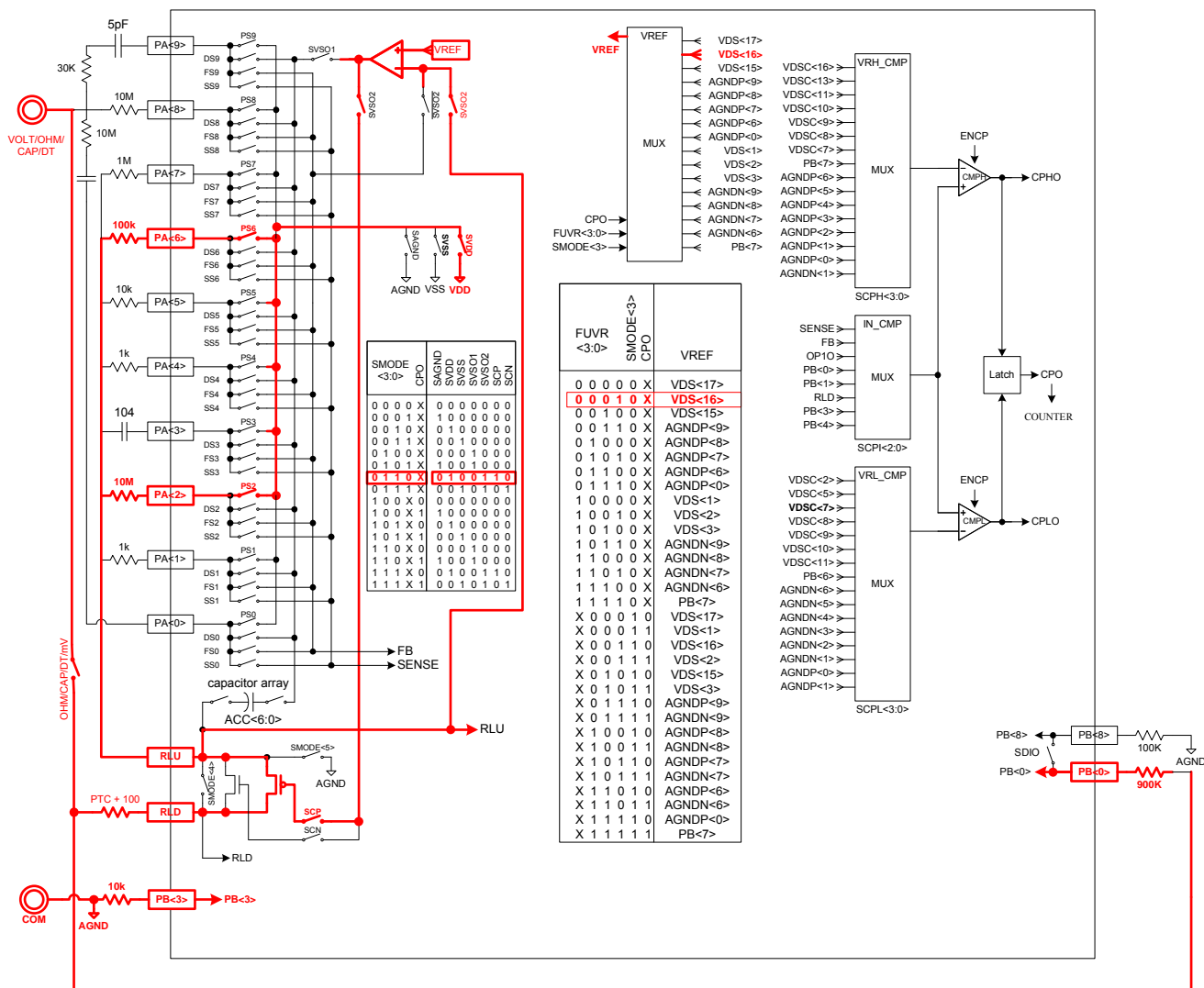


The schematic diagram illustrates the internal circuitry of the VREF and CPO pins. It features a voltage divider network for VREF, a capacitor array for CPO, and a feedback loop for the op-amp. The VREF circuit includes a 30k resistor, a 5pF capacitor, and a 10M resistor. The CPO circuit includes a 10k resistor, a 100k resistor, and a 104 capacitor. The feedback loop includes a 10k resistor, a 100k resistor, and a 104 capacitor. The op-amp is configured as a voltage follower. The schematic also shows the connection of the VREF and CPO pins to the op-amp. The VREF pin is connected to the non-inverting input of the op-amp. The CPO pin is connected to the inverting input of the op-amp. The op-amp output is connected to the CPO pin. The schematic also shows the connection of the VREF and CPO pins to the op-amp. The VREF pin is connected to the non-inverting input of the op-amp. The CPO pin is connected to the inverting input of the op-amp. The op-amp output is connected to the CPO pin.

Table 1: VREF and CPO Pin Configurations

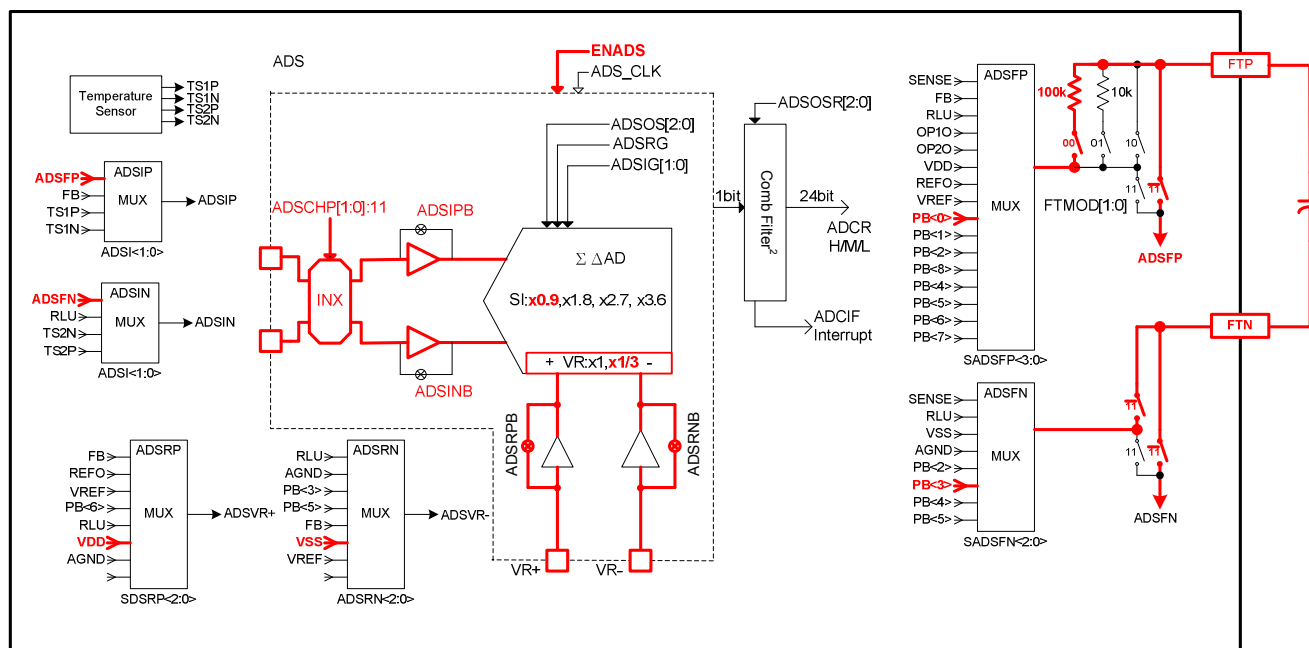
FUVR <3:0>	CPO	VREF
0 0 0 0 X	X	VDS<17>
0 0 0 1 X	X	VDS<16>
0 0 1 0 X	X	VDS<15>
0 0 1 1 0 X	X	AGNDP<9>
0 1 0 0 X	X	AGNDP<8>
0 1 0 1 X	X	AGNDP<7>
0 1 1 0 X	X	AGNDP<6>
0 1 1 1 X	X	AGNDP<5>
1 0 0 0 X	X	VDS<1>
1 0 0 1 X	X	VDS<2>
1 0 1 0 X	X	VDS<3>
1 0 1 1 X	X	AGNDN<9>
1 1 0 0 X	X	AGNDN<8>
1 1 0 1 X	X	AGNDN<7>
1 1 1 0 X	X	AGNDN<6>
1 1 1 1 X	X	PB<7>
X 0 0 0 1	X	VDS<17>
X 0 0 0 1	X	VDS<16>
X 0 0 1 0	X	VDS<15>
X 0 0 1 1	X	VDS<14>
X 0 1 0 0	X	VDS<13>
X 0 1 0 1	X	VDS<12>
X 0 1 1 0	X	VDS<11>
X 0 1 1 1	X	VDS<10>
X 1 0 0 0	X	VDS<9>
X 1 0 0 1	X	VDS<8>
X 1 0 1 0	X	VDS<7>
X 1 0 1 1	X	VDS<6>
X 1 1 0 0	X	VDS<5>
X 1 1 0 1	X	VDS<4>
X 1 1 1 0	X	VDS<3>
X 1 1 1 1	X	VDS<2>
X 1 1 1 1	X	VDS<1>
X 1 1 1 1	X	VDS<0>
X 1 1 1 1	X	VDS<-1>
X 1 1 1 1	X	VDS<-2>
X 1 1 1 1	X	VDS<-3>
X 1 1 1 1	X	VDS<-4>
X 1 1 1 1	X	VDS<-5>
X 1 1 1 1	X	VDS<-6>
X 1 1 1 1	X	VDS<-7>
X 1 1 1 1	X	VDS<-8>
X 1 1 1 1	X	VDS<-9>
X 1 1 1 1	X	VDS<-10>
X 1 1 1 1	X	VDS<-11>
X 1 1 1 1	X	VDS<-12>
X 1 1 1 1	X	VDS<-13>
X 1 1 1 1	X	VDS<-14>
X 1 1 1 1	X	VDS<-15>
X 1 1 1 1	X	VDS<-16>
X 1 1 1 1	X	VDS<-17>

6.6. 500Kohm Input Network Configuration

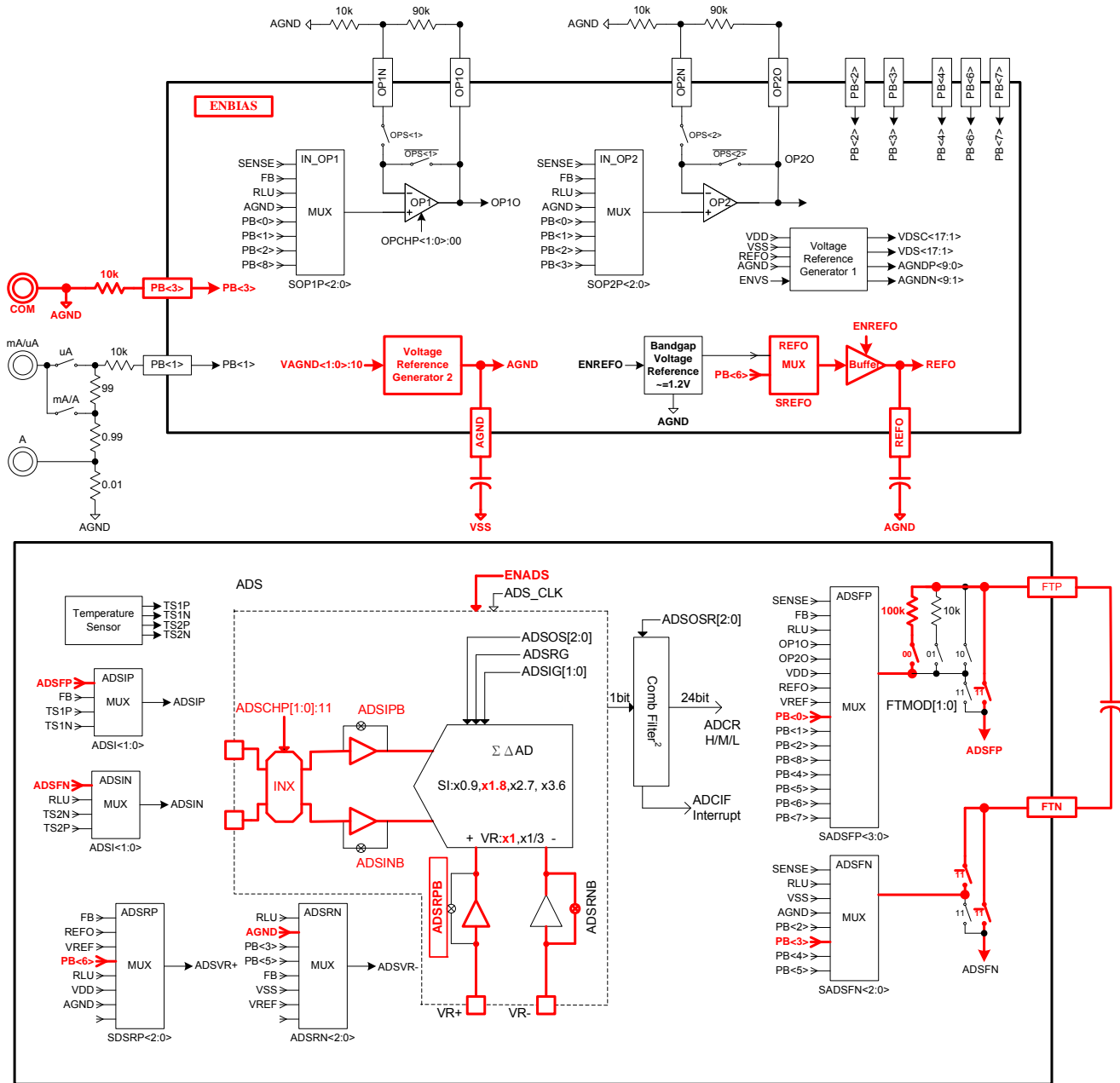


[illegible]

[illegible]

[illegible]

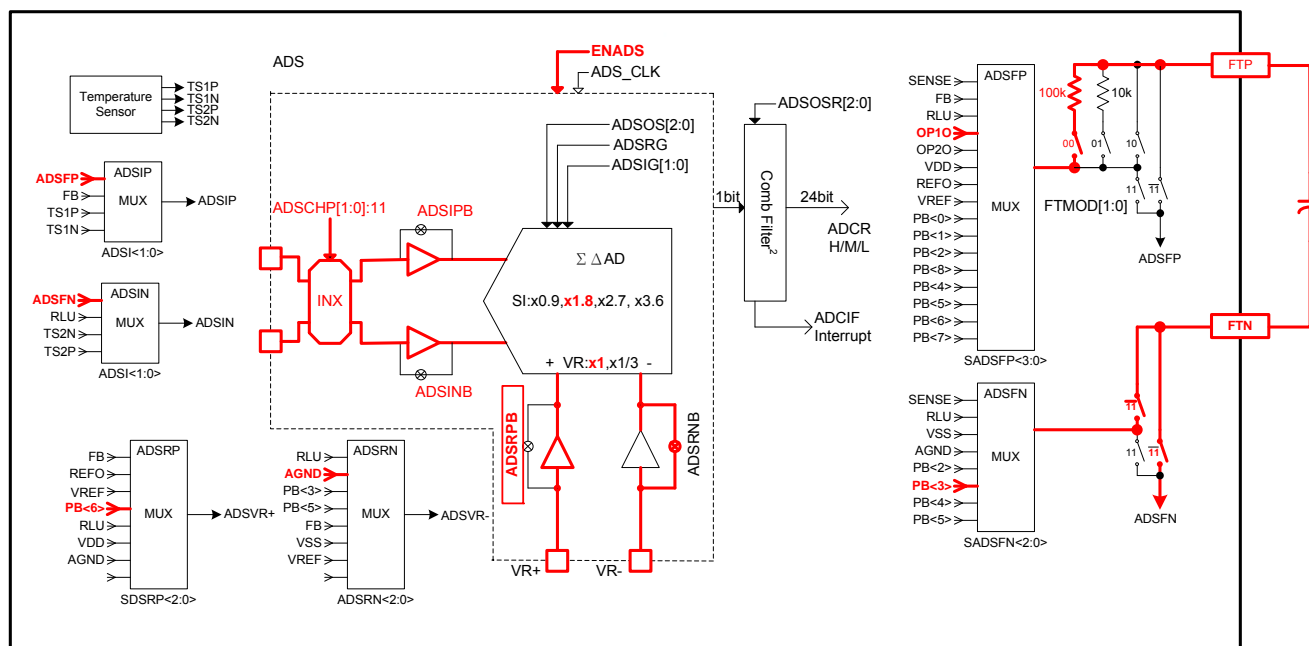
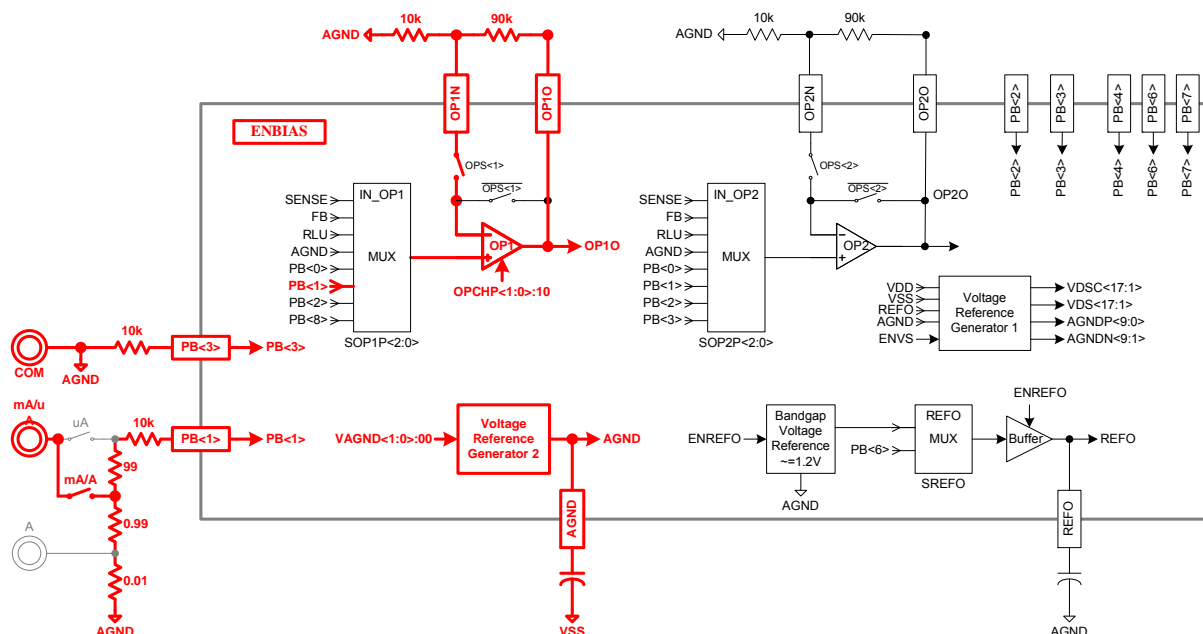
7.2. Diode Measurement Network Configuration



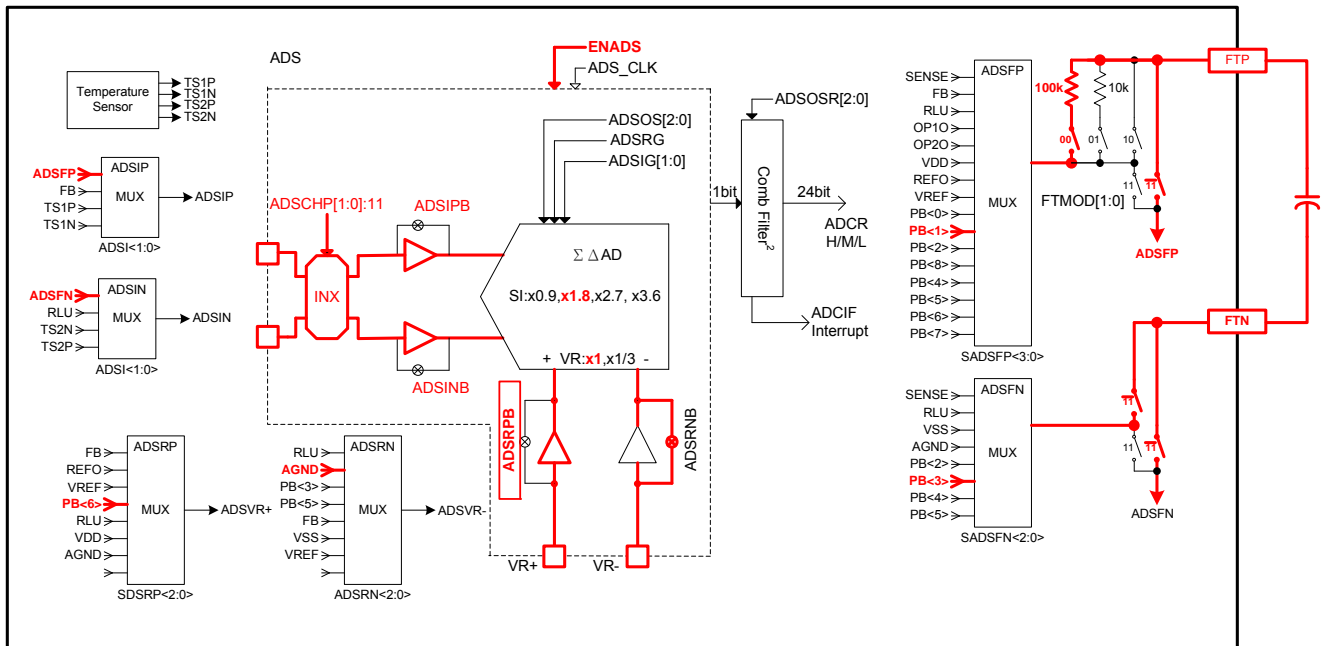
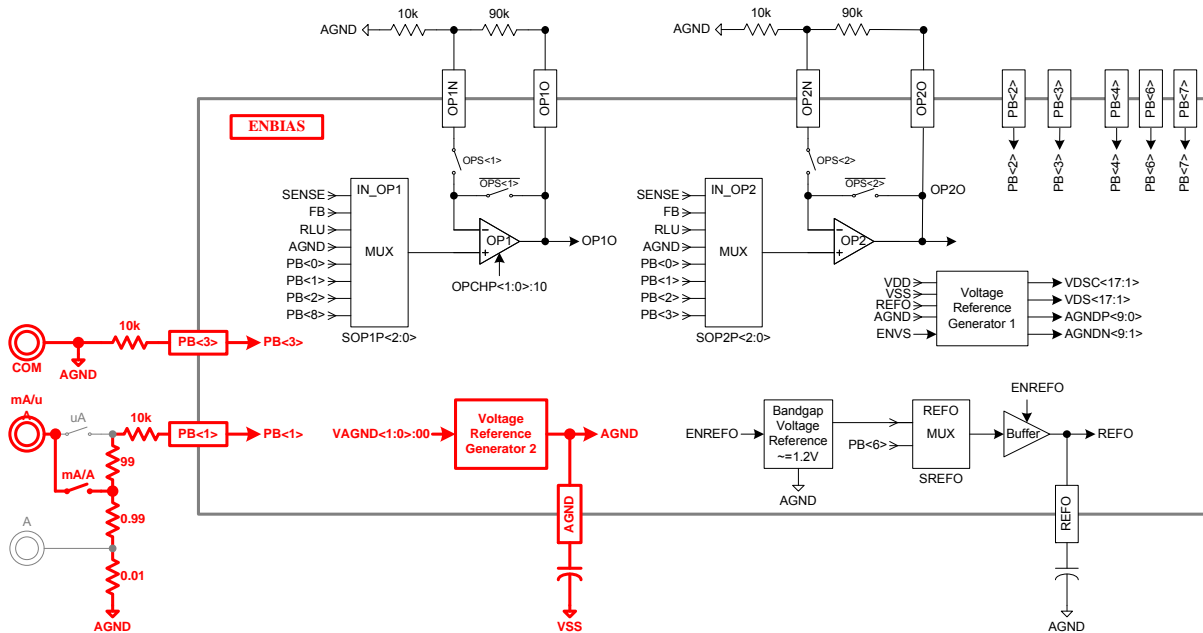
This function can use constant current or constant voltage output measurements. This case is positive constant current output measurement.



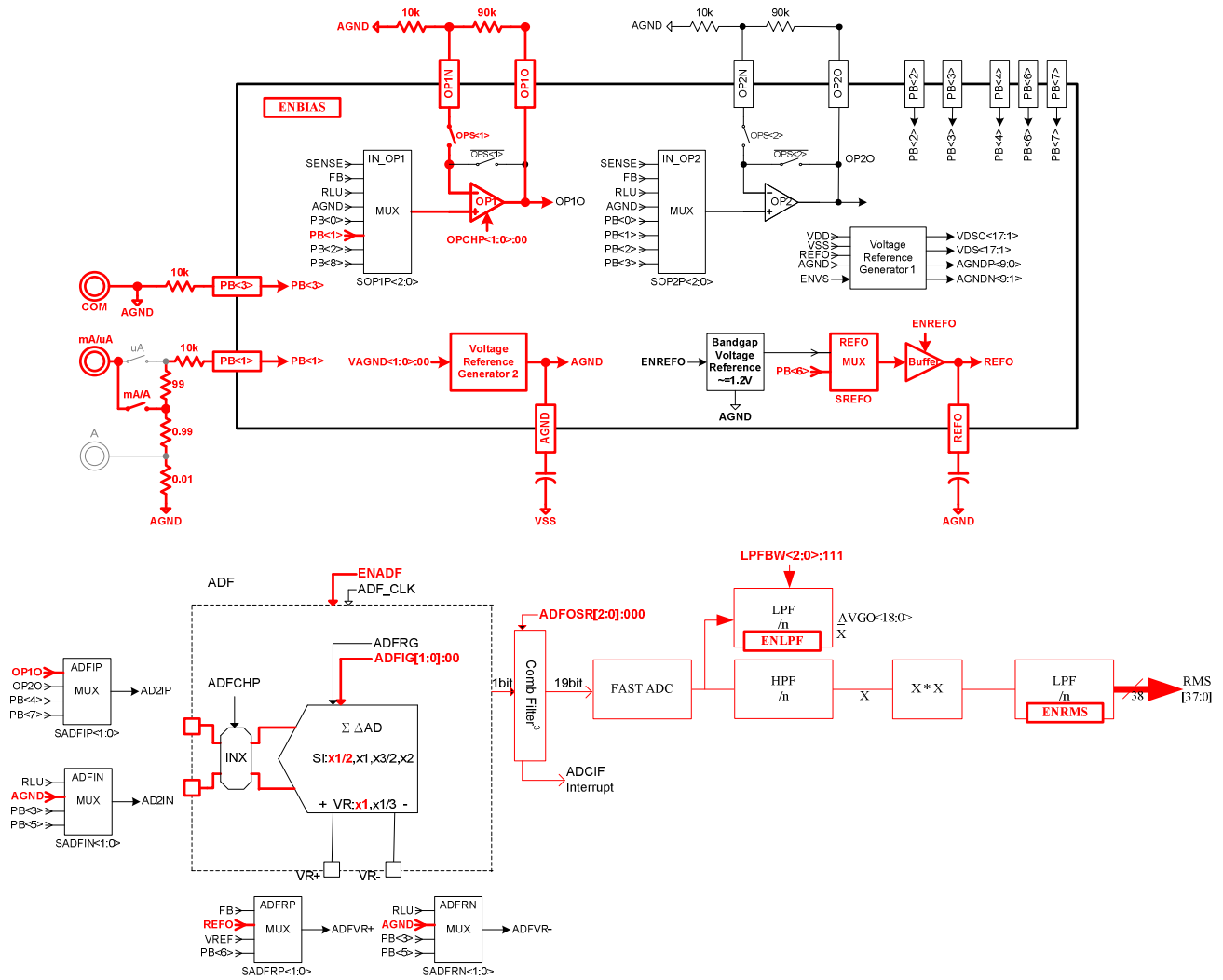
Current measurement is similar with that of measuring mV.

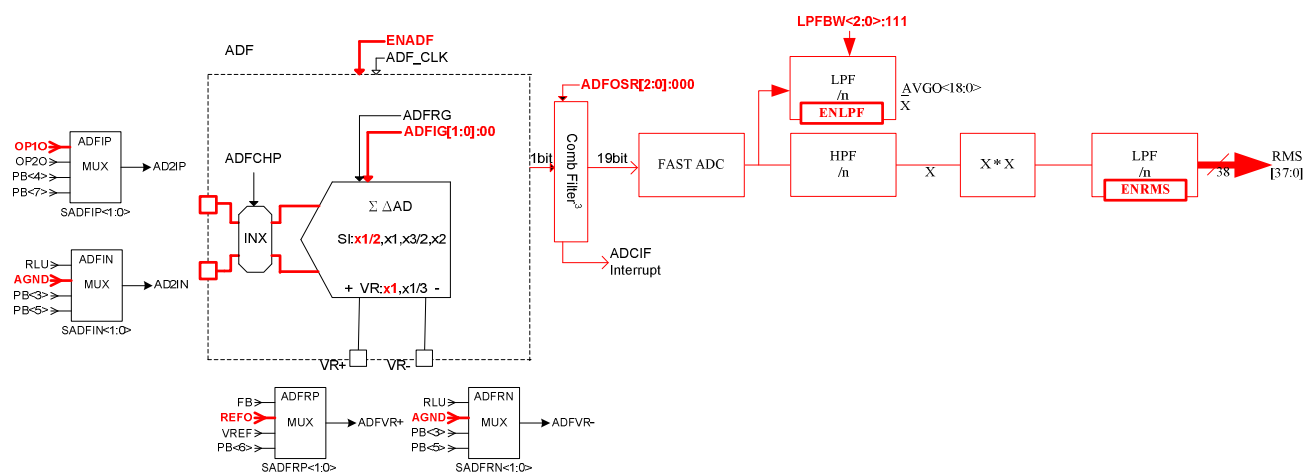


9.2. DC 500mA



9.3. AC 50mA

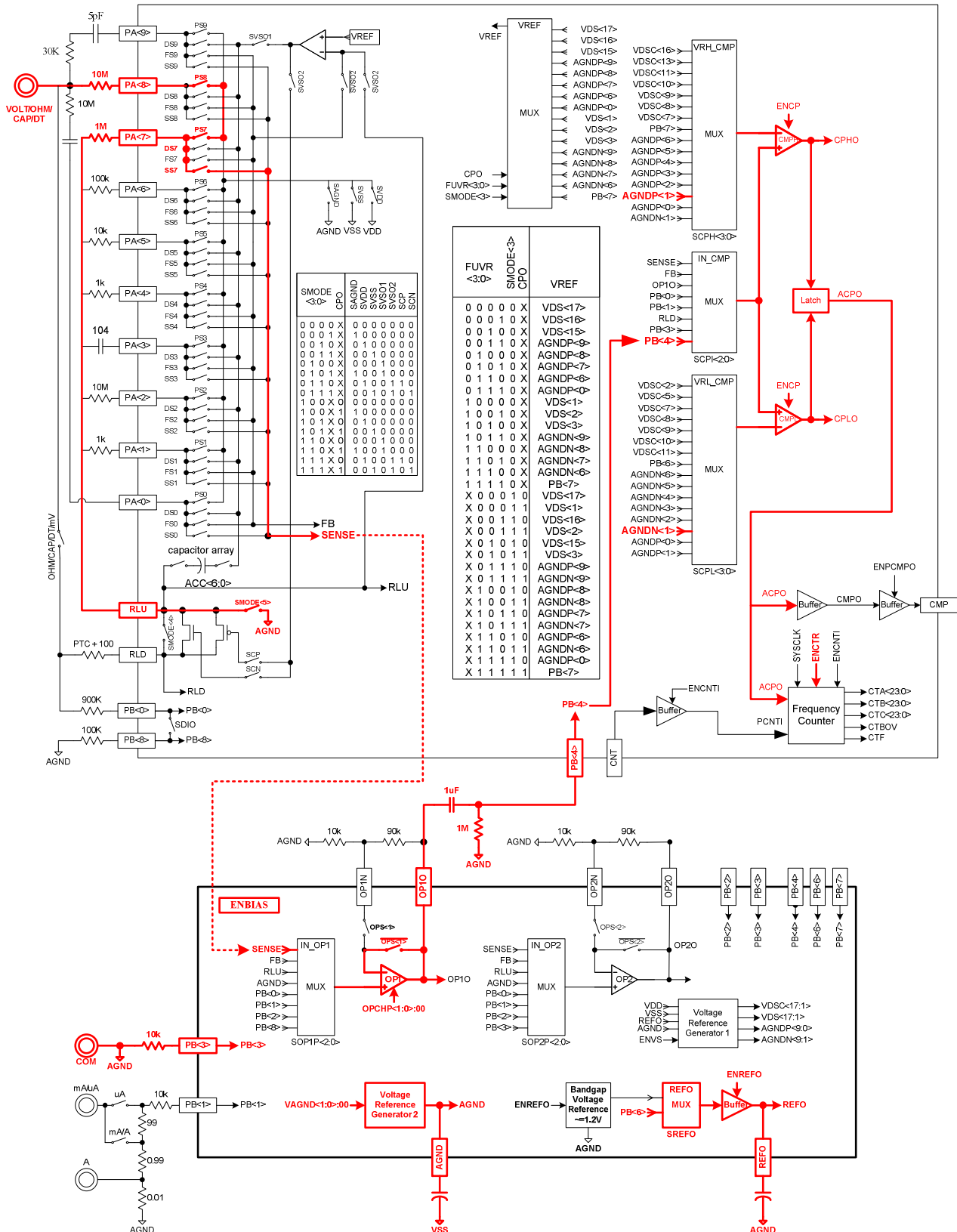




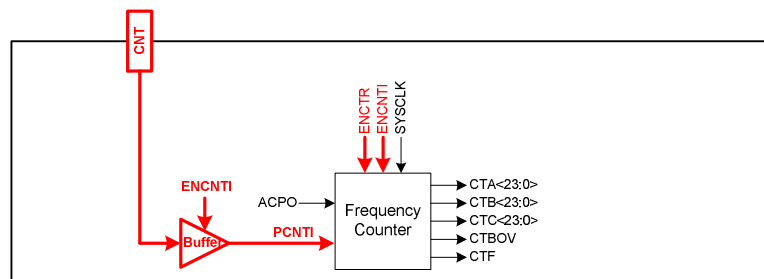
10. Frequency

10.1. Voltage input

When measured frequency, the signal is inputted by PA<n> and PB<n>. If the input contains DC, must be removed by AC Coupled capacitors.



10.2. CNT input



11. Revision History

Major differences are stated thereafter:

Version	Page	Revision Summary
V01	All	First edition
V02	All	Revise all contents