

A high-magnification microscopic image of a silicon chip. The chip's surface is covered with a complex grid of circuitry, including various sized rectangular blocks, lines, and small circular features. A circular orange highlight is centered on a specific component in the middle of the chip. The background is dark and out of focus.

# Single Chip Analog RF Memory & Spectral Imager, ARFM

RF Time & Frequency Domain Snapshots Captured  
with CMOS Single Chip Spectral Imager  
“Spectrum Analyzer on a Chip”

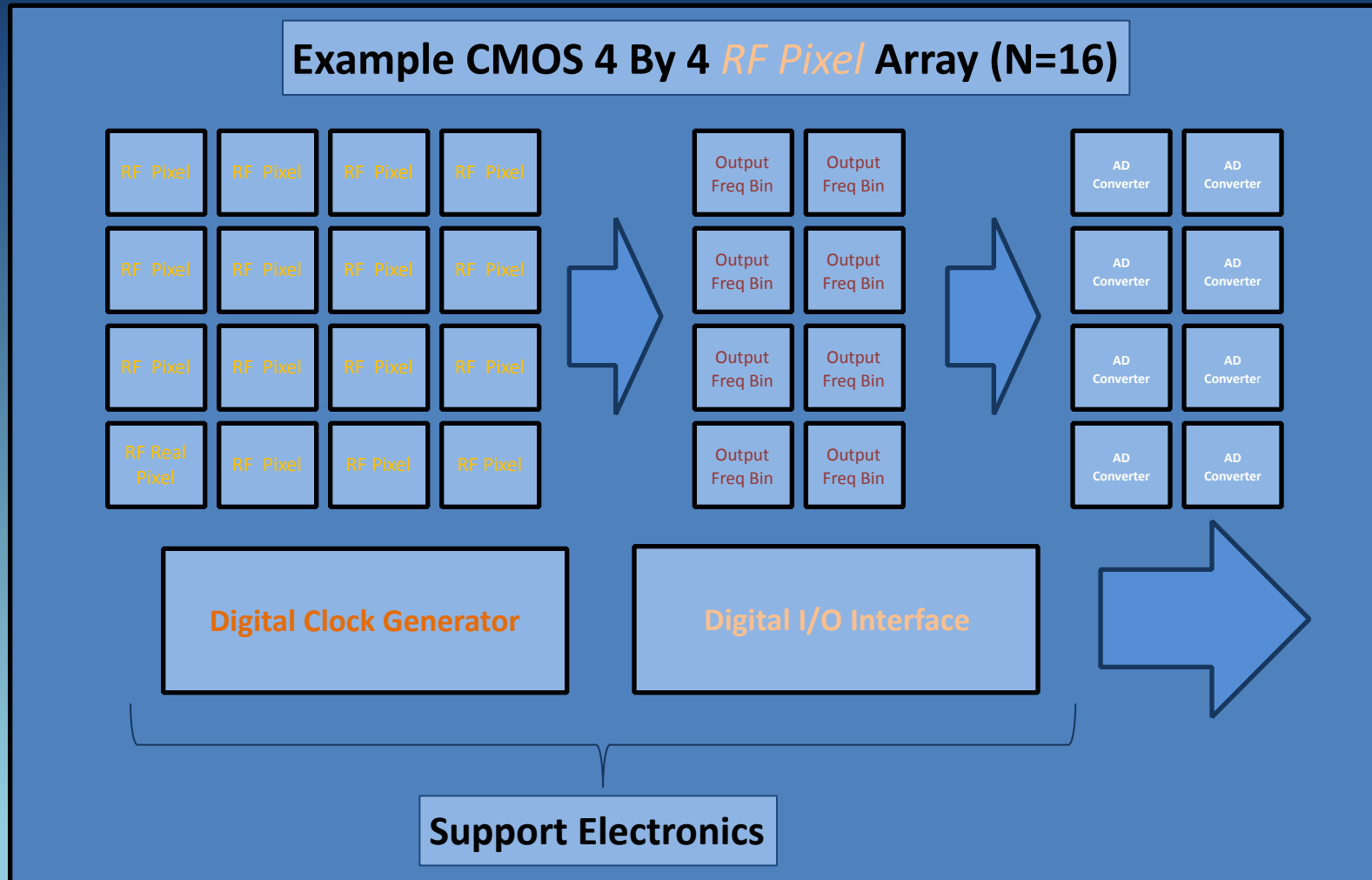
# Single Chip ARFM Time & Spectral Domain Imager

## Utilize Digital Imaging Sensor/DRAM Technology

- Employ Large CMOS Sensor Device Arrays
  - Sensor Configured
    - “N<sub>c</sub>” Columns
    - “N<sub>row</sub>” Rows
    - N Array Size = N<sub>c</sub>\*N<sub>row</sub>
  - Signal Input
    - Applied to each Column via NMOS switch
      - » Column Sequentially Addressed in Time
      - » Stores Signal Input *Current* on **RF Pixel** Column NMOS Device
        - Behaves like N *Current Mode* Sample and Holds
    - Step to next Column when previous Column full
- Captures RF Time Domain
  - Discrete Time Continuous Amplitude
  - N Time Samples
  - N\*ts = Total Capture Time Slot
- Large Number of **RF Pixels**
  - Limited by Chip Size
    - Greater than 100K Pixels
      - » 10u by 10u CMOS (Example)
- High RF Sample Rates
  - Limited by Clock/Switch Speed
    - Improves with Silicon Feature Size Reduction
- Large RF “Image” Capture Time
  - Limited by Chip Size
    - Improves with RF Pixel Number
  - Limited (long end) by NMOS Device Gate Charge Hold Time
    - Dictated by Process Node
    - Limited by Leakage
    - Partial Leakage Compensation Possible

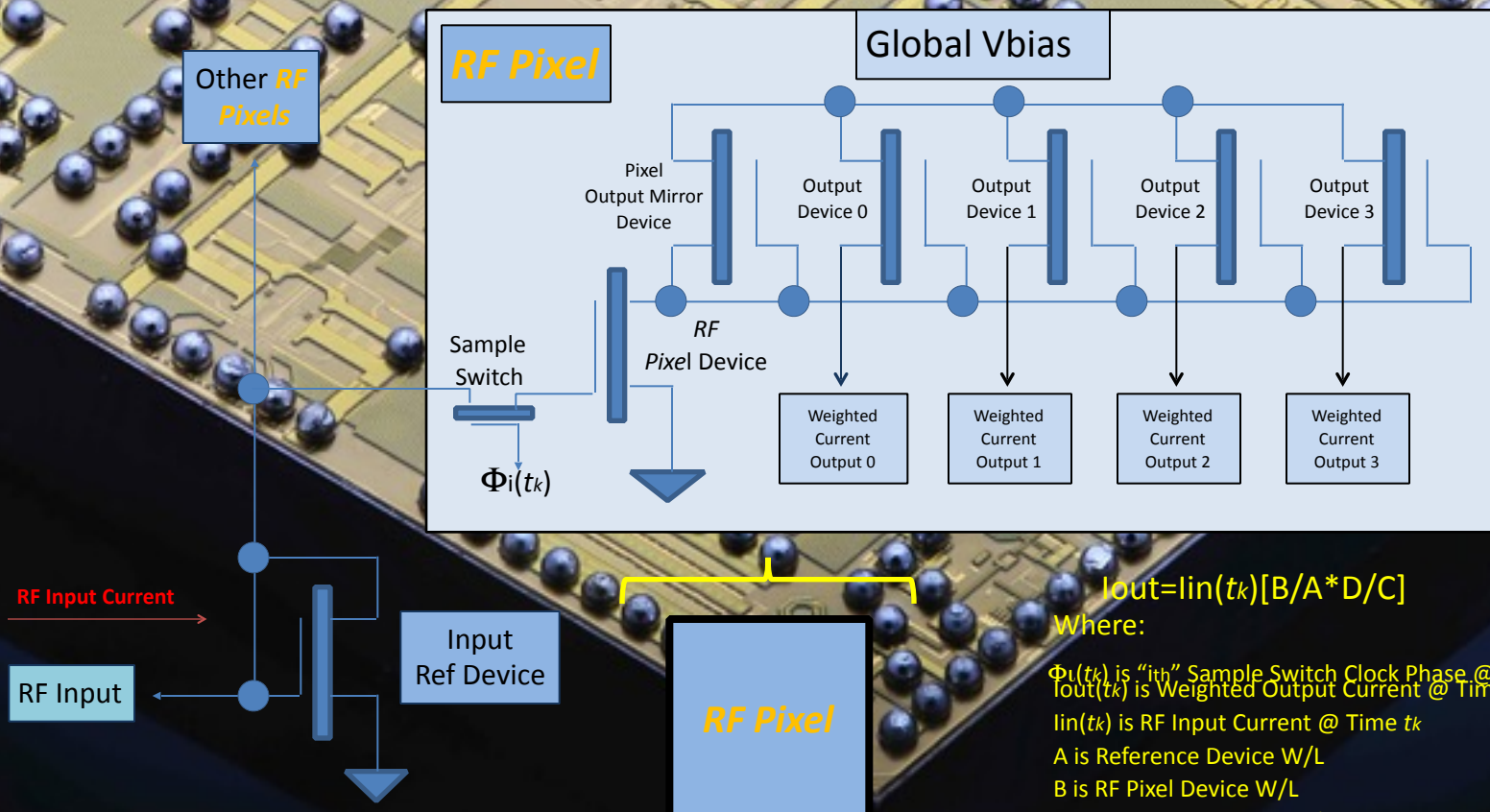
Enables Large Array Single Chip RF Time Domain Signal Capture

# Notional 4 By 4 Example: Single Chip RF Imager



# "RF Pixel" Circuit Concept

Input *RF Pixel*



$$I_{out} = I_{in}(t_k) [B/A * D/C]$$

Where:

$\Phi_i(t_k)$  is "i"th Sample Switch Clock Phase @ Time  $t_k$   
 $I_{out}(t_k)$  is Weighted Output Current @ Time  $t_k$

$I_{in}(t_k)$  is RF Input Current @ Time  $t_k$

A is Reference Device W/L

B is RF Pixel Device W/L

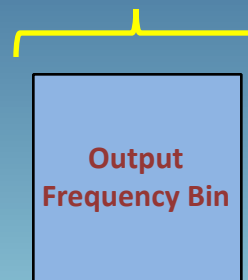
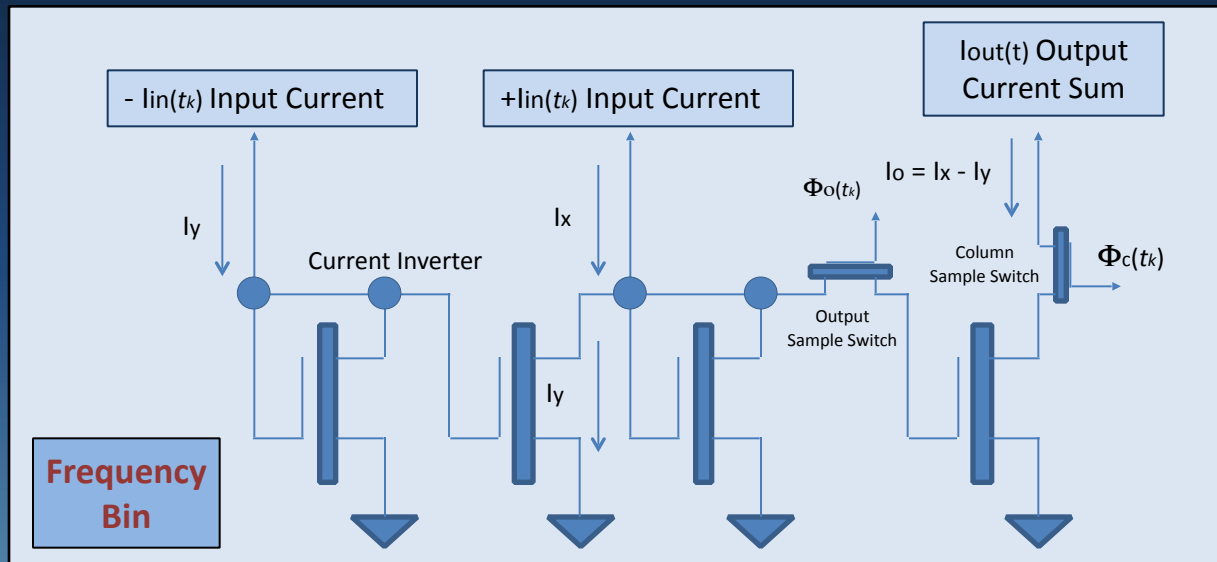
C is Output Ref Device W/L

D is Mirror Device W/L

# Spectral Image Analog FFT

## “Frequency Bin” Circuit Concept

### Output Current Summation *Frequency Bin*



$$I_{out}(t) = \sum +I_{in}(t_k) - \sum -I_{in}(t_k)$$

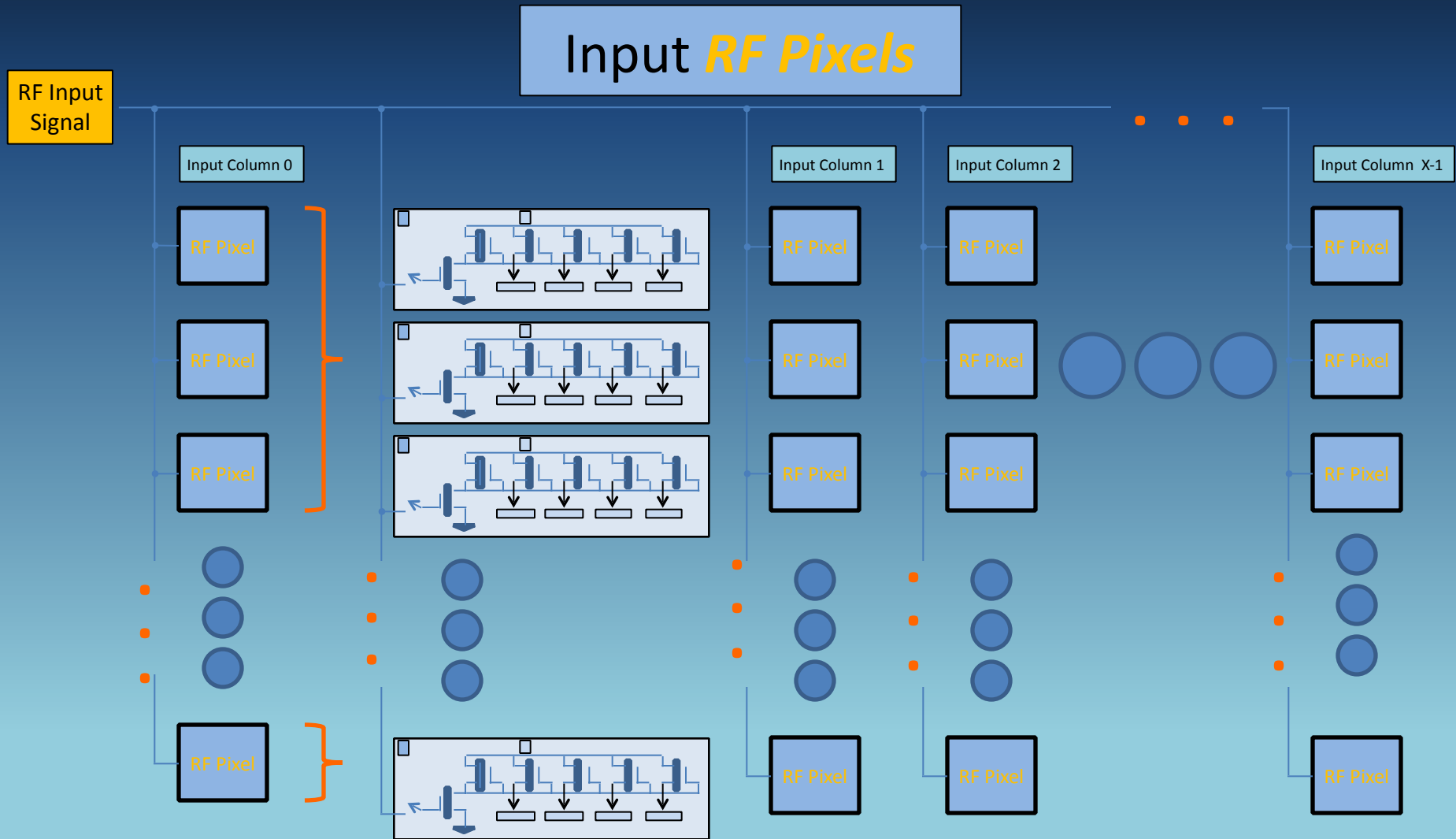
Where:

$I_{out}(t_k)$  is Weighted Sum Output Current

$+I_{in}(t_k)$  is Added Input Current

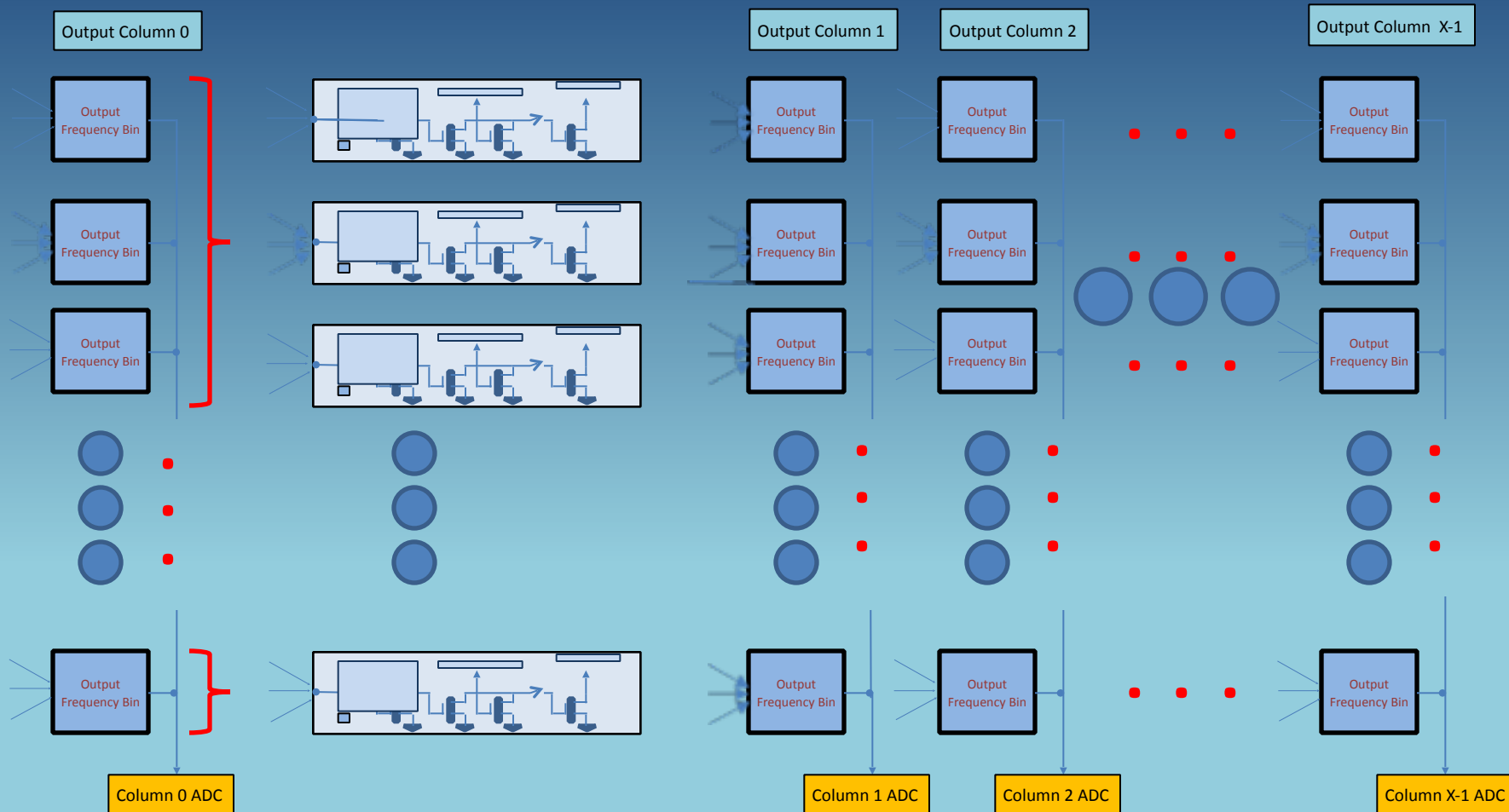
$-I_{in}(t_k)$  is Subtracted Input Current

# Single Chip ARFM Time Capture



# Single Chip ARFM Spectral Image

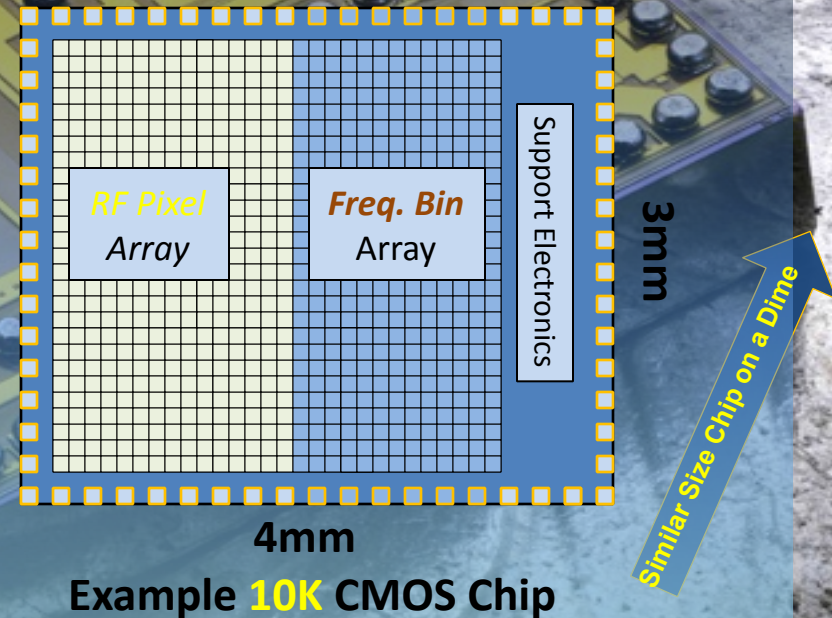
## Output Current Summation *Frequency Bins*





# Example Single Chip 10K RF Pixel ARFM Time & Spectral Domain Imager

- **Example Chip: 10K RF Pixel**, DC-5GHz, @ 1MHz Res. with 1 $\mu$ s RF Spectral Image Capture
  - 4mm by 3mm CMOS Chip Size
    - 100 by 100 X & Y Array
      - 10 $\mu$  by 10 $\mu$  **RF Pixel** Size
        - » NMOS Sample Device
    - 10GSPS Sample Rate
      - 1 $\mu$ s Total RF Time Image Capture
        - » 10ns per Column
      - DC-5GHz Nyquist Frequency Span
        - » 1MHz Frequency Resolution
    - 10 Bit Analog to Digital Conversion
      - One AD Converter per Column
        - » 100 Total
  - Input Clocking
    - Single Input Clock Reference
    - **RF Pixel** Sample Clock Derived
      - Each Column Delay/Phase Locked
    - Column ADC
      - Delay/Phase Locked
    - Output Clock
      - Delay/Phase locked
  - Single 2.7 Volt Supply
    - On Chip Low Drop Out Regulators
    - Higher Efficiency with separate 1.2v Digital Supply
  - Digital Interface
    - 100 10 Bit AD Converter
    - 10K 10 Bit Words
    - High Speed Digital Data Outputs
      - Advanced FPGA Compatible
      - Advanced DSP Compatible



4mm  
**Example 10K CMOS Chip**