AC Input Stage

The scope is connected to the power grid via a power cable and AC plug that conforms to the standards of the country where the scope is to be used. The PSU supports 100 – 250 VAC RMS @ 50 - 60 Hz mains for international compatibility. A 2A 250V fuse provides internal catastrophic failure protection and it's also the only built in transient protection since the circuit does not include an MOV. The Standby Switch can be used to disconnect the AC power completely. With the Standby Switch in the On position the PSU will be at least partially energized at all times and the battery charging circuit will be active.

Following the AC-IN connector (J6) we find a conventional EMI filter consisting of two Y capacitors (CY1 and CY2), one X capacitor (CX1), and a common mode choke (LF1). Since this stage is ahead of the bridge rectifier it provides filtering for incoming power grid noise as well as filtering for outgoing noise generated by the PSU. CY1, CY2, and LF1 are used to suppress common mode noise and CX1 is used to suppress differential mode noise. R1 and R1A provide a safety discharge path for the X and Y capacitors when the PSU is disconnected from the mains.

A 10Ω negative temperature coefficient (NTC) thermistor is connected in series with the AC live to protect the fuse and PSU rectifiers from inrush current when the PSU is first turned on and the electrolytic capacitors are charged for the first time. The thermistor self heats in a short time and its value drops to a fraction of an ohm. There is no provision to short out the thermistor (e.g. with a relay) once its function is performed. As a result the thermistor remains hot and will not provide protection during a short power interruption. However, this is normally not a concern since the electrolytic capacitors will be at least partially charged.

Unregulated Rectifier Stage

This stage consists of a conventional bridge rectifier implemented with four 1N4007s (D1 -D4), an electrolytic capacitor (EC1), and a high frequency bypass capacitor (C3). Since the AC input is 100 – 250 VAC RMS, the unregulated DC output will be √2 greater or about 140 – 350 VDC. There is no power transformer in this stage, so it is theoretically possible to use a 140VDC supply instead of AC mains to power the scope. Note, however, that this is not specified or recommended by the manufacturer.

140 – 350 VDC to 8.4 VDC DC/DC Converter

This stage is an isolated DCM (discontinuous mode) switching regulator built around the Richtek R7731A PWM Flyback Controller. The components associated with Primary and secondary side isolation are flyback transformer TR1, opto-coupler PH2, and bypass capacitor CY3.

The converter's output is used to charge the optional Li-ion battery pack as well as to provide the DC input for other DC/DC converters necessary for scope operation. When the scope is battery operated, the 7.4V Li-ion battery pack provides the DC input for the other DC/DC converters.

The converter's output voltage is set to 8.4V by a CV (constant voltage) feedback loop external to the R7731A. In addition, an external CC (constant current) feedback loop is set to 3.75A. The two external feedback loops are necessary to support the converter's battery charging function. When the converter's output current reaches 3.75A, the CC loop will cause the converter's output voltage to drop below 8.4V

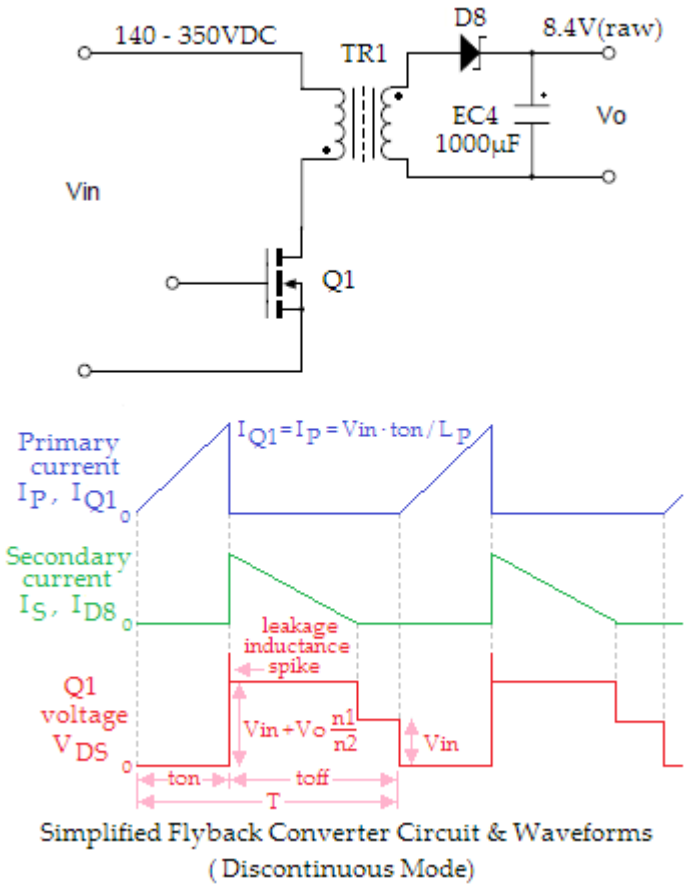
as necessary. This insures that the battery charge current doesn't exceed the battery pack's cells maximum continuous charge current specification (≤4.0A).

The Flyback Circuit & its Output Connections

The Flyback Circuit:

A flyback transformer like TR1 is more like a coupled inductor than a classic transformer. When Q1 is turned on, current flows through the primary and energy is stored in the core, when Q1 is turned off this energy is coupled to the converter's output through the secondary. In contrast, a classic transformer couples the energy from the primary to the secondary continuously and therefore doesn't need to store energy. As a result, classic transformers are not designed to store large amounts of energy and are a very poor choice for flyback applications.

Flyback transformers require high peak currents to store the large amounts of energy required for their operation. Their primary inductance is designed to be significantly lower than what is required for a classic transformer so that it won't oppose a rapidly changing current as much. In most designs this is accomplished by incorporating a gap in the core. The gap stores most of the high peak current energy and as a result helps avoid transformer core saturation.



Simplified Flyback Converter Circuit & Waveforms
(Discontinuous Mode)

Note that the polarity of TR1's windings is such that D8 blocks any current coupled to the secondary during Q1's on time. When Q1 turns off, the secondary voltage reverses while the energy stored in the gap attempts to maintain a constant flux in the core. As the flux rapidly decays the resulting secondary current flows through D8 to the output load. The magnitude of the peak secondary current depends on the peak primary current reached at Q1's turn-off, the transformer's primary to secondary turns ratio, and other transformer characteristics. For a step down transformer such as TR1, this results in a secondary current that is higher than the peak primary current. Ideally, the ratio between the two currents would reflect a constant Ampere-turn balance.

As shown by the Q1 voltage waveform on the illustration, the secondary current that flows as a result of Q1 turning off is coupled back through the transformer to the primary. In addition, a voltage spike is also coupled back at Q1's turn-off due to the stored energy in the transformer leakage inductance. This means that Q1 must be capable of blocking the unregulated supply voltage, plus the reflected voltage, plus the leakage spike. The FIR5N60F MOSFET used for Q1 has a maximum drain-source voltage of 600V. This is certainly not excessive since in this design just the unregulated supply voltage can be as high as 350VDC. Note that depending on the design of the flyback transformer, the voltage coupled back to

the primary by the secondary current can be as high as Vin, up to 350VDC in our case. I've been unable to get a datasheet for TR1, probably because it's custom made for Owon, so I don't know for sure if Q1 is actually underrated. However, I've seen the recommended specs for the switching MOSFET or transistor in similar power supply designs. A breakdown voltage of between 800 and 1000V is usually recommended.

In a flyback design the inductance of the secondary is in series with the rectifier when current is delivered to the load. This tends to have the same effect as a filter inductor in the output circuit. As a result, the need for a large inductor in a pi filter arrangement is reduced or eliminated. However, without a pi filter, the output capacitor needs to be very large and with very low ESR to be able to smooth a pulsating output current which has high peak values. So in many cases, as for example this SMPS, an LC filter, which is about 8 times more effective at ripple reduction than a capacitor alone, is used instead.

The Output Connections:

The junction of D8, EC4, and L1 is designated 8.4V(raw). The name indicates that this output is ahead of the second stage of the output filter (L1 and EC5). The only function of this output is to provide the bias voltage for PH2's light emitting diode. PH2 is the opto-coupler that provides primary to secondary side isolation between the error amplifiers (IC2C & IC2D) and the PWM controller (IC1). Using the raw output for this circuit in a DCM (discontinuous mode) SMPS that contain a pi filter is a widely used strategy. Its purpose is to cancel out the influence of the extra phase delay and resonance introduced by the second stage filter on the CV error amplifier. As a result, the overall response and phase of the CV feedback loop circuit is nearly the same as if the second stage filter didn't exist.

The complete pi filter consists of EC4, L1, and EC5. A bypass capacitor, C7, provides a path for high frequency signals to reduce EMI. The CV error amplifier senses load variations by monitoring the voltage at the pi filter's output. When the PWM controller is under the control of the external CV feedback loop the pi filter's output voltage is regulated to a constant 8.4V.

The 8.4V output is connected to the optional battery pack via J1 and the 6 pin battery connector. When the optional battery pack is being charged the external CC feedback loop may take over control of the PWM controller. The transition takes place when the output current reaches 3.75A. Since in this case the objective is to limit the current to 3.75A the output voltage may drop below 8.4V.

R17 and U1 are used to provide a stable 2.5V reference voltage to the Op-amps used to implement the external feedback loops (IC2C & IC2D). R14, R14A, and R14B are used to sense the converter's output current. Their combined value is 0.0333Ω. When the output current reaches 3.75A the voltage drop between GND-B and GND-C is 125mV. This voltage drop is monitored by the CC error amplifier (IC2C). 125mV is the threshold that causes it to take over control of the PWM controller.

D9, EC3, and R11 are used to drive the green anode of the Power Indicator tricolor LED. The LED will emit green light if a positive voltage is applied to the green anode but not the red anode. If both anodes receive a positive voltage the LED will emit yellow light. Green indicates that the 8.4V converter is energized, yellow indicates that in addition, the optional battery pack is charging. When the scope is running on battery power D8 is reversed biased and as a result the green anode is at ground. If the red anode is also at ground (which it will be, see below), the LED is turned off. Note that D9 is a standard 1N4007 rectifier intended for 50/60Hz operation, however, it is being used in a circuit operating at 65kHz. A possible replacement candidate is the UF4007. The reverse recovery of the 1N4007 is 30µs

(about 2 switching cycles at 65kHz) compared to 75ns for the UF4007.

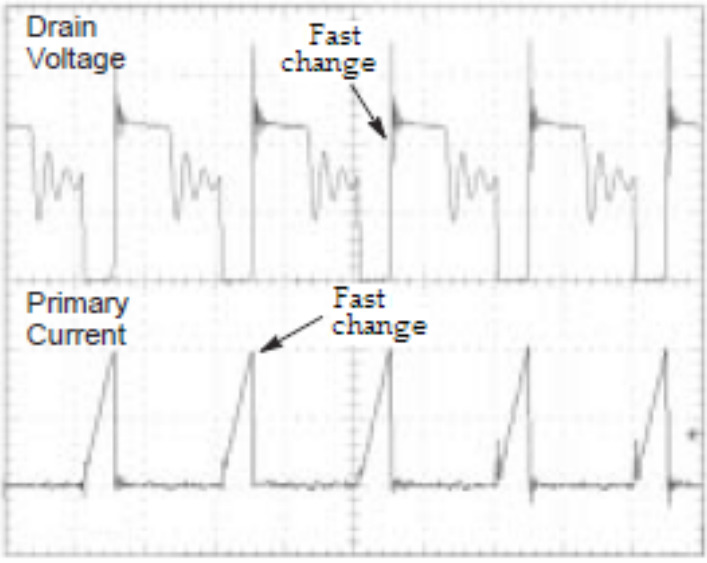
R13, R13A, and R13B are used to sense the charge current delivered to the optional battery pack. Their combined value is 0.0333Ω. When the charge current drops to about 100mA the voltage drop across these resistors is 3.3mV. This voltage drop is monitored by IC2B. IC2B's output drives the red anode of the Power Indicator tricolor LED. When the battery is charging the voltage drop across the parallel resistors will exceed 3.3mV. As a result IC2B's output will be positive. Since the LED's green anode is also positive the LED emits yellow light, indicating that the battery is charging. The threshold at which IC2B switches is output to ground is 3.3mV. As a result, when the charge current drops to about 100mA the LED will emit green light. When the scope is running on battery power the voltage across the parallel resistors is always negative. As a result IC2B's output will apply ground to the LED's red anode. Since the green anode is also at ground the LED is turned off.

When pushed in, the Power Switch (J2) connects the 8.4V output, designated 8.4V(Sw), to the adapter board via J3's pins 5 & 6 . EC10, which is physically close to this connection, is used to provide additional filtering before the 8.4V(Sw) output is received by the adapter board. The 8.4V(Sw) output is also used to power the -7.6V DC/DC converter (IC3). Finally, the 8.4V(Sw) output activates opto-coupler PH1.

PH1 is used to provide an isolated version of the mains AC signal to the scope's AC trigger circuit via J3's pin 1. R2, R2A, R2B, and R2C limit the current flow through the opto-coupler's light emitting diode. R36 and R38 are a voltage divider used to set the AC Trig signal to the level required by the scope's trigger circuit.

The Snubber Circuits:

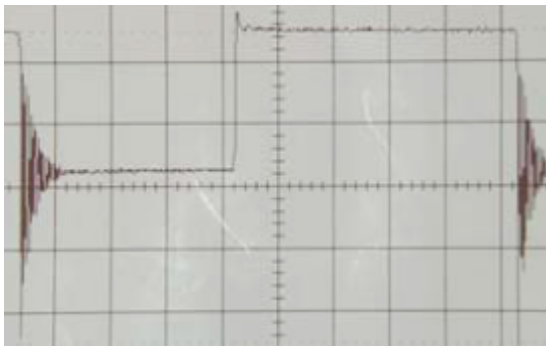
The illustration shows primary side waveforms when there are no snubbers present. In an ideal circuit with ideal components the waveforms produced as a result of Q1 turning on and off or D8 turning on and off would be squarewaves. However, a real transformer will have leakage inductance. In addition, all circuit components, including circuit traces, will have stray capacitances.



When Q1 turns off the current flowing through the leakage inductance is abruptly stopped. The resulting back EMF causes a large voltage spike on Q1's drain. Since the leakage inductance and stray capacitance form a resonant circuit, the spike is just the beginning of subsequent ringing that persists until the circuit's resistance gradually dissipates it. Since the leakage inductance and stray capacitance values are usually low, the ringing frequency can be in the MHz range.

The second ringing burst, starts when the secondary current has ran dry and D8 turns off. As a result, the resonant circuit is now formed by the inductance of the primary and the stray capacitance. Due to the larger inductance the frequency is lower and unlikely to produce EMI.

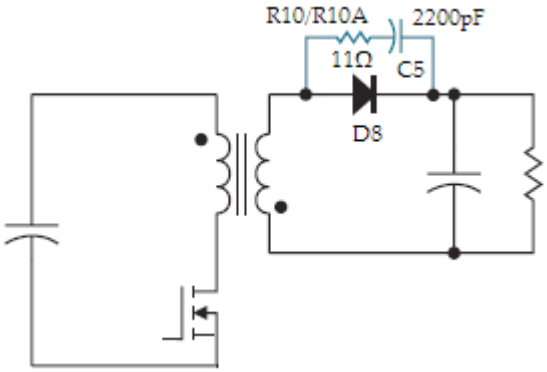
Meanwhile, on the secondary, a large high frequency ringing burst, as shown in the illustration, is produced due to D8 turning off. The mechanism that produces this burst is analogous to the mechanism that produced the ringing burst in the primary at Q1's turn-off.



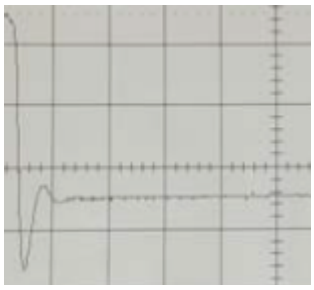
Excessive ringing can expose the MOSFET's drain and the Schottky rectifier at the converter's output to voltages in excess of their breakdown rating. This may eventually lead to component failure. In addition, the ringing energy is a large contributor to the radiated and conductive, both differential and common mode, noise generated by the PSU. If not adequately suppressed, this noise can propagate through the load and thus affect the operation of the entire system. The PSU's EMI spectrum will typically show a peak at the ringing frequencies.

There are three common snubber configurations that are widely used to dampen the ringing and protect circuit components:

- The RC snubber, which is simply a resistor and a capacitor in series placed directly across the component to be protected. This is the approach used for D8. The RC snubber components are C5, R10, and R10A.



To properly dampen the ringing the resistor should be the same value as the impedance of the resonant circuit. The capacitor's reactance at the ringing frequency should be equal or less than the resistor's value. However, too large a capacitor will increase the power loss at the switching frequency and a higher wattage resistor may be needed.



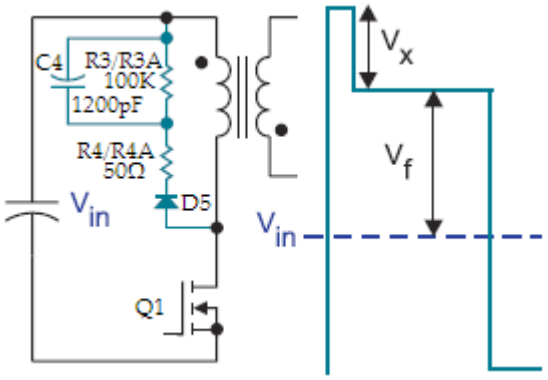
The illustration shows the secondary waveform with a properly designed snubber circuit across the Schottky rectifier.

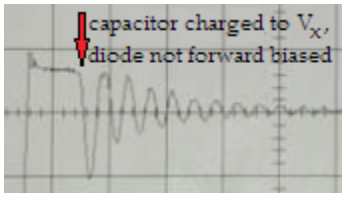
I don't know if the snubber components used in this circuit have optimal values, so this should be investigated during the experimental phase of this project.

- The RCD clamp consists of a capacitor and a resistor in parallel and a diode in series. The circuit is placed across the transformer winding as shown in the illustration below. The capacitor should be large enough to keep a constant voltage during a switching cycle. This is required so that the voltage across it is always close to Vf (the voltage coupled back from the secondary). The parallel resistor determines the capacitor's discharge rate. The charge that remains the next time the MOSFET turns-off determines the clamp voltage, and as a result Vx, which represents how much higher than Vf the drain voltage is allowed to rise. A lower resistance will allow the capacitor to discharge quicker and cause Vx to be lower. However, this

also increases the power losses.

RCD clamps limit the large voltage spike and several ringing cycles to the Vx value. However, once the capacitor is charged, since the diode is no longer forward biased, the remaining cycles of the ringing burst may not be dampened. This happens when due to the diode's slow recovery time, current is allowed to flow in the reverse direction before the diode switches off. For this reason, the diode used in this circuit should be as fast as possible.



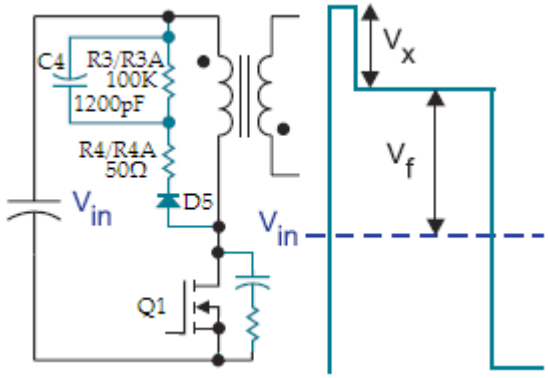


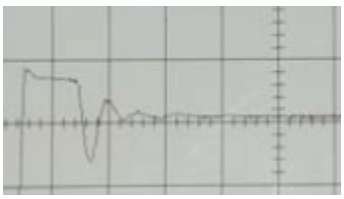
The components used to implement the RCD snubber are C4, R3, R3A, and D5. R4 and R4A are not part of a classic RCD clamp. They may be used to limit inrush current, or may be an attempt to dampen the ringing frequency with a resistor value that matches the resonant's circuit impedance. However, if D5 switches quickly, there wouldn't be a chance for this to happen.

Note that D5 is a standard 1N4007 rectifier intended for 50/60Hz operation, however, it is being used in a circuit operating at 65kHz in an application that deals with ringing in the MHz range. Replacing this diode with a fast recovery equivalent should be investigated as a means of reducing EMI. A possible candidate is the UF4007. The reverse recovery of the 1N4007 is 30µs (about 2 switching cycles at 65kHz) compared to 75ns for the UF4007.

I don't know if the remaining snubber components have optimal values, so this should also be investigated during the experimental phase of this project. Another thing to be investigated is the possible benefit of also replacing D9 and adding a snubber circuit to it.

- A combination of an RC snubber and and RCD clamp. This alternative approach may be used if it's not possible to obtain adequate results with the RCD clamp by itself. By adding an RC snubber as illustrated to the existing RCD clamp, the combination will typically produce the lowest possible EMI levels. However, the converter will incur additional power losses associated to the added RC snubber.





The components for the RC snubber are selected as previously described:

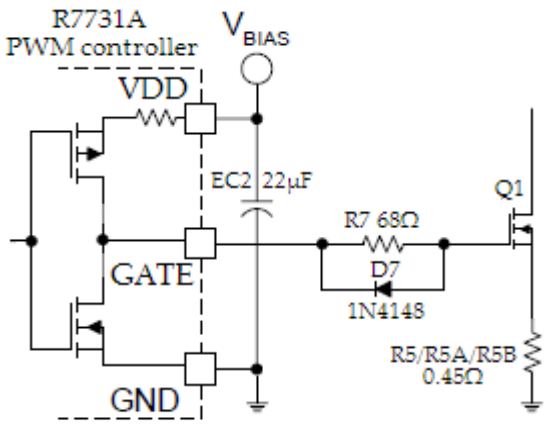
To *properly dampen the ringing the resistor should be the same value as the impedance of the resonant circuit. The capacitor's reactance at the ringing frequency should be equal or less than the resistor's value. However, too large a capacitor will increase the power loss at the switching frequency and a higher wattage resistor may be needed.*

As shown in the illustration, the added RC snubber should effectively dampen the cycles of the ringing burst that the RCD clamp circuit may have left undamped.

Adding an RC snubber to Q1 should also be investigated during the experimental phase of this project. This should be considered after replacing D5 with a fast diode and optimizing the values of the remaining RCD clamp components.

The Gate Drive Circuit:

When driving the gate of the main switch directly from the gate output of the PWM controller the physical distance between the PWM controller and the MOSFET must be minimized. Otherwise the inductance of the loop formed by the gate drive and ground return traces can slow down the switching speed as well as cause ringing in the gate drive waveform.



Another consideration is the gate drive current capability of the PWM controller, 200mA for the Richtek R7731A, and its power dissipation capability, 0.4W for the SOT-23-6 version of the R7731A that is used in this PSU. Larger MOSFETs may not be able to operate at optimal speed because their gate capacitance can't be charged fast enough, and or may cause over temperature problems because the gate current consistently exceeds the PWM controller's power dissipation capability.

To limit the PWM controller's power dissipation an external gate resistor like R7 may be used. Note that this also reduces the rate of charge and discharge for the MOSFET's gate capacitance, which slows down the MOSFET's switching time. Slower switching times reduce ringing and EMI, but introduce power losses because of additional dissipation across the MOSFET during the transition time.

In DCM (discontinuous mode) the turn-on time is not as critical because it occurs during a dead period where there is no current flowing through the circuit. As a result power losses during MOSFET turn-on are less and further slowing down the turn-on time may be an attractive option. Not only would this transfer some of the power dissipation to the gate resistor but would also help reduce ringing and thus EMI.

In any case, the MOSFET's turn-on time shouldn't be faster than the reverse recovery time of the output Schottky. This is because depending on the current duty cycle, the output Schottky may not stop conducting and start its reverse recovery period until the secondary current reverses direction. This event is caused by, and therefore coincides with, the beginning of the MOSFET's turn-on time. If the MOSFET turns-on too quickly, since the Schottky hasn't had a chance to switch yet, secondary current in the reverse direction flows through it, which is not helpful and may cause additional ringing.

The MOSFET's turn-off time is more critical because it occurs during the primary's peak current. A slow turn-off time would result in significant power losses under these conditions. If an external gate resistor is used, additional circuitry can be added to accelerate the discharge of the MOSFET's gate capacitance. For example, a diode like D7, can allow a faster discharge of the MOSFET's gate

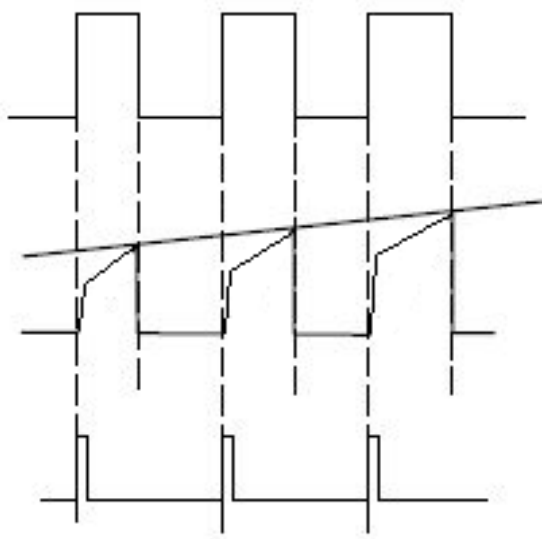
capacitance by shunting R7 when the controller pulls its GATE output to GND. A fast diode like the 1N4148 is required. Unfortunately the diode is not fully active until the end of the discharge due to its Vf (forward voltage) limitation. More elaborate higher efficiency circuits may also be used.

The MOSFET gate is driven by high current spikes which besides producing EMI may disrupt the operation of the circuitry inside the PWM controller. It is important to have a bypass capacitor placed physically close or preferably directly across the PWM controller's Vbias and GND connections. The capacitor should be large enough to provide the entire gate drive current at turn-on with no appreciable ripple across it. EC2 seems to be close enough to the R7731, but I don't know for sure that it meets the other requirements. This should be investigated during the experimental phase of this project.

R5, R5A, and R5B are used to sense the primary current. The voltage drop across these resistor is monitored by the PWM controller's CS (current sense) input. The operation of the PWM controller is explained in the next section.

The R7731A PWM Controller

The R7731A is a current mode PWM controller, it has a current sense input in addition to a comparator input for external feedback loops. The controller's CS (current sense) input, not to be confused with the external CC feedback loop, is used to establish a primary side current limit. When this limit is reached the present Gate pulse ends. As a result, the external CV and CC feedback loops control of the pulse switching is limited to Gate pulse widths that don't exceed the programmed primary side current limit. In contrast to non-current mode PWM controllers, the primary side current limit influence over the control of pulse switching has benefits such as instantaneous response to input voltage variations and therefore better line regulation. It also simplifies the design and implementation of the CV and CC external loops since they only need to deal with load variations.



GATE,
wider pulses cause converter to increase its output

COMP (CV or CC),
positive slope indicates an increasing load

CS with leading edge blanked & amplified X3,
larger amplitude indicates a larger primary current

Oscillator, 65kHz (15.4µs/cycle)

R7731A Startup Circuit

The R7731A requires <36µA to start up, however, the start up current should always be <380µA if hiccup mode is expected to operate successfully. This requirement is fulfilled with series resistors R6, R6A, and R6B which supply about 75µA to VDD when the unregulated DC supply reaches about 90VDC. When the supply reaches 350VDC the current increases to about 300µA. The R7731A starts

up when EC2 charges to 14V. From this point on the output of TR1's auxiliary winding (pins 5 and 3), rectified by D6 and filtered by EC2, is used to supply VDD with a voltage within the recommended range (12V to 25V). R8 is used to limit inrush current when EC2 is first charged via D6. Note that D6 is a standard 1N4007 rectifier intended for 50/60Hz operation, however, it is being used in a circuit operating at 65kHz. A possible replacement candidate is the UF4007. The reverse recovery of the 1N4007 is 30µs (about 2 switching cycles at 65kHz) compared to 75ns for the UF4007.

The R7731A has built in Under Voltage Lockout (UVLO) and Over Voltage Protection (OVP) features that monitor the VDD input. The UVLO waits until VDD reaches 14V before enabling the controller. It's hysteresis curve allows the controller to continue working even if there are subsequent variations in VDD as long as it doesn't drop below 10V. This allows a reliable startup, otherwise the controller would be shutdown when EC2 partially discharges during the short time that it takes for the auxiliary winding of TR1 to start providing VDD. OVP will shutdown the controller if VDD reaches 27V. This is a measure against catastrophic failure such as a runaway converter output voltage.

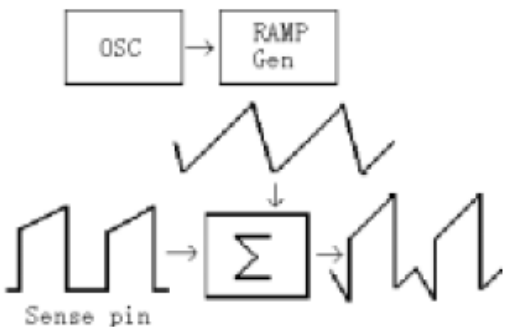
R7731A Oscillator Circuit

The oscillator's operating range is 50kHz to 130kHz. The desired frequency in kHz is set by the value of the resistor connected between the RT input and ground as per the formula: f = 6500/R in kΩ. Since R9 is 100K the oscillator's center frequency in this application is about 65kHz.

The R7731A uses a jittering oscillator. This feature's function is to smooth the EMI signature of the converter. The frequency deviation is ±6%. This causes the switching components to operate at the jittering frequencies instead of on a single frequency. As a result, any EMI generated by the switching components is spread over a wider frequency range.

The oscillator also controls the Gate pulse's maximum duty cycle. This is implemented via the internal Dmax output. Normally one of the feedback loop ends the present Gate pulse. However, if the pulse has not ended when the duty cycle approaches 75%, the Dmax output, via the OR gate, will reset the Gate latch and end the pulse. This mechanism limits the duty cycle to a maximum of 75%.

One other oscillator function is to generate a saw-tooth waveform used to implement the built-in slope compensation. For this function the oscillator's output is connected to an internal Slope Ramp generator circuit. The resulting saw-tooth waveform is combined with the signal at the CS input via a summing (Σ) circuit. This has the effect of varying the amount of primary side current needed to end the present Gate pulse. The further into the cycle, the higher the ramp, and therefore the less CS signal needed to end the Gate pulse.



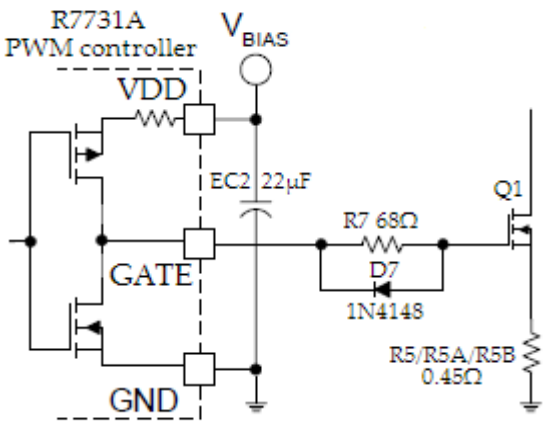
Current mode PWM converters with duty cycles exceeding 50% may oscillate at 1/2 the oscillator's frequency when trying to correct load variations. These subharmonic oscillations may persist indefinitely if there is no slope compensation. As the value of the compensation saw-tooth is increased, the faster the recovery from subharmonic oscillations. However, this also has the effect of gradually nullifying the benefits of current mode operation since the gate pulses end at a lower primary side current value. In other words, the ability of the current mode PWM converter to quickly correct input voltage variations is gradually diminished as the level of slope compensation is gradually increased. The built in R7731A slope

compensation is a compromise between quick recovery from subharmonic oscillation and optimal current mode gain.

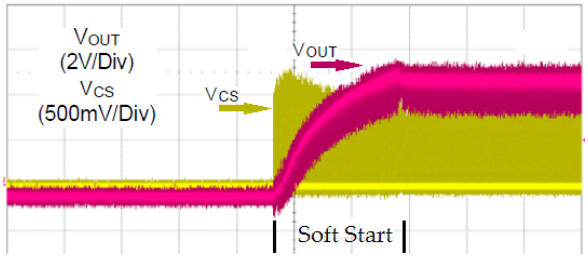
R7731A Gate, CS, and Comparator Circuits

The Gate Control:

The gate drive circuit uses the popular totem pole configuration. It has a signal rise time of 250ns, and a fall time of 150ns. This is a fairly slow rise and fall time which as a result reduces EMI but increases MOSFET power losses. Drivers that exhibit this behavior are called Soft Drivers. According to the manufacturer the R7731A Soft Driver is finely tuned to provide both EMI reduction and efficiency.



The Soft Driver current capability is rated at 200mA. The output voltage is clamped at 12V to protect the external MOSFET. In addition, an internal pull low circuit is activated during UVLO (under voltage lockout) to prevent the external MOSFET from turning on accidentally.



The gate pulse width is normally controlled by the external CV or CC feedback loops in conjunction with the CS (current sense) loop. However, during initial startup, a soft-start (SS) circuit takes control of the gate pulse width for about 4ms. The intent of this mechanism is to reduced the initial stresses associated with bringing the output voltage up to its nominal value from a zero starting point. To this effect, during the first 4ms after initial startup, the pulse width is slowly ramped up. Otherwise, if the feedback loops were given initial control, the pulse width would go as high as the CS (current sense) loop would allow in an attempt to bring the output voltage up to its nominal value immediately.

During light or no load conditions (for example, the scope is in standby and the battery pack is fully charged or there is no battery) the gate pulse width is so narrow that most of the consumed power is due to losses. To reduce power consumption during these periods and meet 'green mode' guidelines, a number of different schemes have been implemented by PWM controller manufacturers. The R7731A uses the Burst Mode or the VDD Holdup Mode during these periods.

The Burst Mode is entered when the feedback signal voltage drops below a threshold named VBURL. This blocks the gate pulses and all switching stops. As a result the output voltage eventually drops and the feedback voltage begins to raise. When it reaches a threshold named VBURH, the gate pulses are enabled and switching resumes. This process is repeated over and over again until there is enough load to keep the feedback voltage consistently above VBURL.

The VDD Holdup Mode is designed to prevent the controller from shutting down if switching is reduced to a level where the transformer's auxiliary winding is unable to produce enough current to supply the controller's VDD input. To this effect the VDD voltage is monitored and if it drops to 11V any other gate controls are bypassed and enough gate pulses are provided to maintain VDD above 11V.

The CS input:

The COMP input:

THIS SECTION IS INCOMPLETE, THE BELOW IS JUST A NOTE TO MYSELF

The CV error amplifier senses load variations by monitoring the voltage at the 8.4V output. As a result, the extra phase delay and resonance of the second stage filter (L1 and EC5) affects the high frequency low gain portion of its response curve. Using the 8.4V(raw) output to complete the feedback loop circuit via the opto-coupler's light emitting diode cancels out the phase delay introduced at the error amplifier end of the circuit. The net effect is that the overall response and phase of the feedback loop circuit is the same as if the second stage filter didn't exist.