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JADE MCT DIGITAL OUTPUT SPECIFICATION

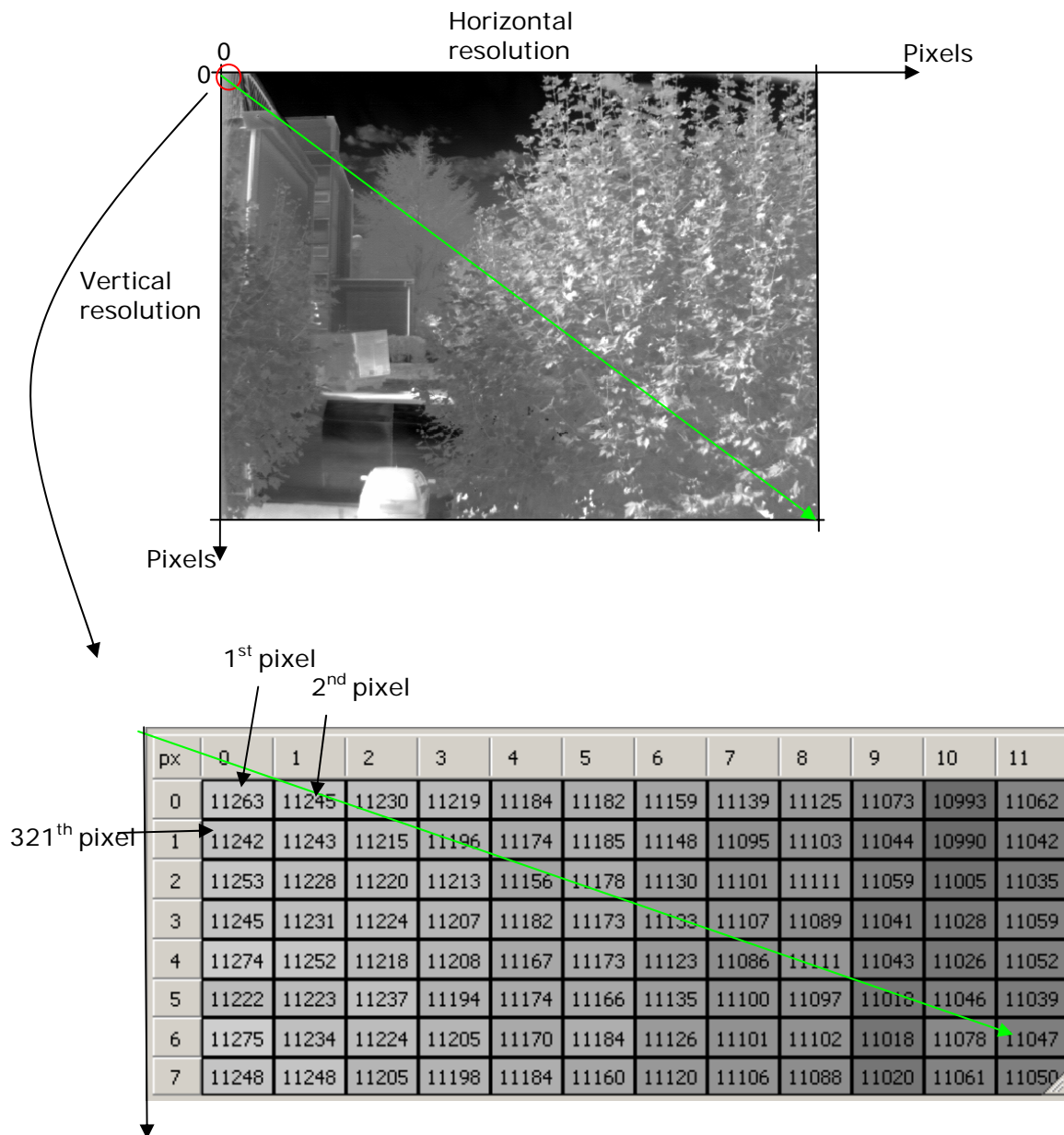
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1. INTRODUCTION

This Document describes signals generate by a Cirrus-IDMM067 for a digital acquisition.

1.1 Structure



1.2 Industrial Camera Pin out

Connector:

Manufacturer: **Souriau**

Ref: **85106J2041S50**

| Designation | Industrial Connector SOURIAU 41 Female |
|-----------------------|---|
| +DATA D0 | A |
| - DATA D0 | B |
| + DATA D1 | C |
| - DATA D1 | D |
| + DATA D2 | E |
| - DATA D2 | F |
| + DATA D3 | G |
| - DATA D3 | H |
| + DATA D4 | J |
| - DATA D4 | K |
| + DATA D5 | L |
| - DATA D5 | M |
| + DATA D6 | N |
| - DATA D6 | P |
| + DATA D7 | R |
| - DATA D7 | S |
| + DATA D8 | T |
| - DATA D8 | U |
| + DATA D9 | V |
| - DATA D9 | W |
| + DATA D10 | X |
| - DATA D10 | Y |
| + DATA D11 | Z |
| - DATA D11 | a |
| + DATA D12 | b |
| - DATA D12 | c |
| + DATA D13 | d |
| - DATA D13 | e |
| + DATA D14 (Note 1) | f |
| - DATA D14 (Note 1) | g |
| + DATA D15 (Note 1) | h |
| - DATA D15 (Note 1) | i |
| + DATA LINE | j |
| - DATA LINE | k |
| + DATA FRAME | m |
| - DATA FRAME | n |
| + DATA CLOCK | p |
| - DATA CLOCK | q |
| GND | r |
| +DATA CCLOCK (Note 2) | s |
| -DATA CCLOCK (Note 2) | t |

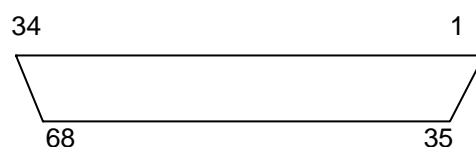
1.3 Commercial Camera Pint out

Connector:

Manufacturer: **Harting**

Ref: **60 04 068 5344**

| Designation | SCSI Commercial Connector | Designation | SCSI Commercial Connector |
|---------------------|---------------------------|--------------------|---------------------------|
| GND | 1 | NC | 18 |
| GND | 35 | NC | 52 |
| + DATA_D0 | 2 | NC | 19 |
| - DATA_D0 | 36 | NC | 53 |
| + DATA_D1 | 3 | NC | 20 |
| - DATA_D1 | 37 | NC | 54 |
| + DATA_D2 | 4 | NC | 21 |
| - DATA_D2 | 38 | NC | 55 |
| + DATA_D3 | 5 | NC | 22 |
| - DATA_D3 | 39 | NC | 56 |
| + DATA_D4 | 6 | NC | 23 |
| - DATA_D4 | 40 | NC | 57 |
| + DATA_D5 | 7 | NC | 24 |
| - DATA_D5 | 41 | NC | 58 |
| + DATA_D6 | 8 | NC | 25 |
| - DATA_D6 | 42 | NC | 59 |
| + DATA_D7 | 9 | NC | 26 |
| - DATA_D7 | 43 | NC | 60 |
| + DATA_D8 | 10 | NC | 27 |
| - DATA_D8 | 44 | NC | 61 |
| + DATA_D9 | 11 | NC | 28 |
| - DATA_D9 | 45 | NC | 62 |
| + DATA_D10 | 12 | NC | 29 |
| - DATA_D10 | 46 | NC | 63 |
| + DATA_D11 | 13 | NC | 30 |
| - DATA_D11 | 47 | NC | 64 |
| + DATA_D12 | 14 | +DATA_CCLOCK (Note | 31 |
| - DATA_D12 | 48 | -DATA_CCLOCK (Note | 65 |
| + DATA_D13 | 15 | + DATA_CLOCK | 32 |
| - DATA_D13 | 49 | - DATA_CLOCK | 66 |
| + DATA_D14 (Note 1) | 16 | + DATA_FRAME | 33 |
| - DATA_D14 (Note 1) | 50 | - DATA_FRAME | 67 |
| + DATA_D15 (Note 1) | 17 | + DATA_LINE | 34 |
| - DATA_D15 (Note 1) | 51 | - DATA_LINE | 68 |



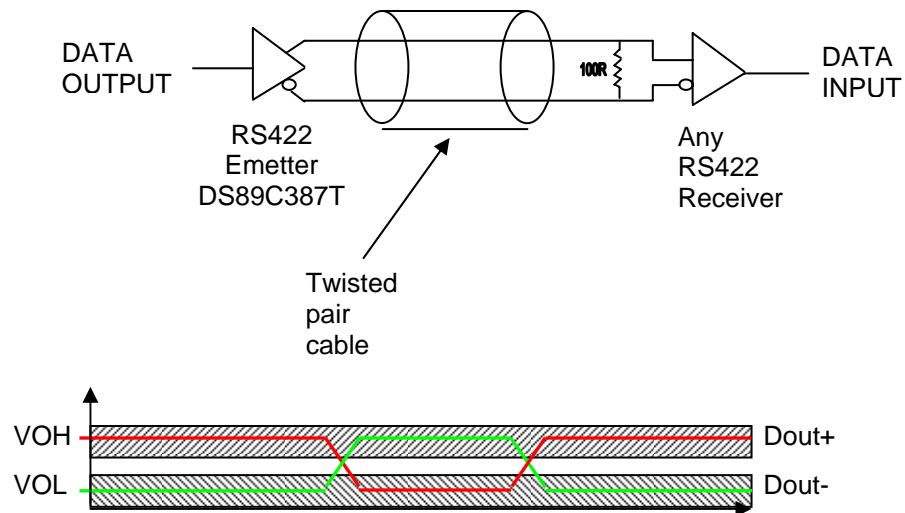
Connector SCSI – Front View

Note 1: These signals are available if the camera is able to switch in multi-ti mode.

Note 2: These signals are available on camera manufactured after 2003

2. RS422 SPECIFICATION

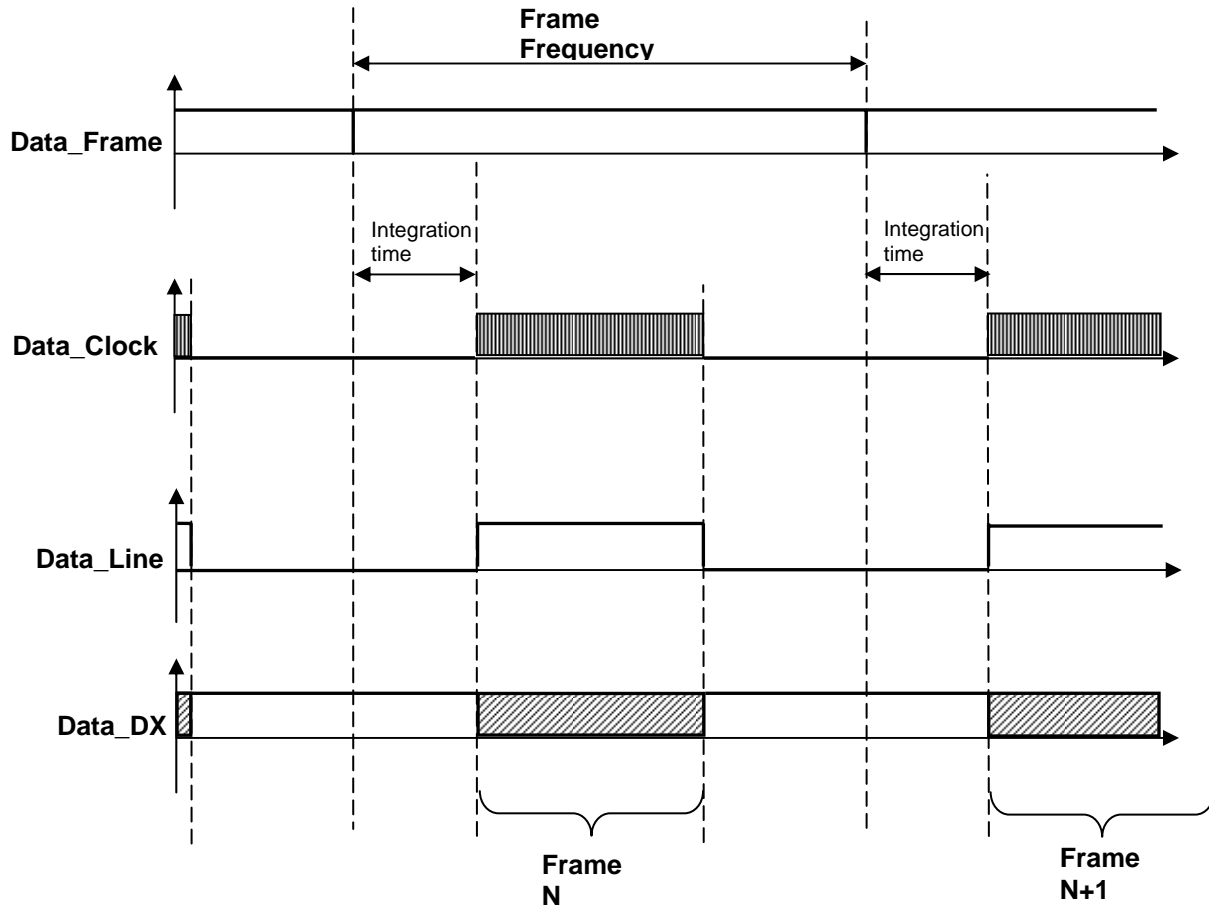
Electrical Characteristic:



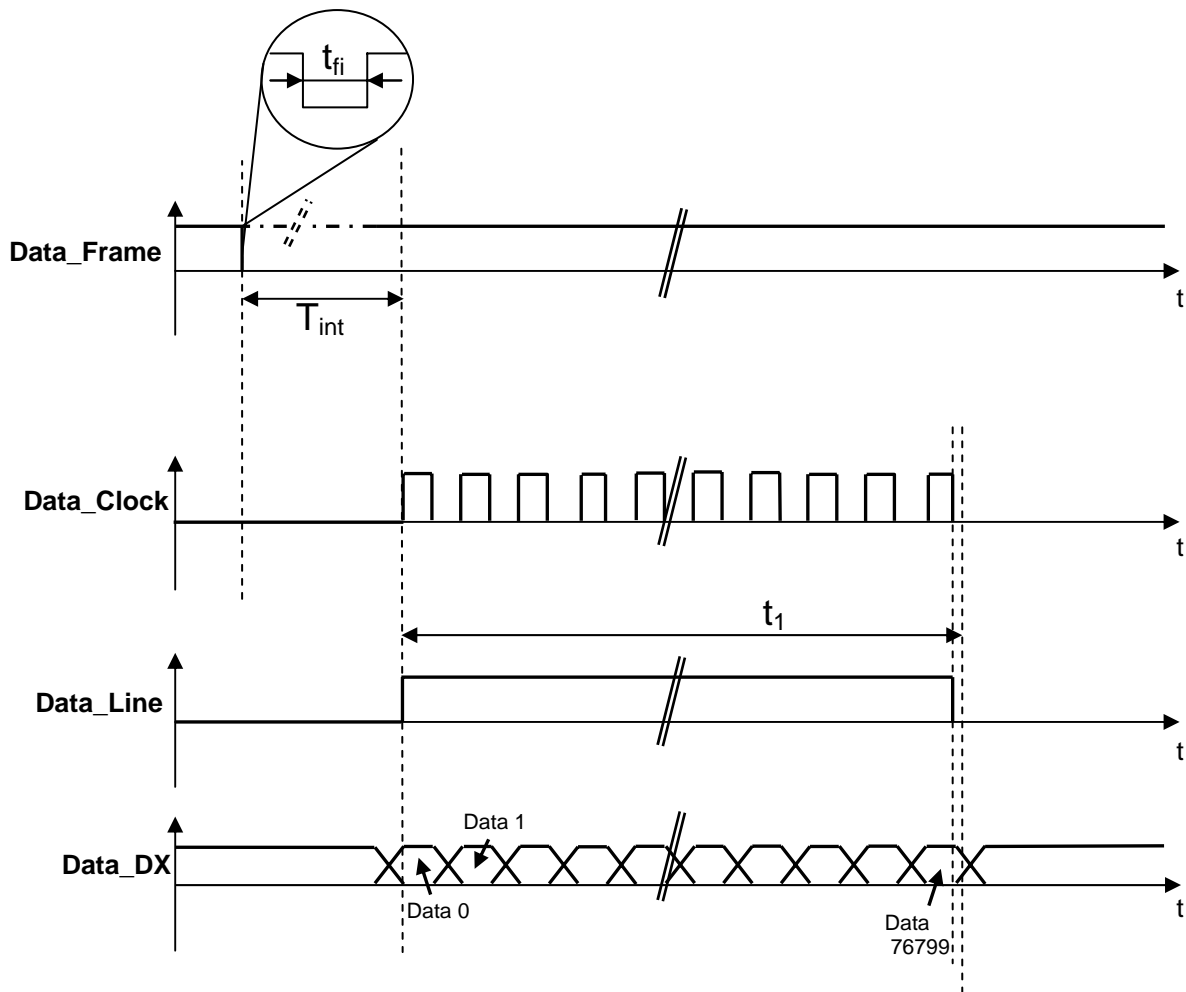
| Symbol | Parameter | Min | Typ | Max | Units |
|--------|---------------------|-----|-----|-----|-------|
| VOH | Output High Voltage | 2.5 | 3.4 | | V |
| VOL | Output Low Voltage | | 0.2 | 0.5 | V |

For more details about RS422 Technology, see Application notes 214 and datasheet of the DS89C387 RS-422 Driver on the national semiconductor web site.

2.1 Cirrus Sofradir IDMX067 Digital Output



- ❑ Data_Frame indicates the beginning of each frame. The frequency is limited only by the number of pixels, Data_clock frequency, and the integration time.
- ❑ Data_Clock is the pixel clock. The number of Data_Clock period starts from 64(minimum horizontal resolution) to 320 by 4 pixels step. Data_DX (D0 to D15) are available on the rising edge of Data_Clock. The Data_Clock frequency up to 20Mhz.
- ❑ Data_Line indicates the beginning of Data. The length of data_line is the vertical resolution, and it can be adjust from 2 to 240 by 1 lines step, for example with a master clock at 20MHz and a resolution of 320*240, the data_line length is $(320 \times 240) / 20\text{Mhz} = 3.84\text{ms}$.
- ❑ Data_DX are digital data from D0 to D15, they are available on Data_Clock rising edge.
- ❑ Data_CCLOCK is a Continuous Clock, i.e. this clock is always available, and clocking at the pixel clock frequency.



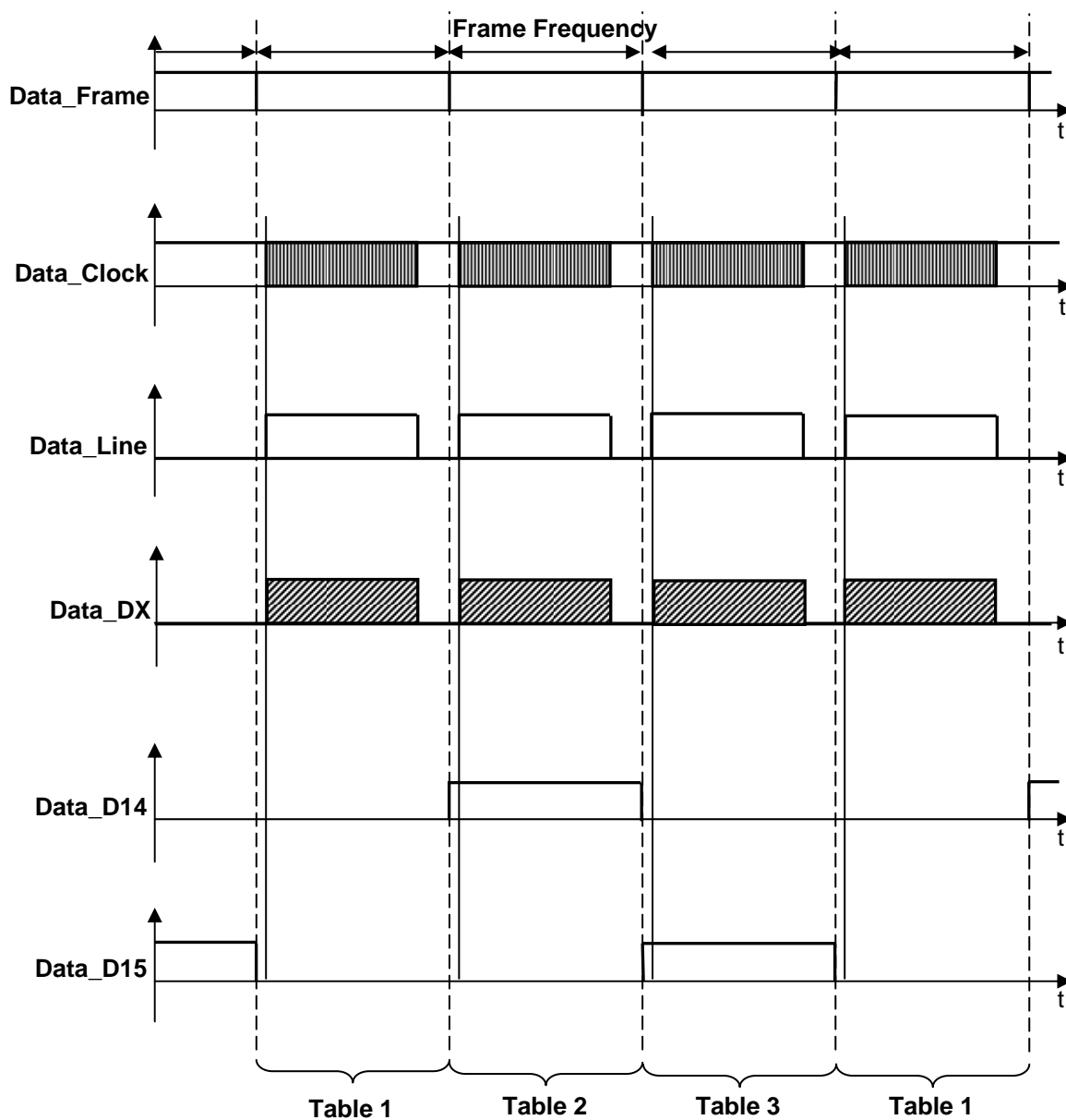
| | Symbol | Conditions | MIN | MAX | Unit |
|--------------------|-----------|--|------|-----|---------|
| Integration time | T_{int} | | 3 | | μs |
| Top_Frame Duration | T_{fi} | Master Clock = 20MHz: Master Clock = 16MHz: | 4.5 | 5.7 | μs |
| Line Duration | T_1 | Master Clock = 20MHz; 320*240 pix Master Clock = 16MHz; 320*240 pix | 3.84 | 4.8 | μs |

Line Duration:

$$T_1 (\mu s) = \frac{\text{Horizontal resolution (pixel)} * \text{Vertical resolution (pixel)}}{\text{Pixel Clock (MHz)}}$$

2.2 Multi-Ti Mode

In multi-integration mode, each NUC Table are signed by 2 Bits (DATA15&DATA14). When this mode is selected (see Cirrus User manual for more details), it's performed a rolling of the NUC table. At each Top Frame, the next NUC Table (from 1 to 3max) is available.



Here is Data_D14 and D15, this 2 signal indicate the Current Nuc available.