PLESSEY ML101/102/153/154

MOSAIC ANALOGUE SWITCHES

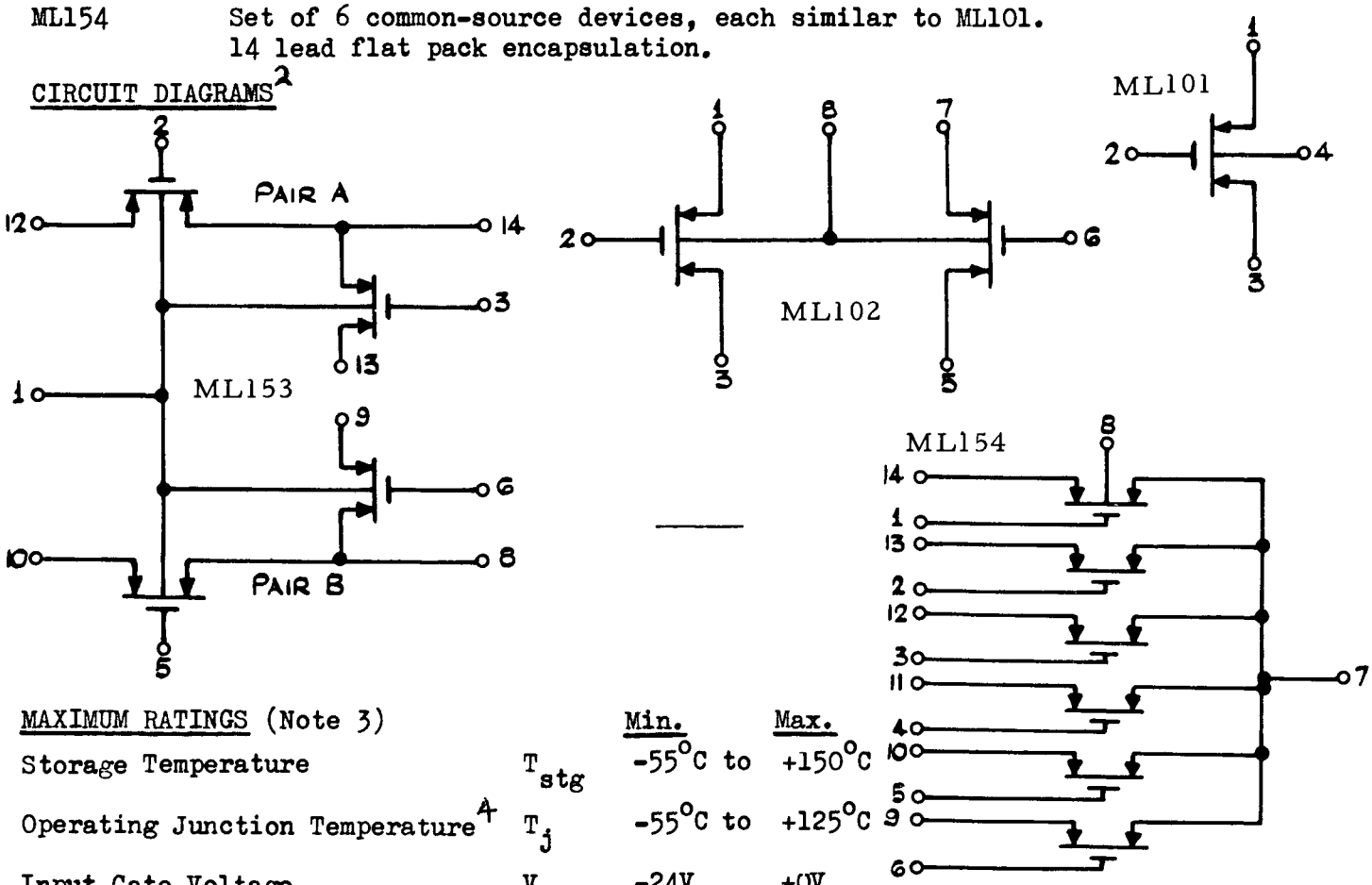
ADVANCE LABORATORY INFORMATION

This series of MOSAIC[1] devices consists of various combinations of well matched p-channel enhancement MOS transistors. All devices in the range incorporate gate protection diodes to obviate the need for special care in handling. As a consequence, they are not so suitable for ultra high input impedance applications as are devices lacking such protection, for example the MTO 1. They are primarily intended for use as analogue switches, low level choppers, multiplexers and so on.

Description

ML101	Single MOS device for use as a chopper. Resembles MTO 1 but incorporates gate protection. TO-18 encapsulation.
ML102	Matched pair of devices similar to the ML101. 8 lead TO-5 encapsulation.
ML153	Two common-source pairs, each pair similar to the ML102. 14 lead flat pack encapsulation.
ML154	Set of 6 common-source devices, each similar to ML101. 14 lead flat pack encapsulation.

CIRCUIT DIAGRAMS[2]



MAXIMUM RATINGS (Note 3)

		Min.	Max.
Storage Temperature	T_{stg}	-55°C to	+150°C
Operating Junction Temperature[4]	T_j	-55°C to	+125°C
Input Gate Voltage	V_{GSub}	-24V	+0V
Drain-Source Voltage	V_{DS}	-24V	+24V
Drain-Substrate Voltage	V_{DSub}	-24V	+0V
Source-Substrate Voltage	V_{SSub}	-24V	+0V
Drain Current	I_D		50mA

ELECTRICAL CHARACTERISTICS (at 25°C unless otherwise stated) INTEGRATED CIRCUITS

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Gate threshold voltage	V_T	-3.8	-5.1	-6.5	Volts	$V_{GS} = V_{DS}$ $I_D = 10uA$
Drain-source ON resistance	R_{ON}		470	700	ohms	V_{DS} =0V V_{SSub} =0V V_{GS} = -10V
			200	350	ohms	V_{DS} = 0V V_{SSub} = 0V V_{GS} = -20V
Matching of R_{ON} (between devices in the same package)	ΔR_{ON}		±4%	±10%		V_{GS} = -10V to -24V
Gate-source capacitance	C_{GS}		3.5	5.3	pF	$V_{DS} = V_{GS}$ I_D = 1mA f = 1 MHz
Gate-drain capacitance	C_{GD}		2.0	3.0	pF	$V_{DS} = V_{GS}$ I_D = 1mA f = 1 MHz
Drain-source capacitance	C_{DS} ML101/ML102		1.7	3.0	pF	$V_{DS} = V_{GS}$
	C_{DS} ML153/ML154		2.7	4.1	pF	I_D = 1mA f = 1 MHz
Drain-substrate capacitance	C_{DSub} ML101/ML102		4.0	6.0	pF	V_{DSub} = 0V
	C_{DSub} ML153/ML154		5.5	8.3	pF	f= 1 MHz
Source-substrate capacitance	C_{SSub} ML101/ML102		5.1	7.7	pF	V_{SSub} = 0V
	C_{SSub} ML153		11	16.5	pF	f = 1 MHz
	C_{SSub} ML154		32	48	pF	
Drain-source leakage			0.2	20	nA	V_{GS} = 0V V_{DS} = -20V
Drain-substrate leakage			1	20	nA	V_{GS} = 0V

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MOSAIC ANALOGUE SWITCHES (Contd)

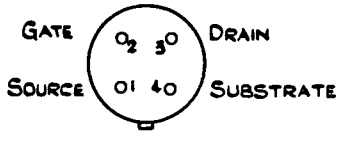
Electrical Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Source-substrate leakage	ML101 ML102		1	20	nA	V_{DSub} = -20V V_{GS} = 0V
	ML153		3	20	nA	
	ML154		4.5	20	nA	V_{SSub} = -20V
Gate-channel leakage [5]				1	nA	V_{GSub} = -24V
						V_{DSub} = V_{SSub} = 0V
Temperature coefficient of R_{ON} (referred to value of R_{ON} at 25°C)			0.45		%/°C	

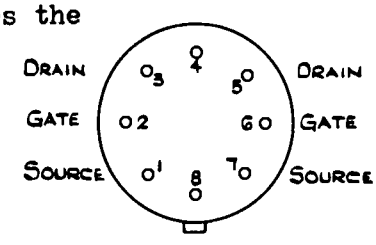
Notes

1. Metal Oxide Silicon Advanced Integrated Circuit: Plessey Trade Mark applied for.
2. Because of the symmetrical nature of the MOST, identification of Source and Drain is arbitary. In multiple devices having a common terminal this is designated the Source.
3. The maximum ratings are limiting absolute values above which life or satisfactory performance may be impaired.
4. A chip temperature of 125°C must not be exceeded. The ratings for the different encapsulation are as follows:-
   TO-18 Junction to ambient thermal resistance of 486°C/W and junction to case thermal resistance of 146°C/W.
   TO-5 and 14 lead flat pack. Junction to ambient thermal resistance of 250°C/W and junction to case thermal resistance of 80°C/W.
5. Gate-channel 'leakage' is a consequence of the gate protection device. When the device is turned on by negative gate voltage a current is also induced in a spurious MOST between the gate protection diode and the source-drain channel. Operation at lower gate voltages reduces the effect.

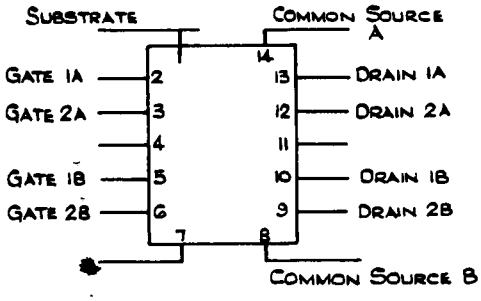
PIN CONNECTIONS.



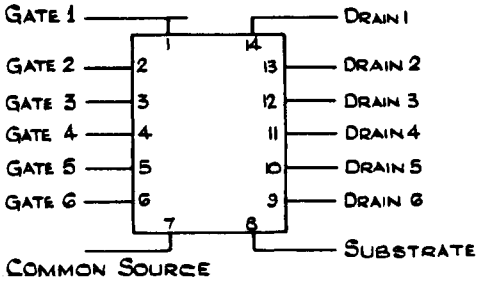
ML 101
Bottom view 4 lead TO-18



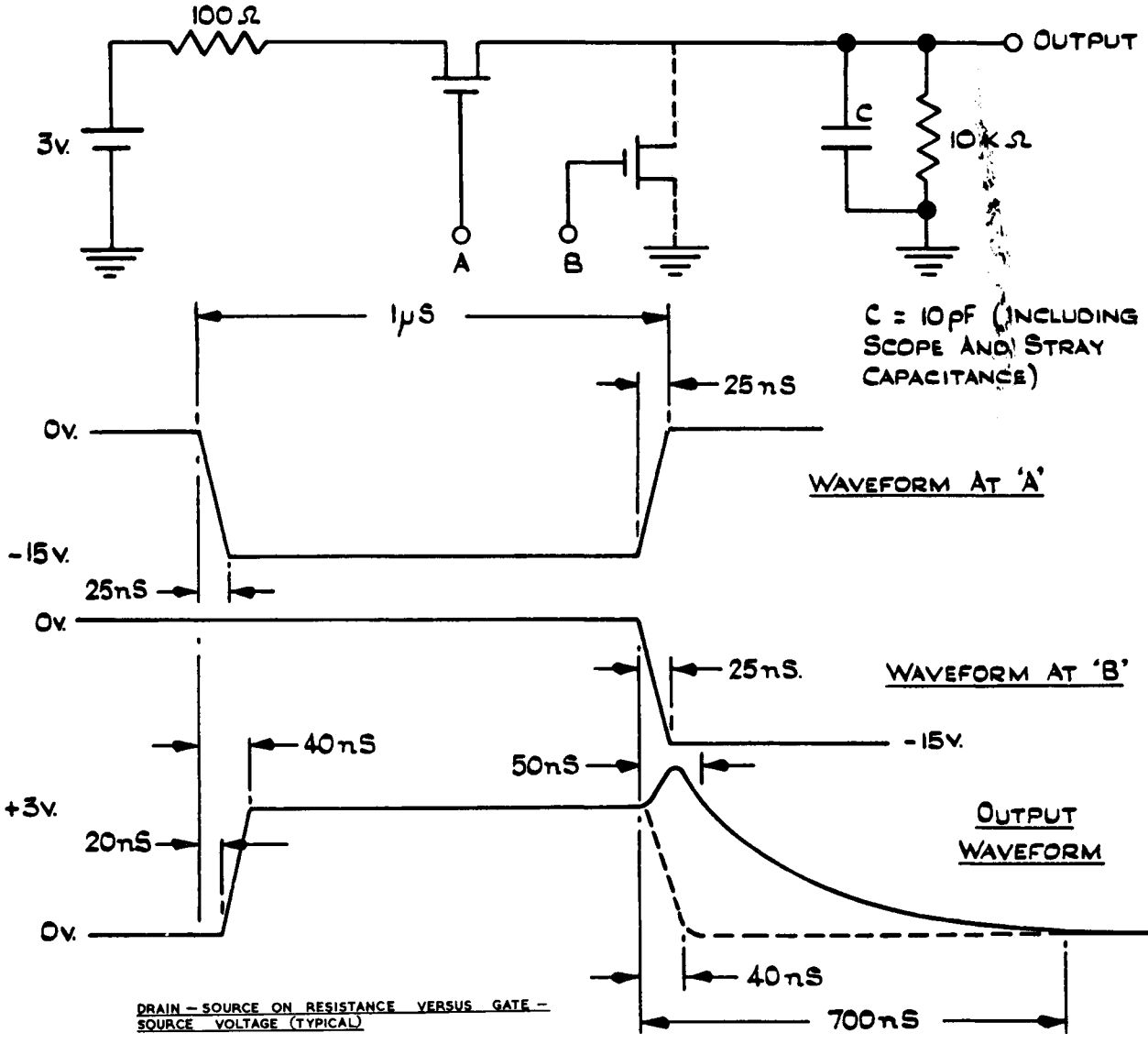
ML 102
Bottom view 8 lead TO-5



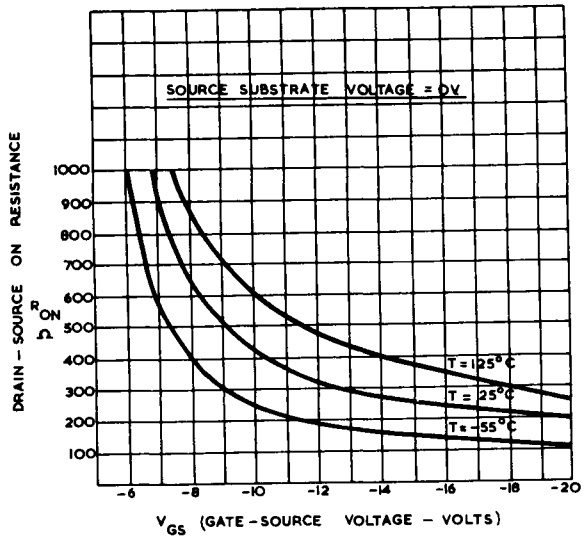
ML 153
14 lead flat pack.



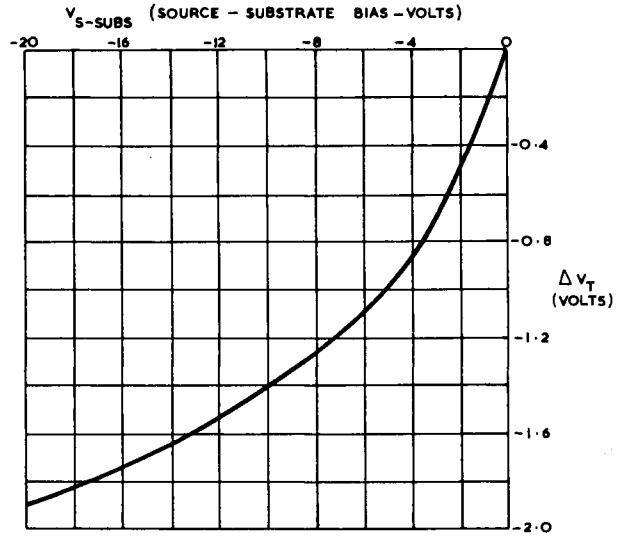
ML 154
14 lead flat pack



DRAIN – SOURCE ON RESISTANCE VERSUS GATE – SOURCE VOLTAGE (TYPICAL)



CHANGE OF THRESHOLD VOLTAGE (ΔV_T) VERSUS SOURCE – SUBSTRATE BIAS VOLTAGE (TYPICAL)



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